IFN5196, IFN5197, IFN5198, IFN5199

N-Channel Matched Dual Silicon Junction Field-Effect Transistor

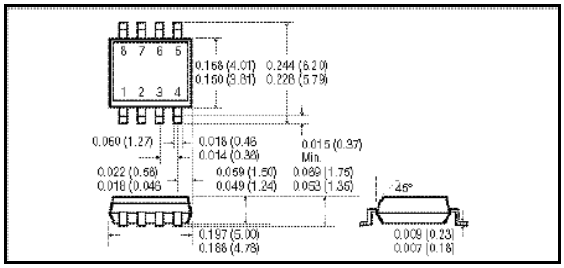
- **Improved Replacement for the 2N5196, 2N5197, 2N5198, 2N5199**
- **Differential Inputs**

Absolute maximum ratings at $T_A = 25^oC$

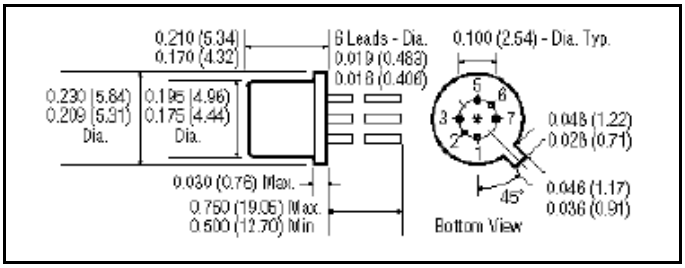
Reverse Gate Source & Gate Drain Voltage	-50V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	250 mW
Power Derating	2.6 mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

At 25°C free air temperature		IFN5196, IFN5197, IFN5198, IFN5199				Process NJ16	
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	-50			V	I_G = -1 uA, V_{DS} = 0 V	
Gate Reverse Current	I_{GSS}			-25 -50	pA nA	V_{GS} = -30 V, V_{DS} = 0 V	150°C
Gate Current	I_G			-50 -15	pA nA	V_{DG} = 10 V, I_D = -200 uA	125°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	-0.7		-4	V	V_{DS} = 20 V, I_D = 1 nA	
Drain Saturation Current (pulsed)	I_{DSS}	0.7		7	mA	V_{DS} = 20 V, V_{GS} = 0 V	
Gate Source Voltage	V_{GS}	-0.2		-3.8	V	V_{DG} = 20 V, I_D = -200 uA	
Dynamic Electrical Characteristics							
Common-Source Forward Transconductance	g_{fs}	1		4	mS	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
Common-Source Output Conductance	g_{os}			50	µS	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
Common-Source Input Capacitance	C_{iss}			6	pF	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 MHz
Common-Source Reverse Transfer Capacitance	C_{rss}			2	pF	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 MHz
Noise Factor R_G = 10 MΩ	NF			0.5	dB	V_{DS} = 20 V, V_{GS} = 0 V	f = 100 Hz
Equivalent Short Circuit Input Noise Voltage	$\sim e_N$			20	nV/√Hz	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz

		IFN5196		IFN5197		IFN5198		IFN5199			
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Test Conditions**
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2} \rvert$		5		5		10		15	mV	V_{DG} = 20 V, I_D = -200 uA
Differential Gate Source Voltage with Temperature [1]	$\frac{\Delta \lvert V_{GS1}-V_{GS2} \rvert}{\Delta T}$		5		10		20		40	µV/°C	V_{DG} = 20 V, I_D = -200 uA
Differential Gate Current @125°	$\lvert I_{G1}-I_{G2} \rvert$		5		5		5		5	nA	V_{DG} = 20 V, I_D = -200 uA
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	0.95	1	0.95	1	0.95	1	0.95	1		V_{DS} = 20 V, V_{GS} = 0 V
Transconductance Ratio @ f = 1 kHz	$\frac{g_{fs1}}{g_{fs2}}$	0.97	1	0.97	1	0.95	1	0.95	1		V_{DG} = 20 V, I_D = -200 uA
Differential Output Conductance @ f = 1 kHz	$\lvert g_{os1}- g_{os2} \rvert$		1		1		1		1	uS	V_{DG} = 20 V, I_D = -200 uA



SOIC-8 Package **Pin Configuration**
SMP5196, SMP5197, SMP5198, SMP5199 1-G1, 2-D1, 3-S1, 4-G2, 5-G2, 6-D2, 7-S2, 8-G1



TO-71: **Pin Configuration**
IFN5196, IFN5197, IFN5198, IFN5199 1-S1, 2-D1, 3-G1, 4-S2, 5-D2, 6-G2

Note 1: T = -55°C, 25°C, 125°C

Note 2: Dimensions in Inches (mm)

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