



BT152X-400R

SCR

18 March 2014

Product data sheet

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT186A (TO-220F) "full pack" plastic package intended for use in applications requiring very high inrush current capability and high thermal cycling performance.

2. Features and benefits

- Good blocking voltage capability
- High thermal cycling performance
- Isolated mounting base package
- Planar passivated for voltage ruggedness and reliability
- Very high current surge capability

3. Applications

- Capacitive Discharge Ignition (CDI)
- Crowbar protection
- Inrush protection
- Motor control
- Voltage regulation

4. Quick reference data

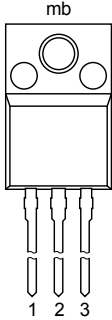
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	400	V
V_{RRM}	repetitive peak reverse voltage		-	-	400	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	-	200	A
$I_{\text{T(RMS)}}$	RMS on-state current	half sine wave; $T_{\text{h}} \leq 43\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	20	A
Static characteristics						
I_{GT}	gate trigger current	$V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; $T_{\text{j}} = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	3	32	mA



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 TO-220F (SOT186A)	
2	A	anode		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT152X-400R	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

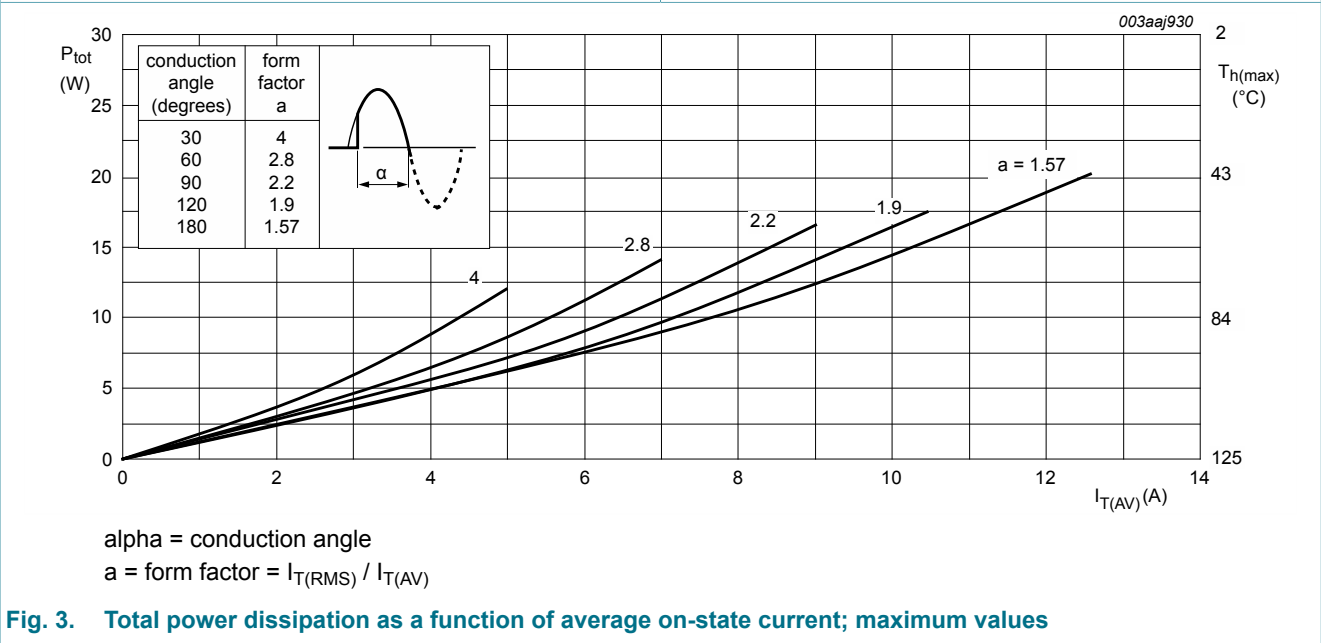
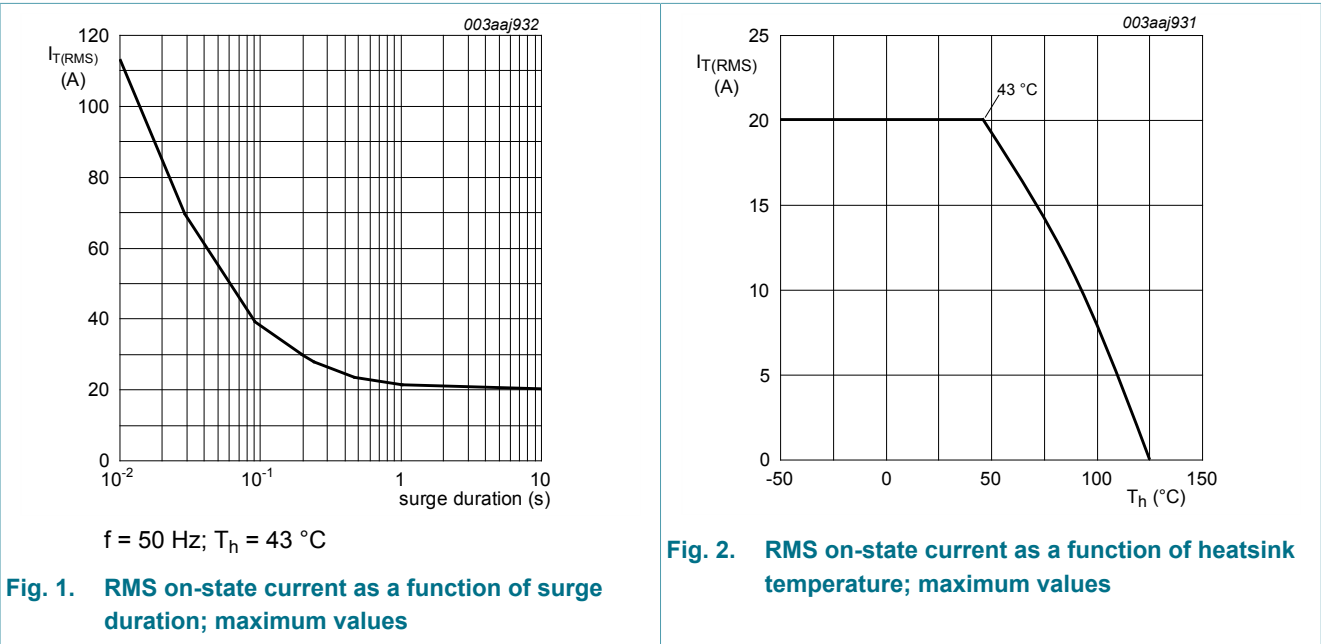
7. Limiting values

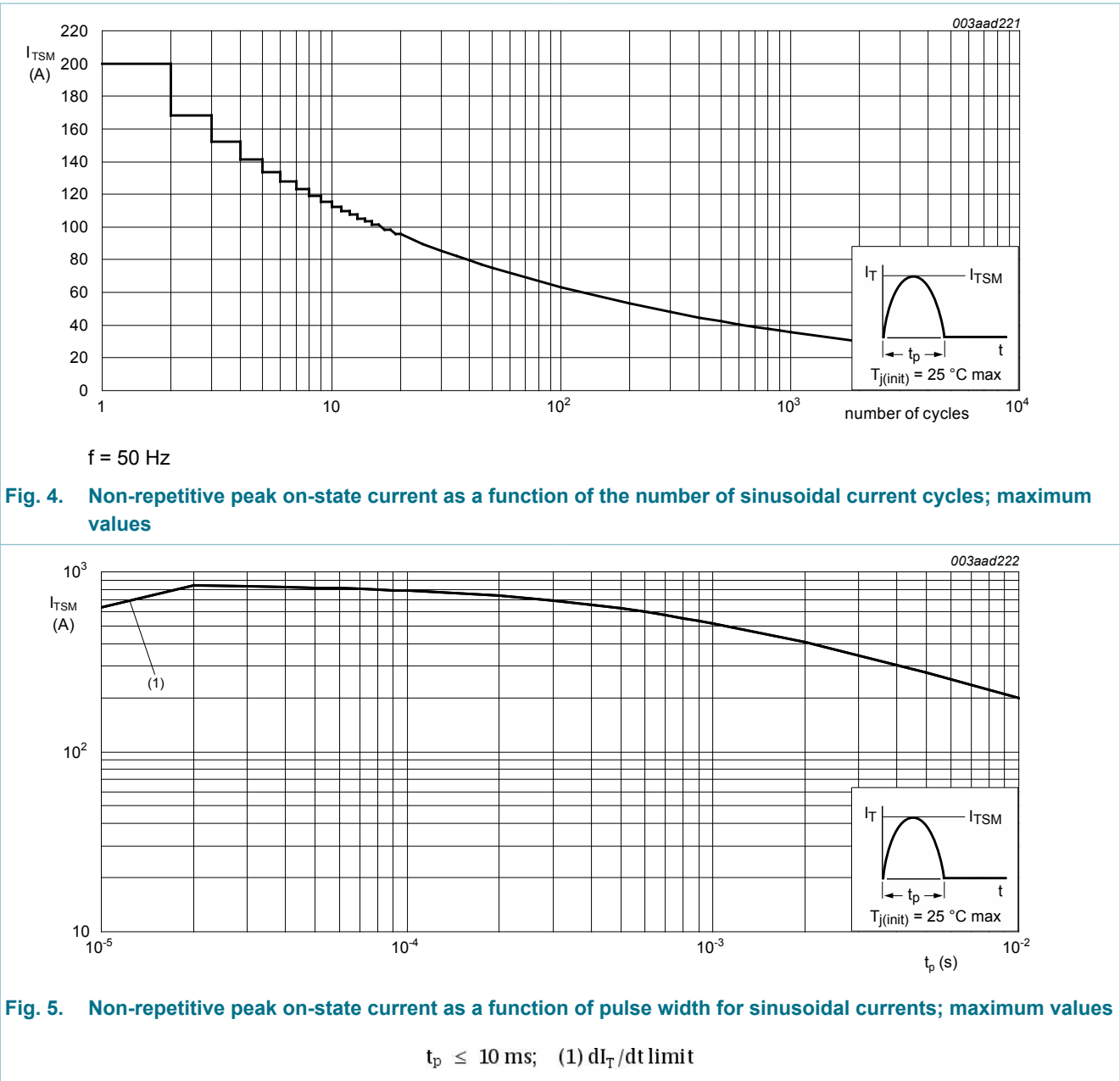
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	400	V
V_{RRM}	repetitive peak reverse voltage		-	400	V
$I_{\text{T(AV)}}$	average on-state current	half sine wave; $T_h \leq 43^\circ\text{C}$	-	13	A
$I_{\text{T(RMS)}}$	RMS on-state current	half sine wave; $T_h \leq 43^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	20	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	200	A
		half sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$; $t_p = 8.3\text{ ms}$	-	220	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	200	A^2s
di_{T}/dt	rate of rise of on-state current	$I_{\text{T}} = 50\text{ A}$; $I_{\text{G}} = 0.2\text{ A}$; $di_{\text{G}}/dt = 0.2\text{ A}/\mu\text{s}$	-	200	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	5	A

Symbol	Parameter	Conditions		Min	Max	Unit
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	20	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C





8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	with heatsink compound; Fig. 6	-	-	4	K/W
		without heatsink compound; Fig. 6	-	-	4.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	55	-	K/W

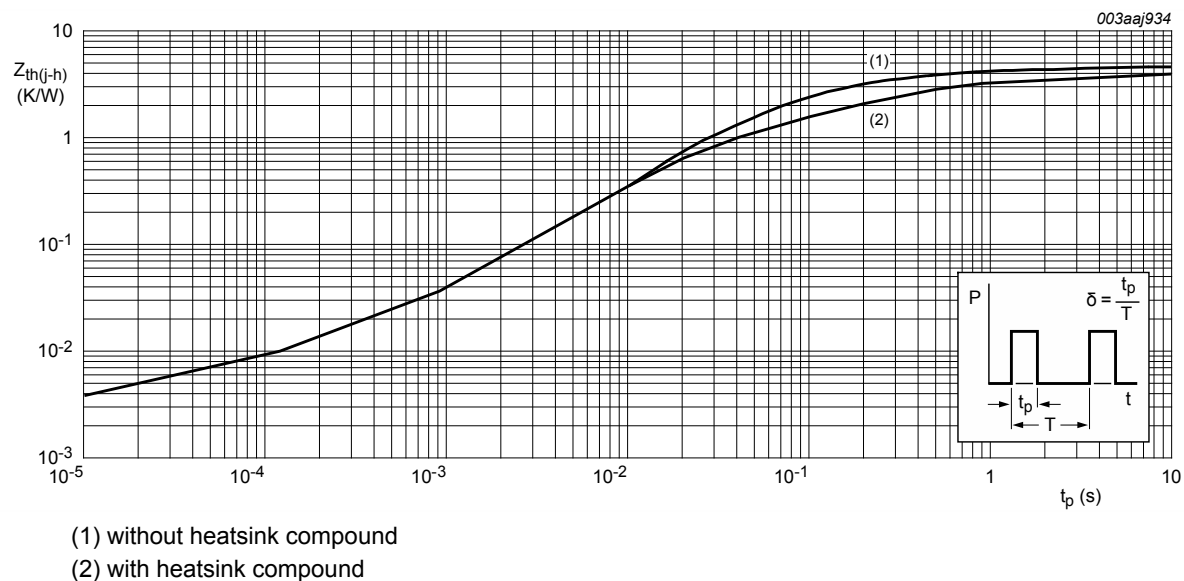


Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse width

9. Isolation characteristics

Table 6. Isolation characteristics

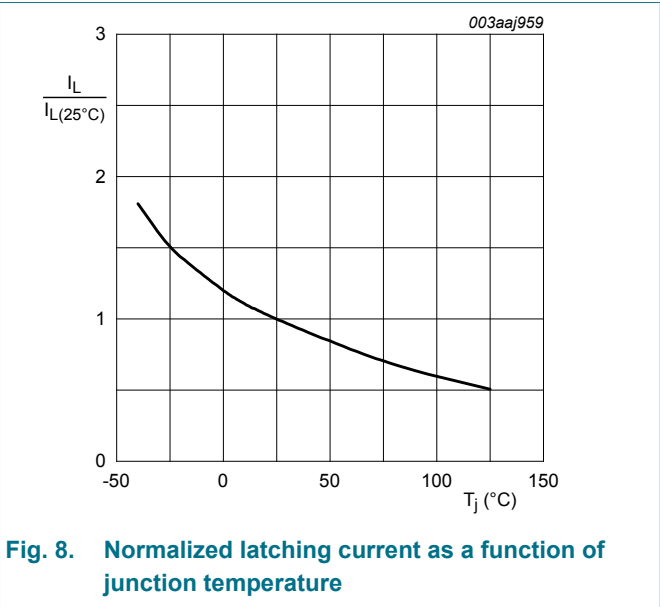
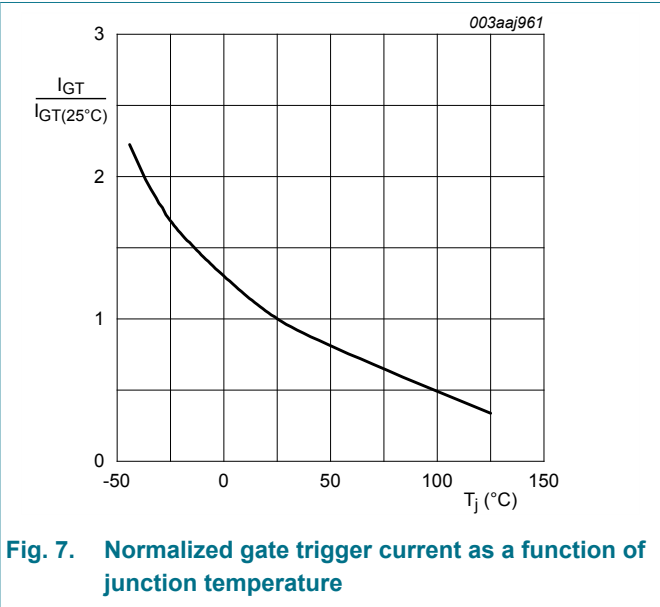
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; $50\text{ Hz} \leq f \leq 60\text{ Hz}$; $RH \leq 65\%$; $T_h = 25\text{ }^\circ\text{C}$	-	-	2500	V
C_{isol}	isolation capacitance	from anode to external heatsink; $f = 1\text{ MHz}$; $T_h = 25\text{ }^\circ\text{C}$	-	10	-	pF

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	3	32	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	25	80	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	15	60	mA
V_T	on-state voltage	$I_T = 40\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	1.4	1.75	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11	-	0.6	1	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$; Fig. 11	0.25	0.4	-	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_D	off-state current	$V_D = 400\text{ V}; T_j = 125\text{ }^{\circ}\text{C}$		-	0.2	1	mA
I_R	reverse current	$V_R = 400\text{ V}; T_j = 125\text{ }^{\circ}\text{C}$		-	0.2	1	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 268\text{ V}; T_j = 125\text{ }^{\circ}\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM}); \text{gate open circuit; exponential waveform; Fig. 12}$		200	300	-	V/ μs
t_{gt}	gate-controlled turn-on time	$I_{TM} = 40\text{ A}; V_D = 400\text{ V}; I_G = 0.1\text{ A}; dI_G/dt = 5\text{ A}/\mu\text{s}; T_j = 25\text{ }^{\circ}\text{C}$		-	2	-	μs
t_q	commutated turn-off time	$V_{DM} = 268\text{ V}; T_j = 125\text{ }^{\circ}\text{C}; I_{TM} = 50\text{ A}; V_R = 25\text{ V}; (dI_T/dt)_M = 50\text{ A}/\mu\text{s}; dV_D/dt = 30\text{ V}/\mu\text{s}; R_{GK} = 100\text{ }\Omega; (V_{DM} = 67\% \text{ of } V_{DRM})$		-	70	-	μs



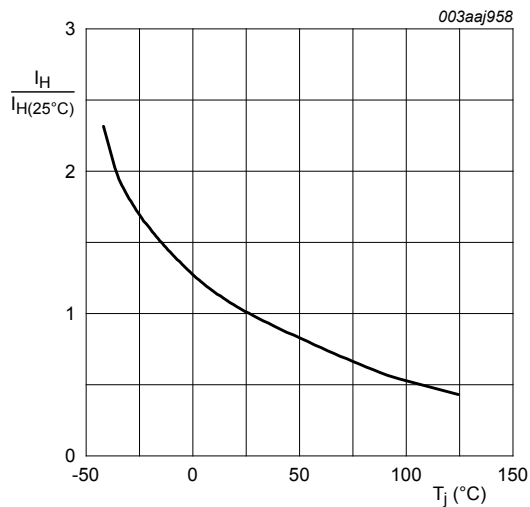
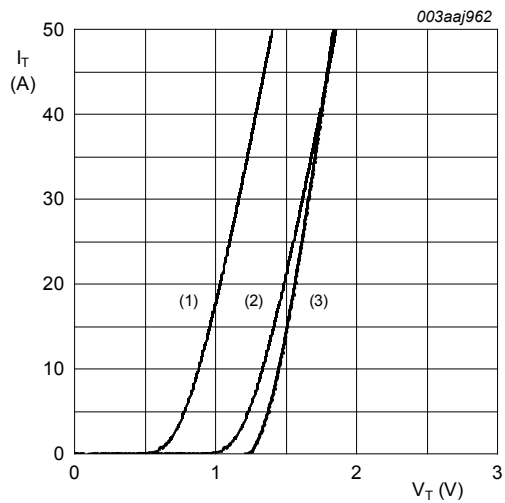


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.12\text{ V}; R_s = 0.015\ \Omega$
(1) $T_j = 125^\circ\text{C}$; typical values
(2) $T_j = 125^\circ\text{C}$; maximum values
(3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

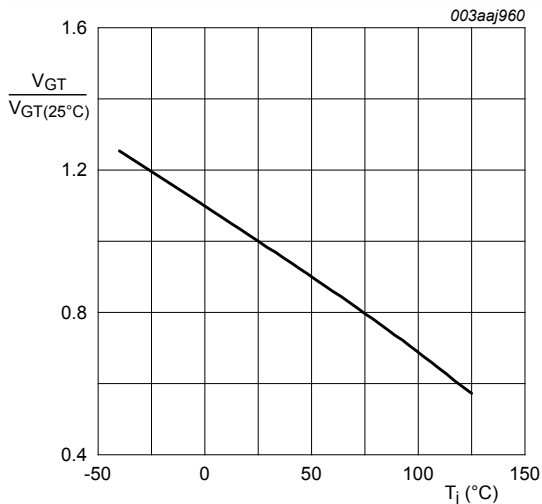
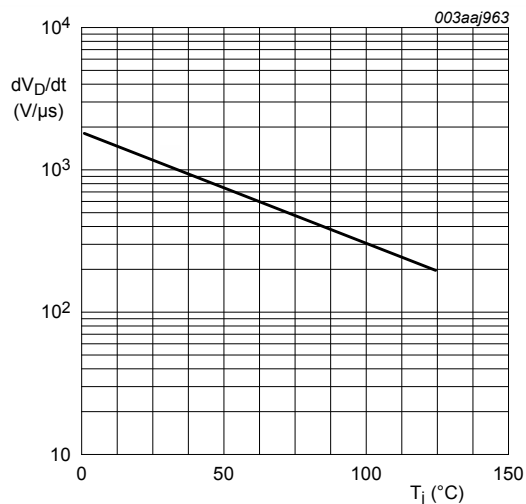


Fig. 11. Normalized gate trigger voltage as a function of junction temperature



gate open circuit

Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

11. Package outline

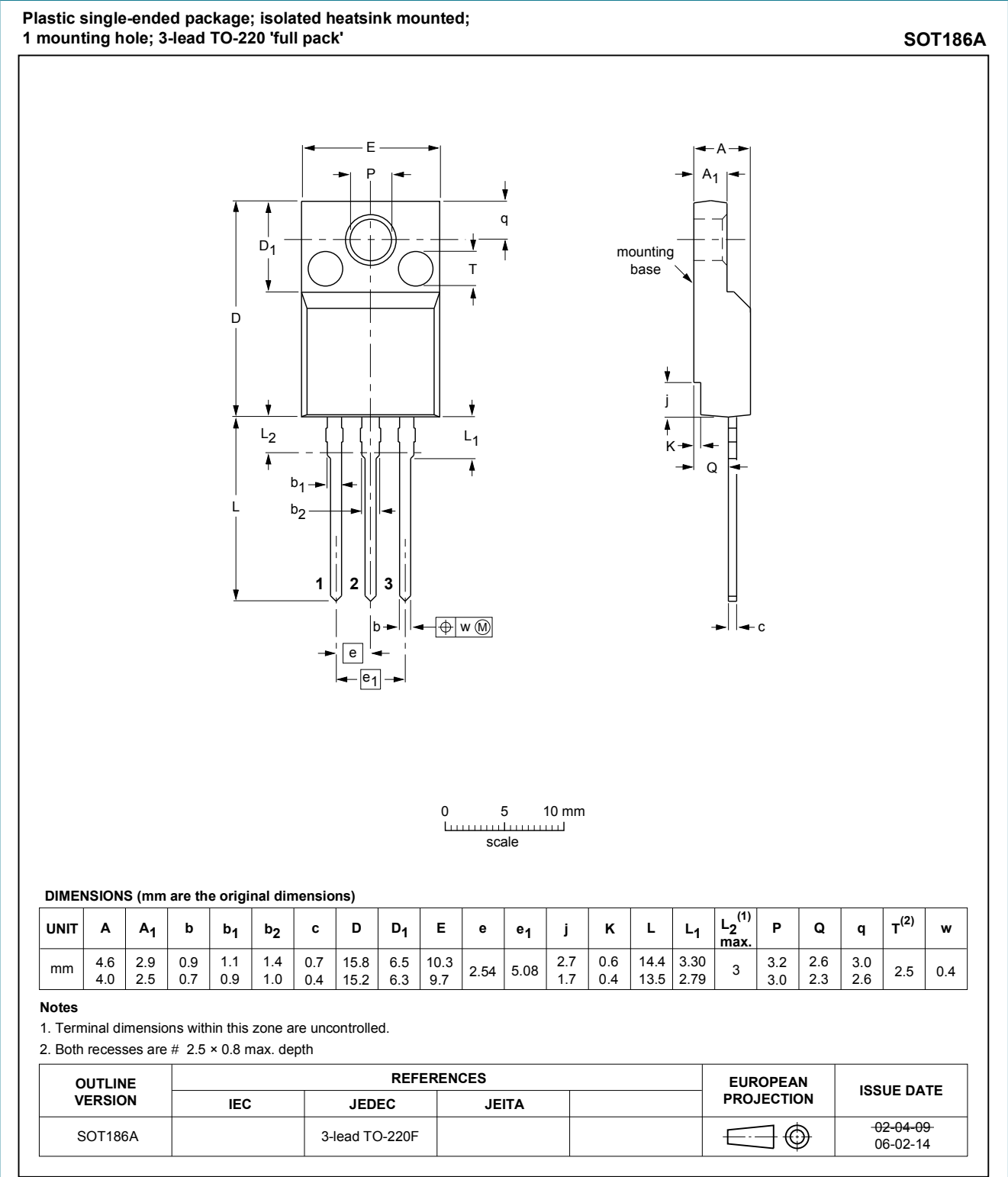


Fig. 13. Package outline TO-220F (SOT186A)

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