

# SN65LBC172, SN75LBC172 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

SLLS163E – JULY 1993 – REVISED APRIL 2006

- Meets or Exceeds EIA Standard RS-485
- Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments
- Support Data Rates up to and Exceeding Ten Million Transfers Per Second
- Common-Mode Output Voltage Range of –7 V to 12 V
- Positive- and Negative-Current Limiting
- Low Power Consumption . . . 1.5 mA Max (Output Disabled)
- Functionally Interchangeable With SN75172

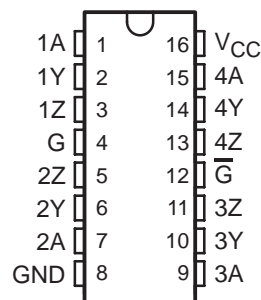
## description

The SN65LBC172 and SN75LBC172 are monolithic quadruple differential line drivers with 3-state outputs. Both devices are designed to meet the requirements of EIA Standard RS-485. These devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown circuitry making it suitable for party-line applications in noisy environments. Both devices are designed using LinBiCMOS™, facilitating ultra-low power consumption and inherent robustness.

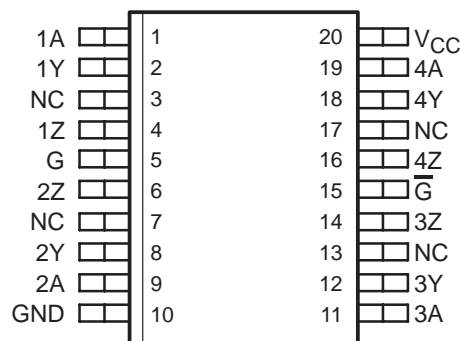
Both the SN65LBC172 and SN75LBC172 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. These devices offer optimum performance when used with the SN75LBC173 or SN75LBC175 quadruple line receivers. The SN65LBC172 and SN75LBC172 are available in the 16-pin DIP package (N) and the 20-pin wide-body small-outline inline-circuit (SOIC) package (DW).

The SN75LBC172 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC172 is characterized over the industrial temperature range of –40°C to 85°C.

**N PACKAGE  
(TOP VIEW)**



**DW PACKAGE  
(TOP VIEW)**



NC – No internal connection

**FUNCTION TABLE  
(each driver)**

INPUT A	ENABLES		OUTPUTS	
	G	Ḡ	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level,  
X = irrelevant, Z = high impedance (off)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

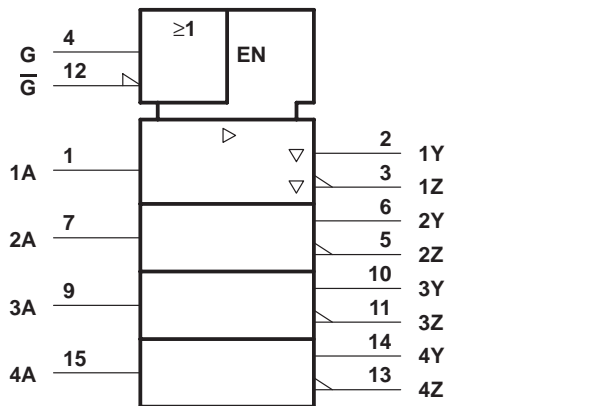
Copyright © 2001–2006, Texas Instruments Incorporated

# SN65LBC172, SN75LBC172

## QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

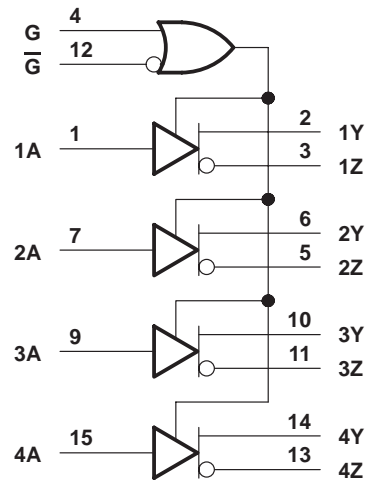
SLLS163E – JULY 1993 – REVISED APRIL 2006

### logic symbol†

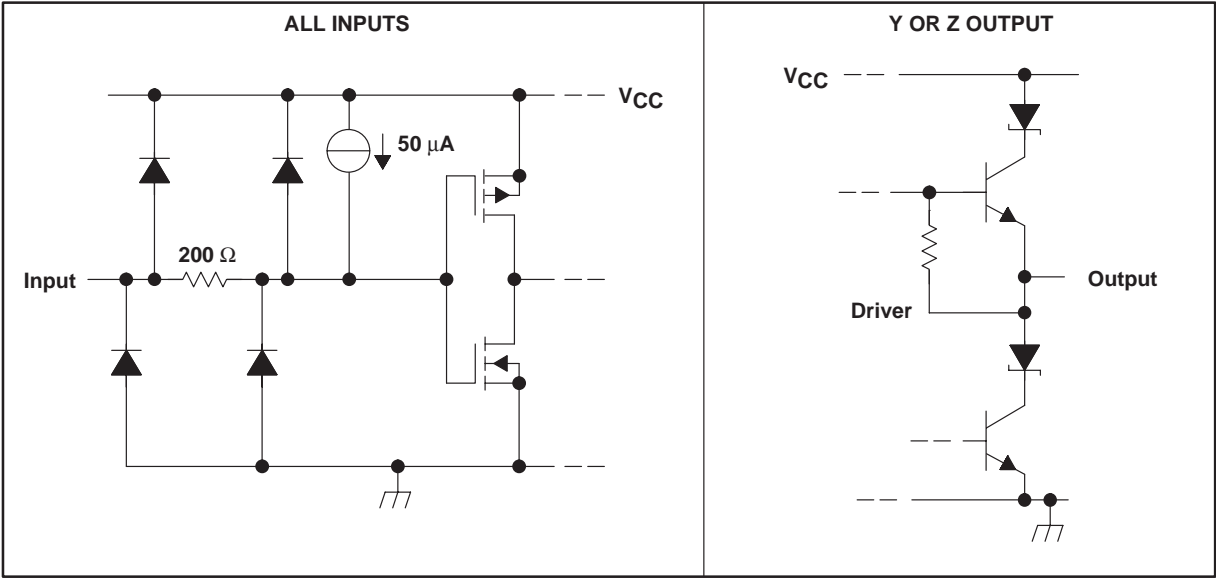


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the N package.

### logic diagram (positive logic)



### schematic diagrams of inputs and outputs



# SN65LBC172, SN75LBC172 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

SLLS163E – JULY 1993 – REVISED APRIL 2006

## absolute maximum ratings†

Supply voltage range, $V_{CC}$ (see Note 1)	–0.3 V to 7 V
Output voltage range, $V_O$	–10 V to 15 V
Voltage range at A, $\overline{G}$ , G	–0.3 V to $V_{CC} + 0.5$ V
Continuous power dissipation	Internally limited‡
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

NOTE 1: All voltage values are with respect to GND.

## recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
High-level input voltage, $V_{IH}$		2			V
Low-level input voltage, $V_{IL}$				0.8	V
Voltage at any bus terminal (separately or common mode), $V_O$	Y or Z			12	V
				–7	V
High-level output current, $I_{OH}$	Y or Z			–60	mA
Low-level output current, $I_{OL}$	Y or Z			60	mA
Continuous total power dissipation		See Dissipation Rating Table			
Junction temperature, $T_J$				140	°C
Operating free-air temperature, $T_A$	SN65LBC172	–40		85	°C
	SN75LBC172	0		70	°C

DISSIPATION RATING TABLE

PACKAGE	THERMAL MODEL	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DW	Low $K^\dagger$	1094 mW	10.4 mW/°C	625 mW	469 mW
	High $K^\ddagger$	1669 mW	15.9 mW/°C	954 mW	715 mW
N		1150 mW	9.2 mW/°C	736 mW	598 mW

† In accordance with the low effective thermal conductivity metric definitions of EIA/JESD 51–3.

‡ In accordance with the high effective thermal conductivity metric definitions of EIA/JESD 51–7.



# SN65LBC172, SN75LBC172

## QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

SLLS163E – JULY 1993 – REVISED APRIL 2006

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	Input clamp voltage	I <sub>I</sub> = −18 mA				−1.5	V
V <sub>OD</sub>	Differential output voltage‡	R <sub>L</sub> = 54 Ω, See Figure 1	SN65LBC172	1.1	1.8	5	V
			SN75LBC172	1.5	1.8	5	
		R <sub>L</sub> = 60 Ω, See Figure 2	SN65LBC172	1.1	1.7	5	
			SN75LBC172	1.5	1.7	5	
Δ V <sub>OD</sub>	Change in magnitude of common-mode output voltage§	R <sub>L</sub> = 54 Ω,      See Figure 1		±0.2			V
V <sub>OC</sub>	Common-mode output voltage			3 −1			V
Δ V <sub>OC</sub>	Change in magnitude of common-mode output voltage§			±0.2			V
I <sub>O</sub>	Output current with power off	V <sub>CC</sub> = 0,      V <sub>O</sub> = −7 V to 12 V		±100			μA
I <sub>OZ</sub>	High-impedance-state output current	V <sub>O</sub> = −7 V to 12 V		±100			μA
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = 2.4 V		−100			μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = 0.4 V		−100			μA
I <sub>OS</sub>	Short-circuit output current	V <sub>O</sub> = −7 V to 12 V		±250			mA
I <sub>CC</sub>	Supply current (all drivers)	No load	Outputs enabled	7			mA
			Outputs disabled	1.5			

† All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

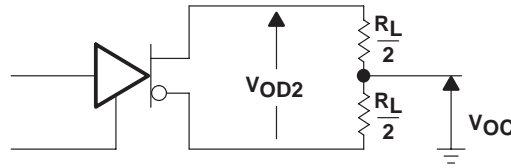
‡ The minimum  $V_{OD}$  specification does not fully comply with EIA-485 at operating temperatures below  $0^\circ\text{C}$ . The lower output signal should be used to determine the maximum signal-transmission distance.

§  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input changes from a high level to a low level.

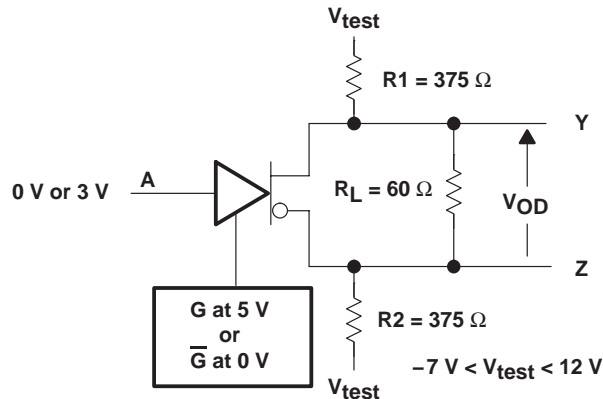
### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$ Differential output delay time	$R_L = 54 \Omega$ , See Figure 3	2	11	20	ns
$t_{t(OD)}$ Differential output transition time		10	15	25	
$t_{PZH}$ Output enable time to high level	$R_L = 110 \Omega$ , See Figure 4		20	30	ns
$t_{PZL}$ Output enable time to low level	$R_L = 110 \Omega$ , See Figure 5		21	30	ns
$t_{PHZ}$ Output disable time from high level	$R_L = 110 \Omega$ , See Figure 4		48	70	ns
$t_{PLZ}$ Output disable time from low level	$R_L = 110 \Omega$ , See Figure 5		21	30	ns

### PARAMETER MEASUREMENT INFORMATION

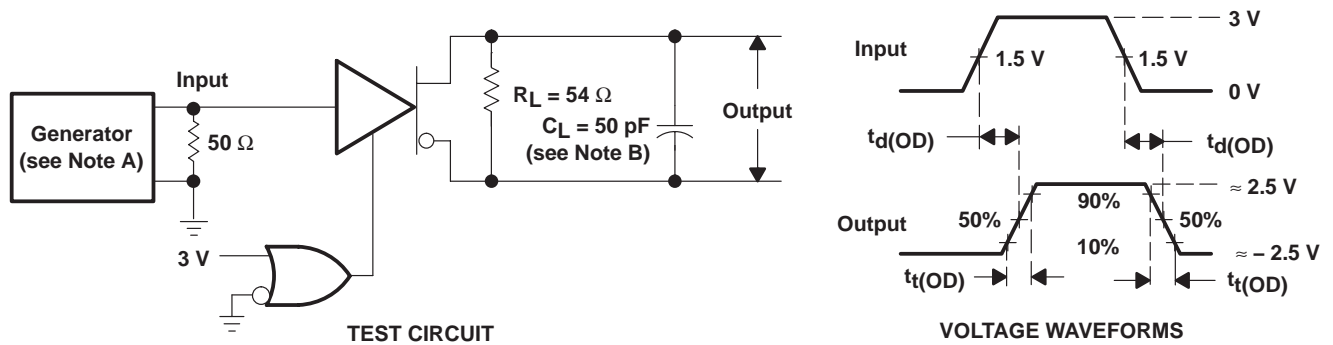


**Figure 1. Differential and Common-Mode Output Voltages**



NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , duty cycle = 50%,  $t_r \leq 5 \text{ ns}$ ,  $t_f \leq 5 \text{ ns}$ ,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and stray capacitance.

**Figure 2. Driver  $V_{OD}$  Test Circuit**



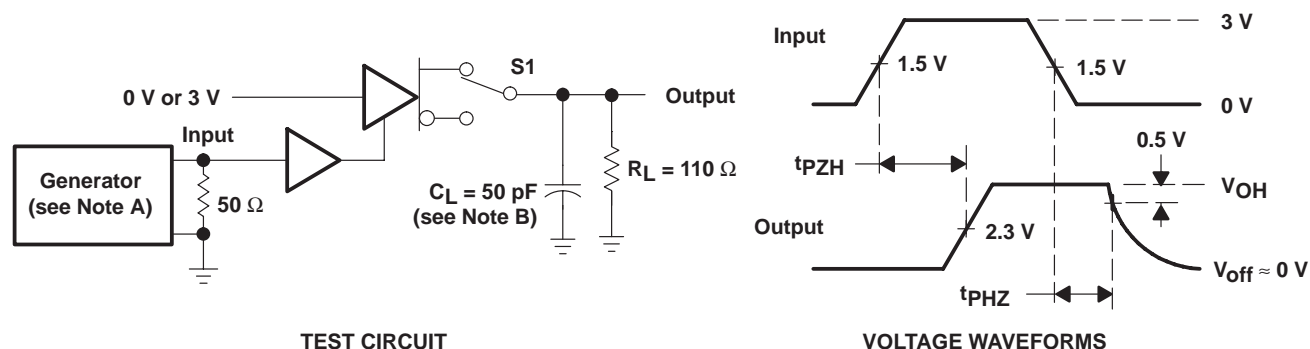
NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , duty cycle = 50%,  $t_r \leq 5 \text{ ns}$ ,  $t_f \leq 5 \text{ ns}$ ,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and stray capacitance.

**Figure 3. Driver Differential-Output Test Circuit and Delay and Transition-Time Waveforms**

# SN65LBC172, SN75LBC172 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

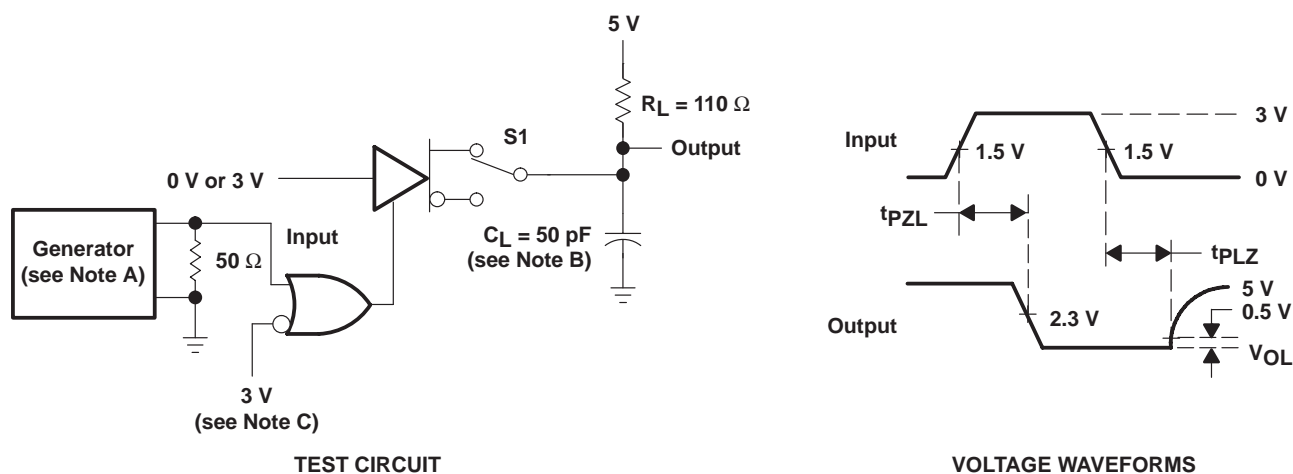
SLLS163E – JULY 1993 – REVISED APRIL 2006

## PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , duty cycle = 50%,  $t_r \leq 5 \text{ ns}$ ,  $t_f \leq 5 \text{ ns}$ ,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and stray capacitance.

Figure 4.  $t_{pZH}$  and  $t_{pHZ}$  Test Circuit and Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , duty cycle = 50%,  $t_r \leq 5 \text{ ns}$ ,  $t_f \leq 5 \text{ ns}$ ,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and stray capacitance.  
C. To test the active-low enable  $\bar{G}$ , ground G and apply an inverted waveform to  $\bar{G}$ .

Figure 5.  $t_{pZL}$  and  $t_{pLZ}$  Test Circuit and Waveforms

# SN65LBC172, SN75LBC172 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

SLLS163E – JULY 1993 – REVISED APRIL 2006

## TYPICAL CHARACTERISTICS

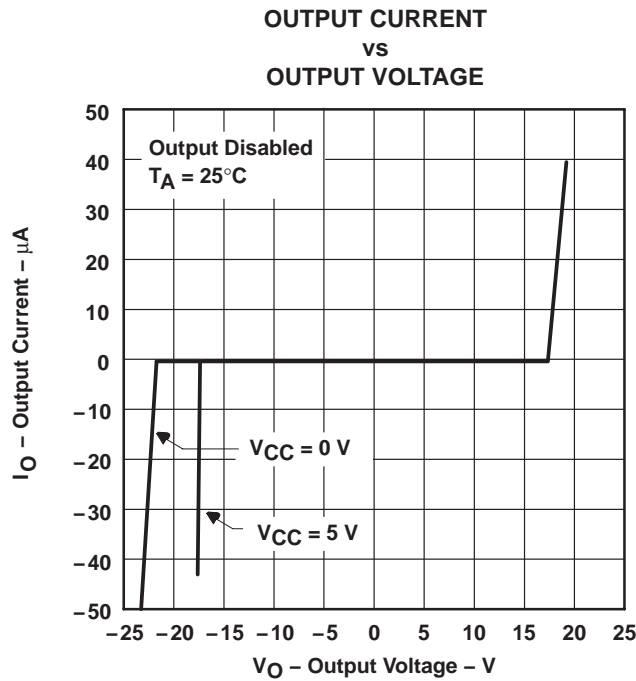


Figure 6

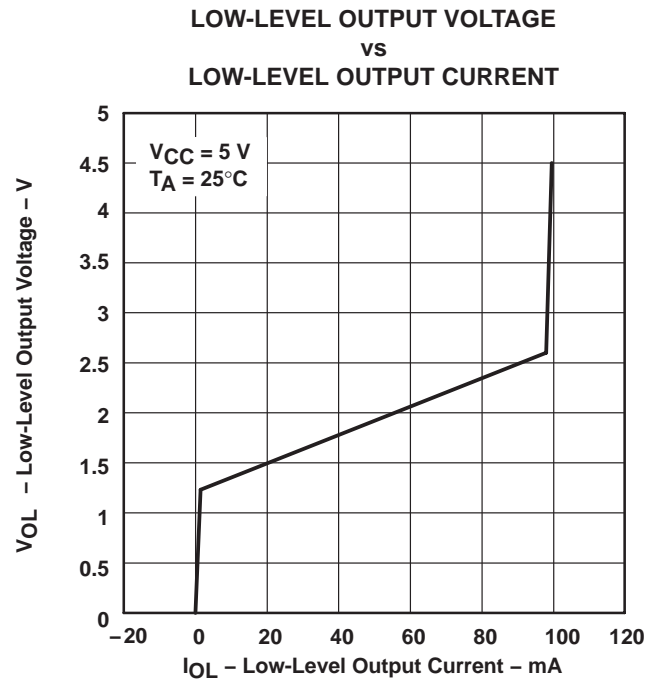


Figure 7

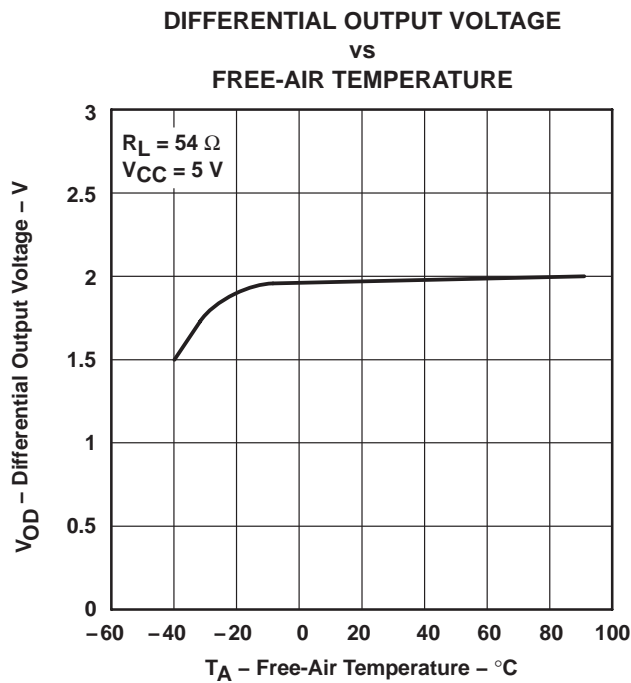


Figure 8

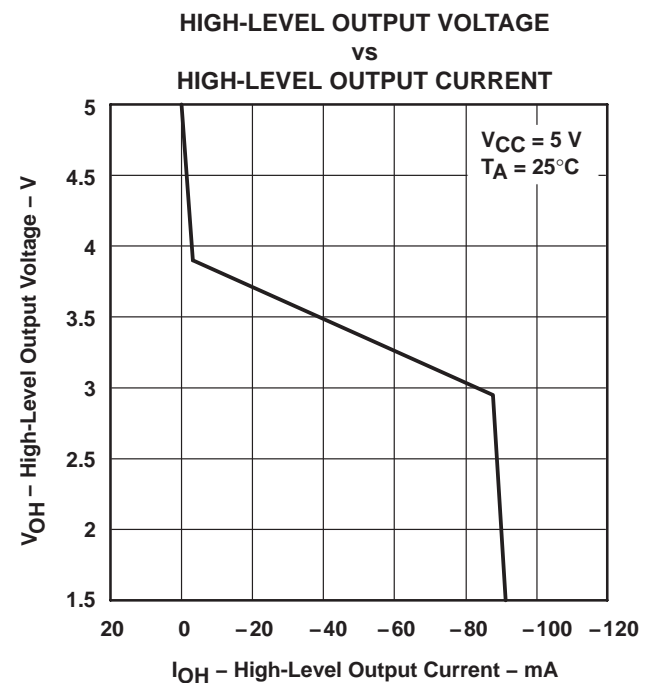


Figure 9

SN65LBC172, SN75LBC172  
QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

SLLS163E – JULY 1993 – REVISED APRIL 2006

TYPICAL CHARACTERISTICS

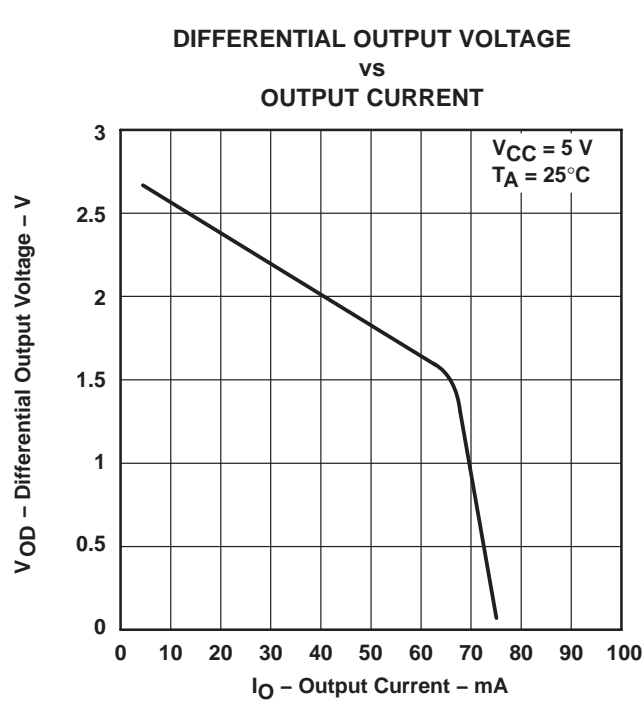


Figure 10

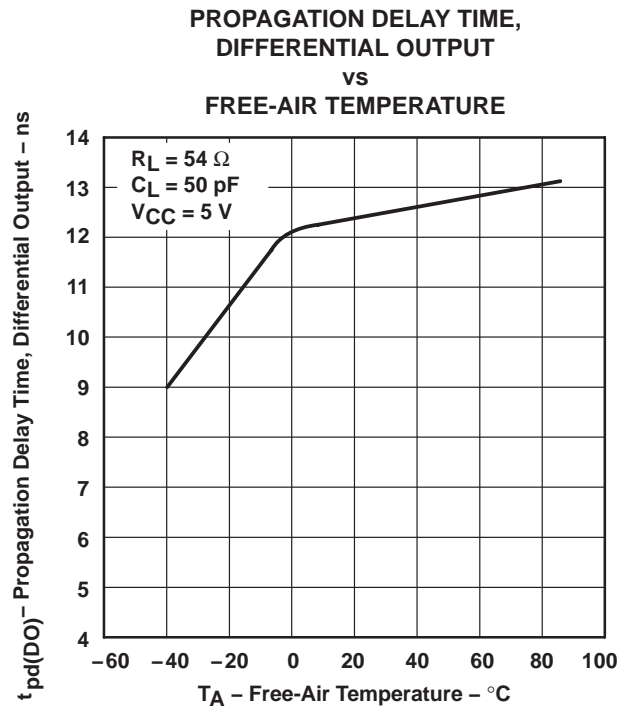


Figure 11

THERMAL CHARACTERISTICS – DW PACKAGE

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Junction-to-ambient thermal resistance, $\theta_{JA}$ <sup>†</sup>	Low-K board, no air flow		96		°C/W
	High-K board, no air flow		62.9		
Junction-to-board thermal resistance, $\theta_{JB}$	High-K board, no air flow		39.6		
Junction-to-case thermal resistance, $\theta_{JC}$			29.1		
Average power dissipation, $P_{(AVG)}$	All four channels maximum loading, maximum signaling rate, $R_L = 54\ \Omega$ , input to D is 10 Mbps 50% duty cycle square wave, $V_{CC} = 5.25\text{ V}$ , $T_J = 130^\circ\text{C}$ .			1100	mW
Ambient free-air temperature, $T_A$	JEDEC high-K board model	-40		85	°C
	JEDEC high-K board model	-40		64	
Thermal shutdown junction temperature, $T_{SD}$			165		

<sup>†</sup> See TI application note literature number SZZA003, Package Thermal Characterization Methodologies, for an explanation of this parameter.



## THERMAL CHARACTERISTICS OF IC PACKAGES

$\Theta_{JA}$  (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

$\Theta_{JA}$  is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

$\Theta_{JA}$  can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures.  $\Theta_{JA}$  is often misused when it is used to calculate junction temperatures for other installations.

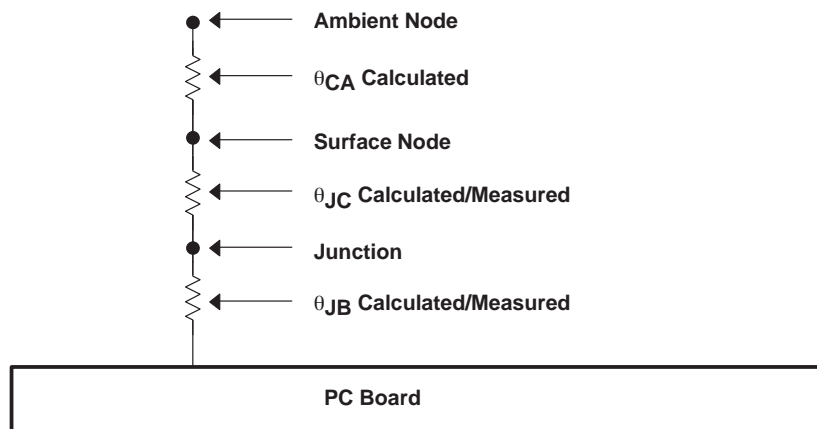
TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives *best case* in-use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in  $\Theta_{JA}$  can be measured between these two test cards

$\Theta_{JC}$  (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

$\Theta_{JC}$  is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with  $\Theta_{JB}$  in 1-dimensional thermal simulation of a package system.

$\Theta_{JB}$  (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure.  $\Theta_{JB}$  is only defined for the high-k test card.

$\Theta_{JB}$  provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see Figure 12).



**Figure 12. Thermal Resistance**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN65LBC172DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LBC172DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LBC172N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type	
SN65LBC172NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type	
SN75LBC172DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75LBC172DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75LBC172DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75LBC172DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75LBC172N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type	
SN75LBC172NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN75LBC172 :**

- Military: [SN55LBC172](#)

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LBC172DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN75LBC172DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LBC172DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75LBC172DWR	SOIC	DW	20	2000	367.0	367.0	45.0

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

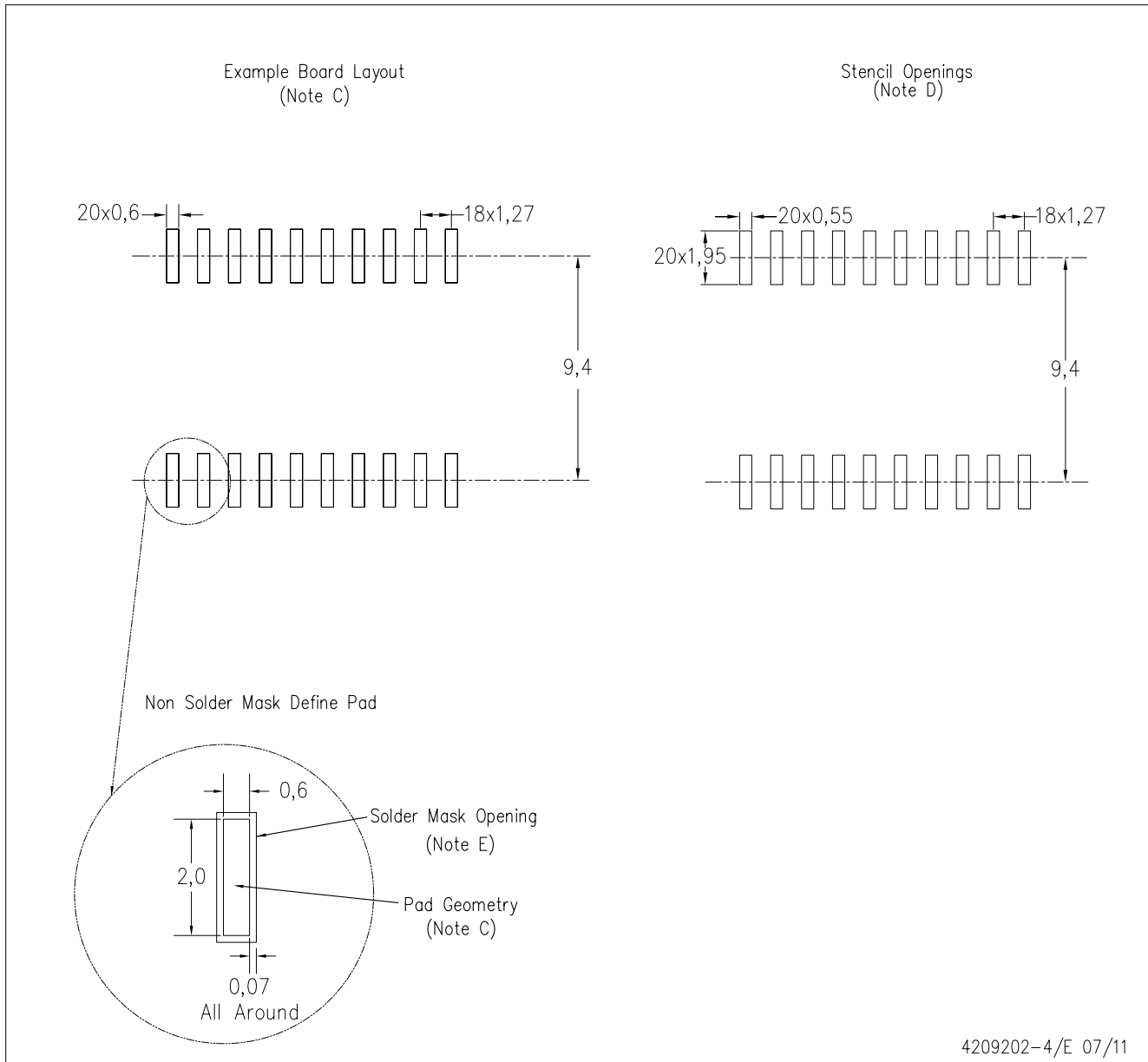
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)

# AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit [www.ameya360.com](http://www.ameya360.com)

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd  
Minhang District, Shanghai , China

➤ Sales :

Direct     +86 (21) 6401-6692  
  
Email       amall@ameya360.com  
  
QQ         800077892  
  
Skype      ameyasales1 ameyasales2

➤ Customer Service :

Email       service@ameya360.com

➤ Partnership :

Tel         +86 (21) 64016692-8333  
  
Email      mkt@ameya360.com