

FDMS7670

N-Channel PowerTrench® MOSFET

30 V, 3.8 mΩ

Features

- Max $r_{DS(on)}$ = 3.8 mΩ at $V_{GS} = 10$ V, $I_D = 21$ A
- Max $r_{DS(on)}$ = 5.0 mΩ at $V_{GS} = 4.5$ V, $I_D = 17$ A
- Advanced Package and Silicon design for low $r_{DS(on)}$ and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery. Provides Schottky-like performance with minimum EMI in sync buck converter applications
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

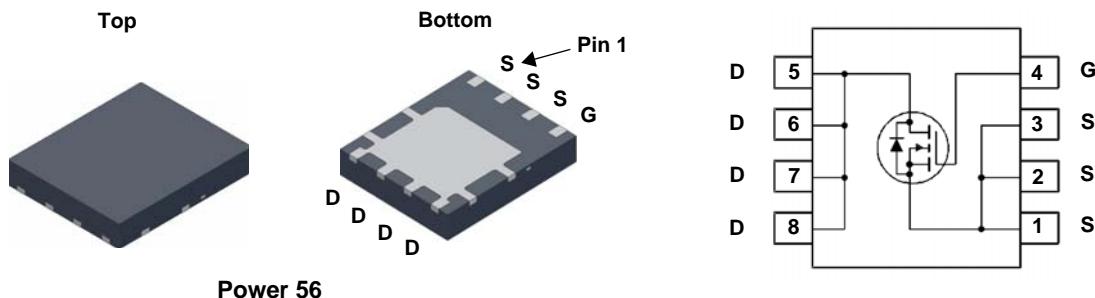


General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Applications

- IMVP Vcore Switching for Notebook
- VRM Vcore Switching for Desktop and Server
- O-ringFET / Load Switch
- DC-DC Conversion



Power 56

MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25$ °C	42	A
	-Continuous (Silicon limited) $T_C = 25$ °C	105	
	-Continuous $T_A = 25$ °C (Note 1a)	21	
	-Pulsed	150	
E_{AS}	Single Pulse Avalanche Energy	144	mJ
P_D	Power Dissipation $T_C = 25$ °C	62	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

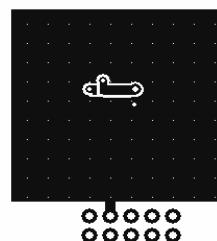
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7670	FDMS7670	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

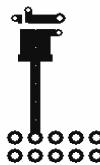
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	30			V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		15		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1.25	1.9	3.0	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		-7		$\text{mV}/^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 21 \text{ A}$		2.9	3.8	
		$V_{GS} = 4.5 \text{ V}, I_D = 17 \text{ A}$		4.1	5.0	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}, I_D = 21 \text{ A}, T_J = 125^\circ\text{C}$		4.0	5.3	
g_{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D = 21 \text{ A}$		136		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		3085	4105	pF
C_{oss}	Output Capacitance			990	1315	pF
C_{rss}	Reverse Transfer Capacitance			75	115	pF
R_g	Gate Resistance			1.2	2.5	Ω
Switching Characteristics						
$t_{d(\text{on})}$	Turn-On Delay Time	$V_{DD} = 15 \text{ V}, I_D = 21 \text{ A}, V_{GS} = 10 \text{ V}, R_{\text{GEN}} = 6 \Omega$		15	26	ns
t_r	Rise Time			6	12	ns
$t_{d(\text{off})}$	Turn-Off Delay Time			31	50	ns
t_f	Fall Time			5	10	ns
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V} \text{ to } 10 \text{ V}$		40	56	nC
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V} \text{ to } 4.5 \text{ V}$	$V_{DD} = 15 \text{ V}, I_D = 21 \text{ A}$	17	24	nC
Q_{gs}	Gate to Source Charge	9.8			nC	
Q_{gd}	Gate to Drain "Miller" Charge	4.4			nC	
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.1 \text{ A}$ (Note 2)		0.7	0.95	
		$V_{GS} = 0 \text{ V}, I_S = 21 \text{ A}$ (Note 2)		0.8	1.1	V
t_{rr}	Reverse Recovery Time	$I_F = 21 \text{ A}, \text{di/dt} = 100 \text{ A}/\mu\text{s}$		38	61	ns
Q_{rr}	Reverse Recovery Charge			19	34	nC
t_a	Reverse Recovery Fall Time			14		ns
t_b	Reverse Recovery Rise Time			24		ns
S	Softness (t_b/t_a)			1.7		
t_{rr}	Reverse Recovery Time	$I_F = 21 \text{ A}, \text{di/dt} = 300 \text{ A}/\mu\text{s}$		32	51	ns
Q_{rr}	Reverse Recovery Charge			34	54	nC

Notes:

1. R_{QJA} is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5×1.5 in. board of FR-4 material. R_{QJC} is guaranteed by design while R_{QCA} is determined by the user's board design.



a. $50^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper.



b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width $< 300 \mu\text{s}$, Duty cycle $< 2.0\%$.

3. E_{AS} of 144 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 1 \text{ mH}$, $I_{\text{AS}} = 17 \text{ A}$, $V_{DD} = 27 \text{ V}$, $V_{GS} = 10 \text{ V}$. 100% test at $L = 0.3 \text{ mH}$, $I_{\text{AS}} = 22 \text{ A}$.

4. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

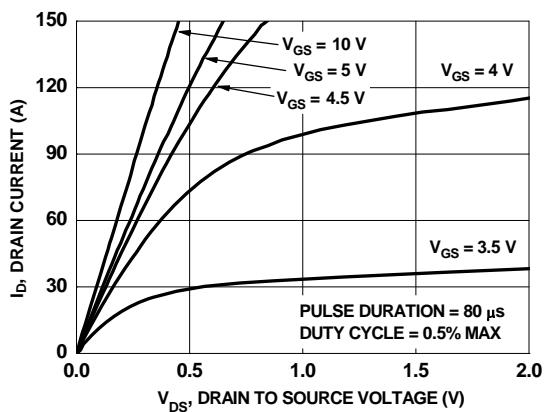


Figure 1. On Region Characteristics

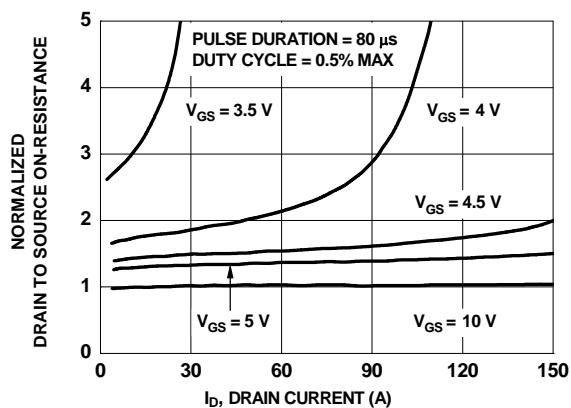


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

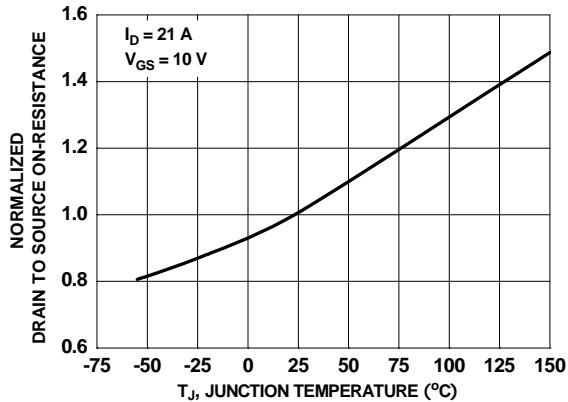


Figure 3. Normalized On Resistance vs Junction Temperature

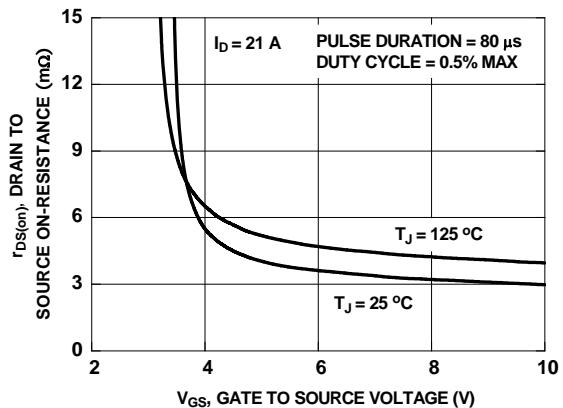


Figure 4. On-Resistance vs Gate to Source Voltage

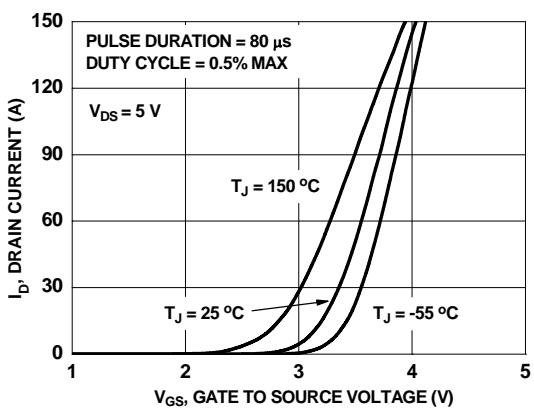


Figure 5. Transfer Characteristics

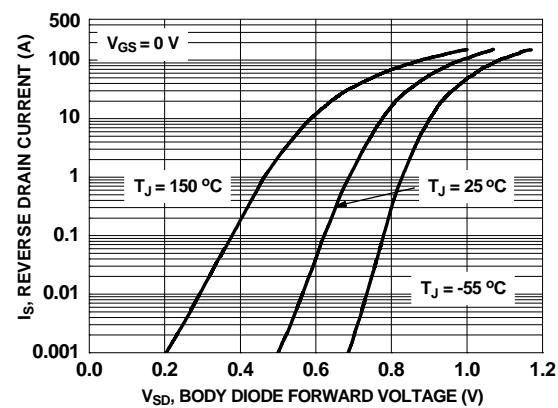


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

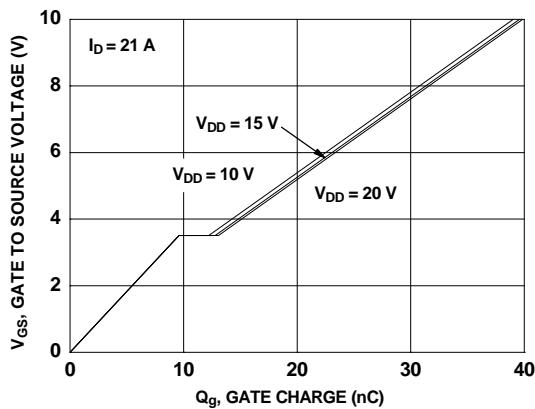


Figure 7. Gate Charge Characteristics

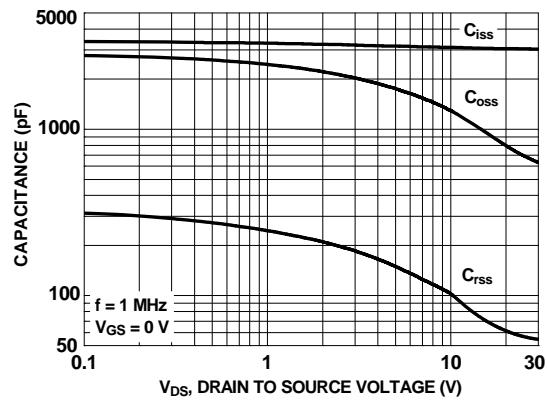


Figure 8. Capacitance vs Drain to Source Voltage

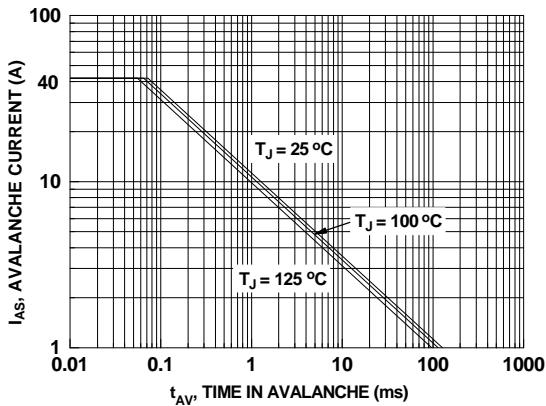


Figure 9. Unclamped Inductive Switching Capability

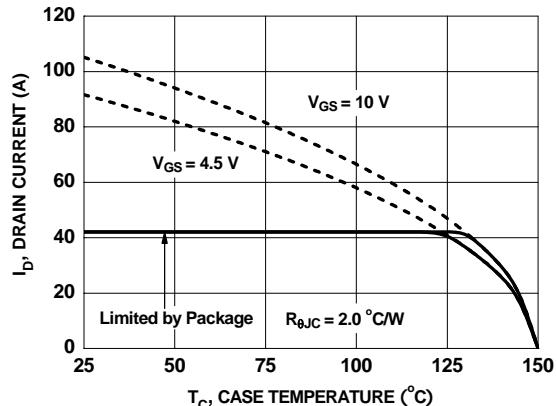


Figure 10. Maximum Continuous Drain Current vs Case Temperature

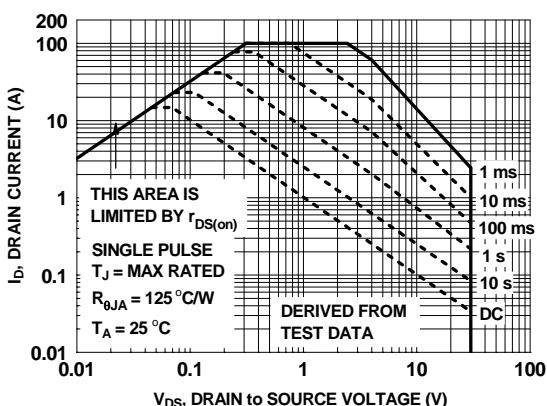


Figure 11. Forward Bias Safe Operating Area

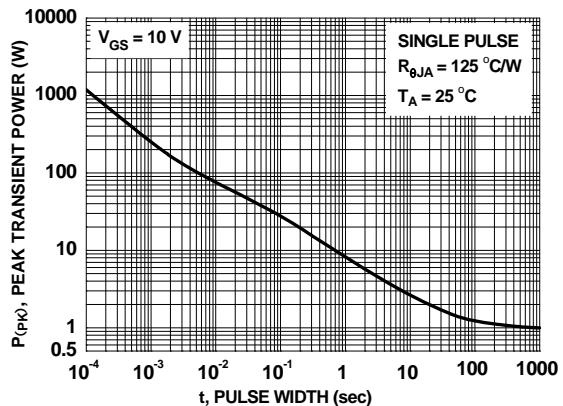


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

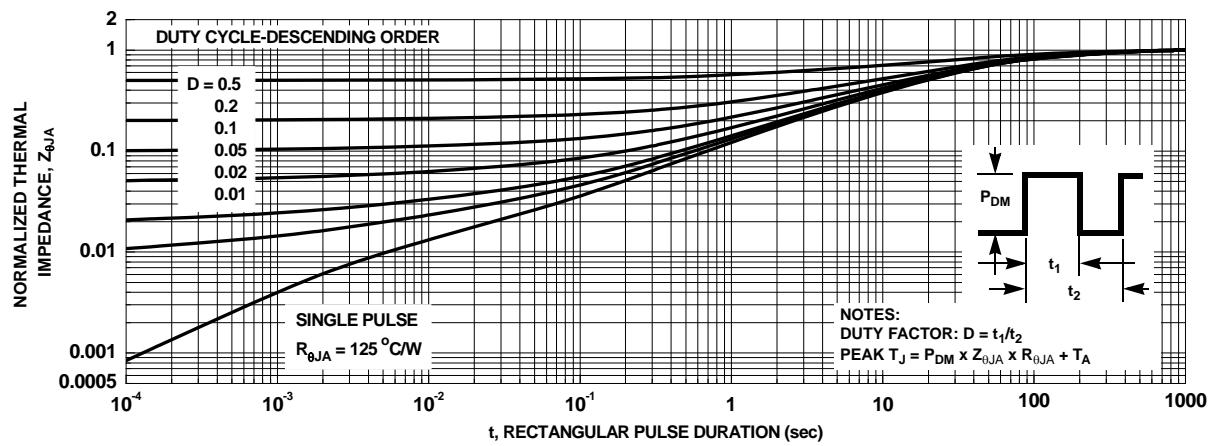


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

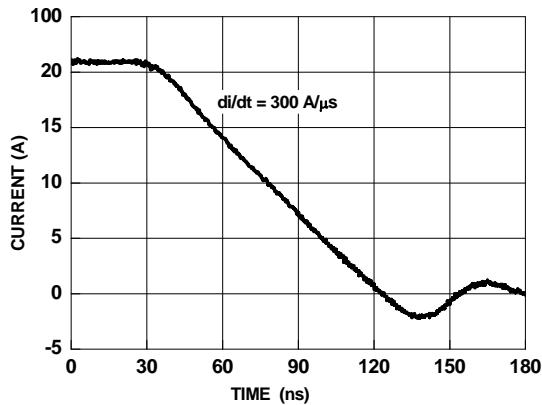
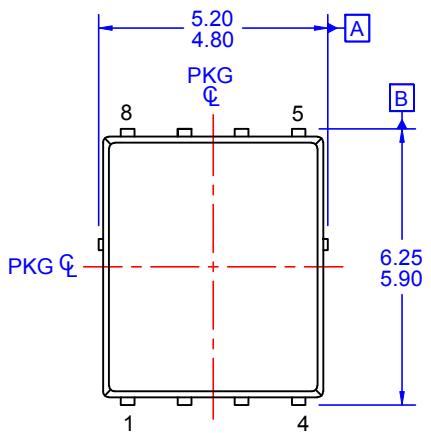
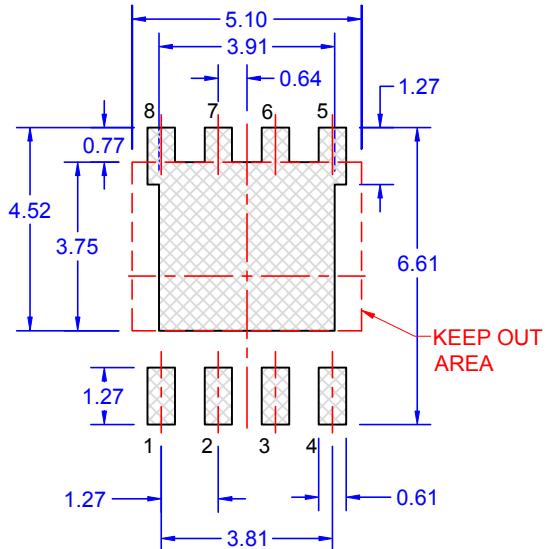
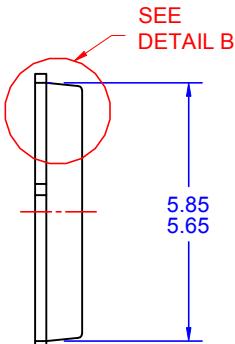


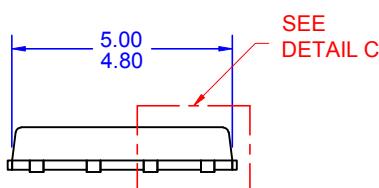
Figure 14. Body Diode Reverse Recovery Characteristics



TOP VIEW

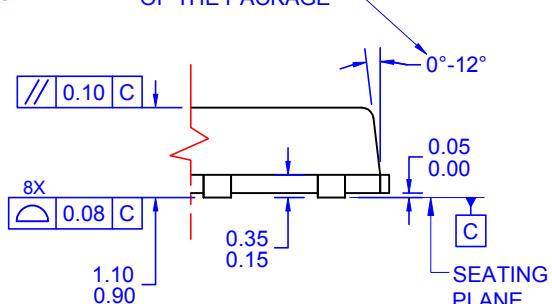


LAND PATTERN RECOMMENDATION



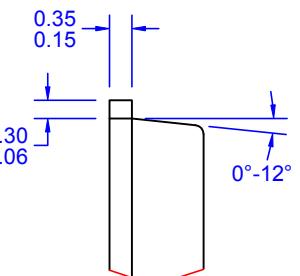
SIDE VIEW

OPTIONAL DRAFT
ANGLE MAY APPEAR
ON FOUR SIDES
OF THE PACKAGE



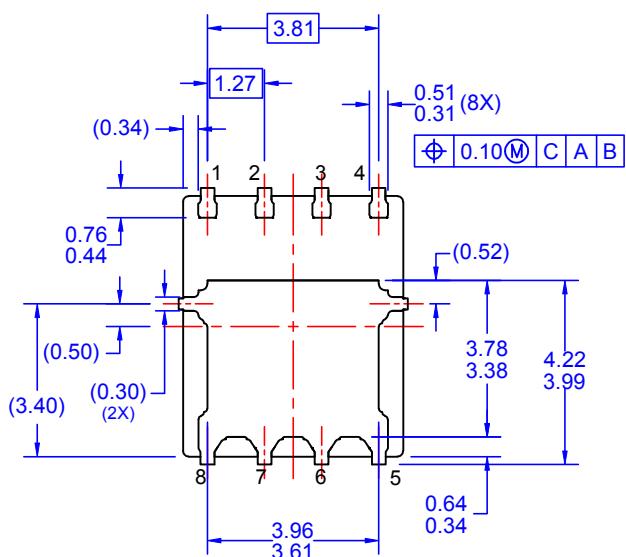
DETAIL C

SCALE 2:1



DETAIL B

SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F. DRAWING FILE NAME: PQFN08AREV8



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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I73

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