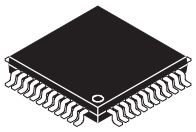
1 Introduction

1.1 Features

- **Optimized for CDMA2000-1X and UMTS**
- **Up to 12 UMTS or 24 CDMA2000 Upconverter Channels**
- **Mixed CDMA2000-1X and UMTS Operation**
- **DUC Output Rates to 125 MSPS**
- **Any DUC Can Sum into Any of Four Output Ports**
- **Real/Complex DUC Outputs**
- **Tx Filtering: 6-Stage CIC, 47-Tap CFIR, 63-Tap PFIR**
- **115-dB SFDR**
- **18-Bit DUC Outputs**
- **1.5-V Core, 3.3-V I/O**



1.1.1 Description

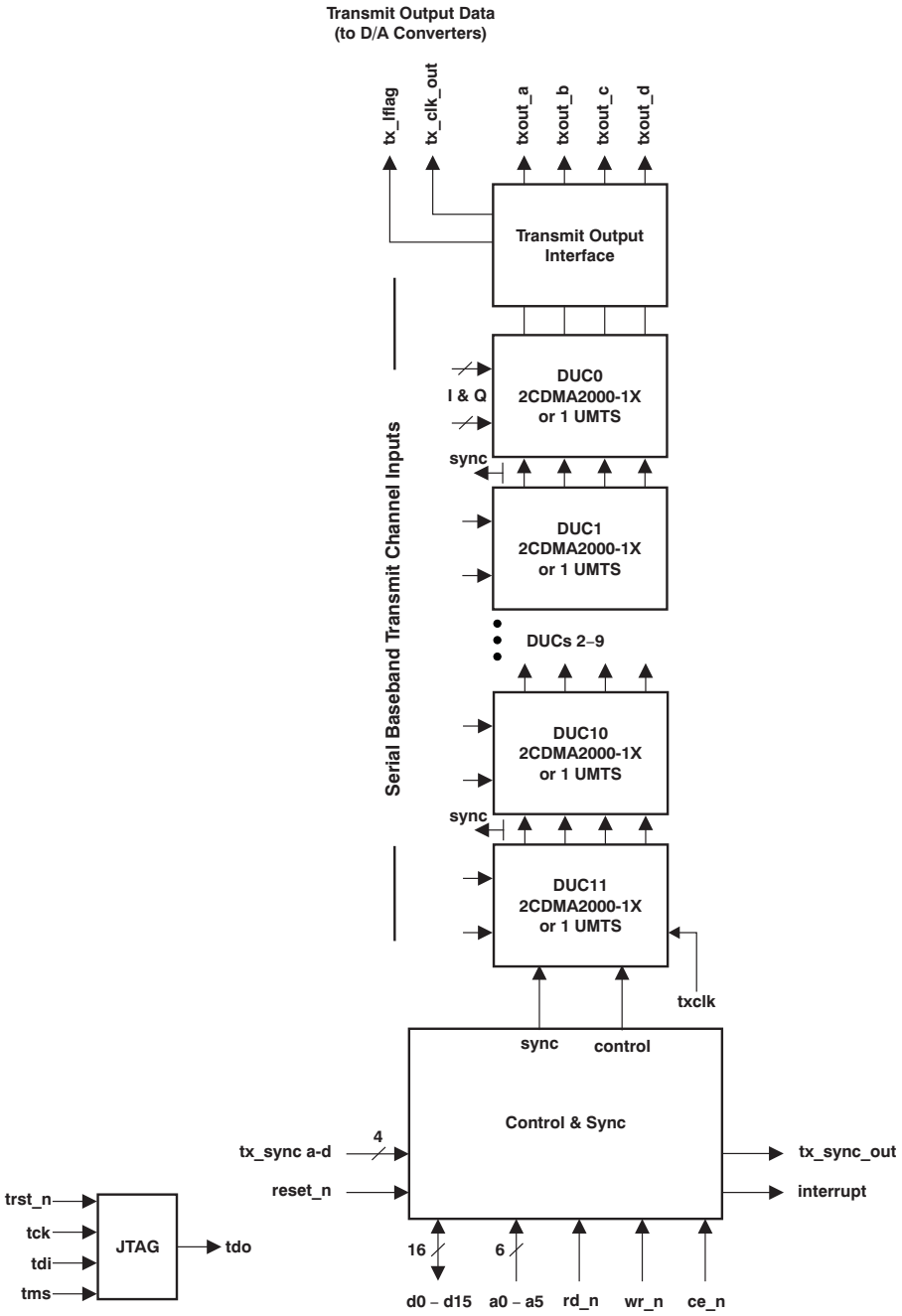
The GC5318 is a high-density multi-channel communications signal processor integrated circuit that provides digital upconversion optimized for cellular base transceiver systems. The device supports both UMTS and CDMA2000 (CDMA) air interface cellular standards.

The chip provides up to 24 CDMA digital upconverter (DUC) channels or 12 UMTS DUC channels. The GC5318 can also support a combination of CDMA and UMTS channels. The DUC channels operate simultaneously.

The chip is ideal for cellular base transceiver systems where a large number of digital radio channels are required. Each of the 24 CDMA (or 12 UMTS) channels can operate independently.

There are four 18-bit output ports. Each output port can sum any of the DUC channels in a daisy-chain fashion. This configuration permits creating a stack of CDMA or UMTS signals. These ports can output either real or complex data. Real output data would generally drive one or more digital-to-analog (D/A) converters and output the stack of signals at an intermediate frequency (IF). Complex data (at baseband or an IF) is used when a quadrature modulator upconversion scheme is employed. Complex output data can also be used when the output stack is further processed using crest factor reduction or power amplifier predistortion techniques.

1.1.2 Functional Block Diagram



1.1.3 Package/Ordering Information

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
GC5318	Thermally-Enhanced Plastic BGA with Heat Slug – 388	ZED	–40°C to +85°C	GC5318IZED	GC5318IZED	Tray, 40

Contents

2 GC5318 Operation

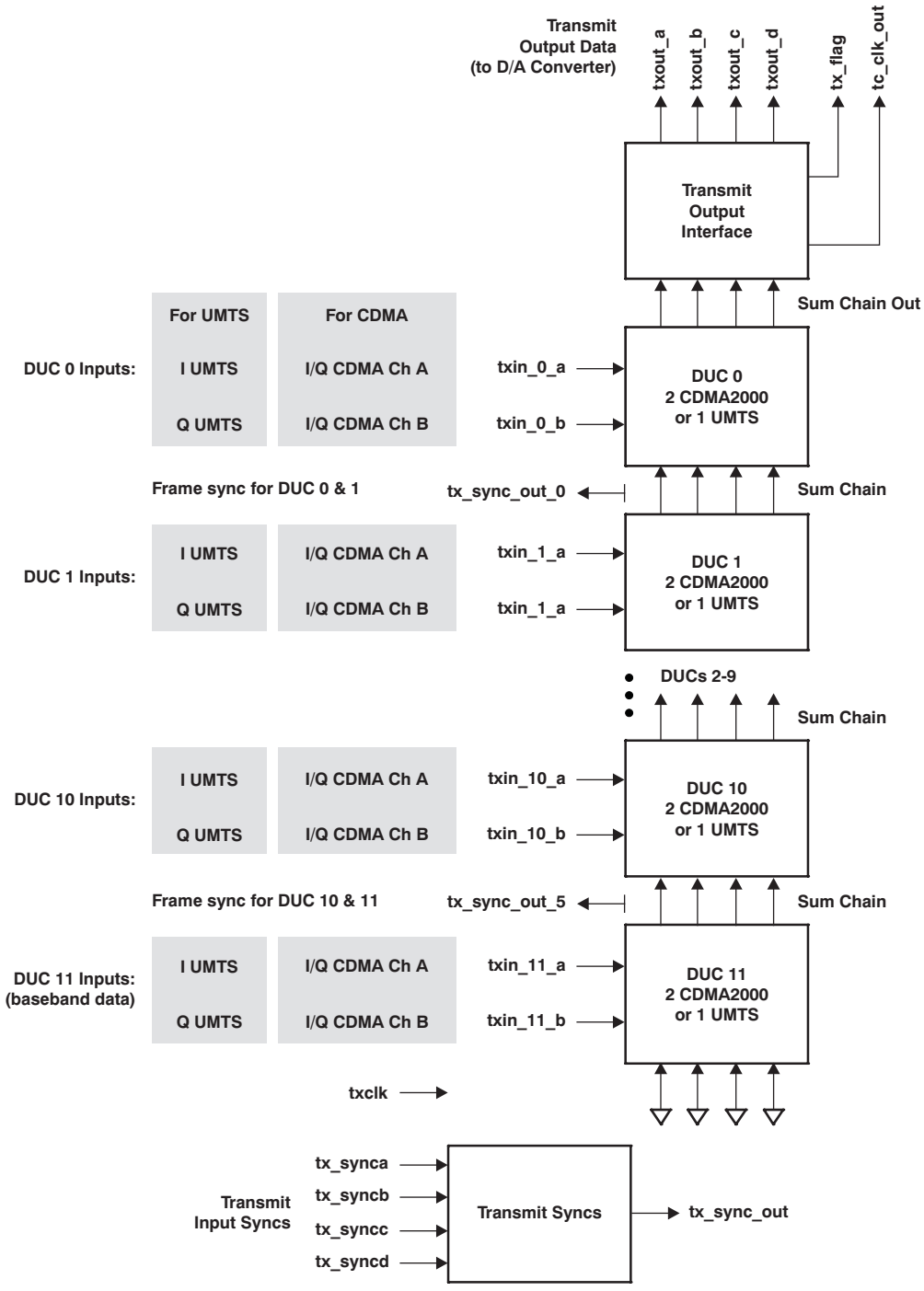


Figure 2-1. GC5318 Block Diagram

The GC5318 provides up to 24 CDMA2000 or 12 UMTS digital upconversion (DUC) channels. There are 12 DUC blocks, DUC 0 through DUC 11, as shown in the block diagram of Figure 2-1. Each block can be configured as a single UMTS channel or as two CDMA channels.

The outputs of all DUCs drive four independent complex sum chains. Any DUC can contribute (or not) to any or all of the four sum chains. The output of a DUC block sum chain drives the sum chain input of the next block. The first DUC to output data is DUC0, while the last is DUC11. The two or four outputs of a DUC are the sum of all the contributing channels of all the higher numbered DUC blocks and itself. The sum chain inputs of DUC 11 are grounded. Within the chain, all DUC blocks from 0 up to the highest numbered DUC in use must be turned on; otherwise, the sum chain is broken.

The transmit output interface takes the four summed chains of DUC output data from the output of DUC 0, then scales and rounds them to a user-programmed number of bits. Composite power meters with programmable integration periods and intervals compute the power in each of the four output streams. The data is then formatted for output over the four tx_data_out ports.

2.1 Digital Upconvert Block (DUC)

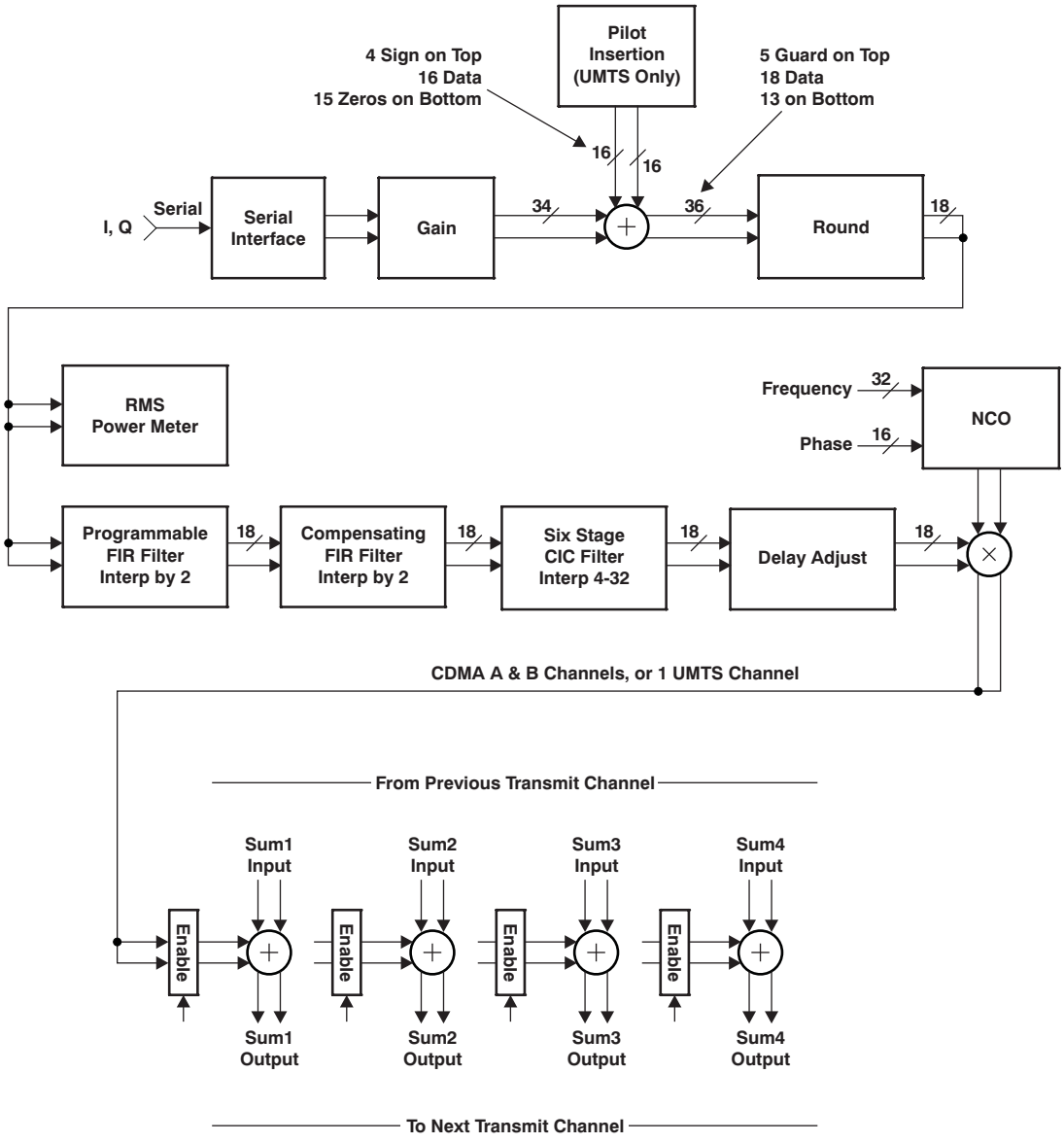


Figure 2-2. Digital Upconvert Block

This section describes the functions available in each of the 12 DUC blocks. Each block has its own register set and may be programmed individually. The final output rates of all DUC blocks must match since they are added together.

Figure 2-2 illustrates the different signal processing blocks and general signal processing flow of an individual transmit channel. Within a block, a single set of hardware performs these functions for one UMTS signal or two CDMA signals. When processing two CDMA signals, the gain, round, power meter, PFIR and CFIR blocks are time-shared to process both signals with one set of hardware. Each DUC can support one UMTS channel or two CDMA channels.

Each block accepts baseband serial data. At this point, the gain can be adjusted and a pilot sequence can be summed with the data. Baseband data gain adjusted and the pilot signal power can be measured. The programmable FIR filter (PFIR) is used to pulse shape the data and interpolates by a factor of two. The compensating CIC filter (CFIR) compensates for the roll-off of the following CIC filter and also interpolates by a factor of two. The CIC filter performs additional interpolation; this additional interpolation is programmable. The delay adjust block permits the channel's delay to be adjusted relative to all other DUC channels.

The interpolated, filtered, and delayed data is then tuned to a user-programmed frequency with a digital mixer and oscillator. The DUC output data then drives four independent sum chain paths, where output data from each DUC can be summed into four composite streams.

Each function block is described in greater detail in subsequent sections.

Table 2-1. Programming

VARIABLE	DESCRIPTION
cdma_mode	When set, the DUC block is in CDMA2000 mode.

2.1.1 Transmit Serial Input Interface

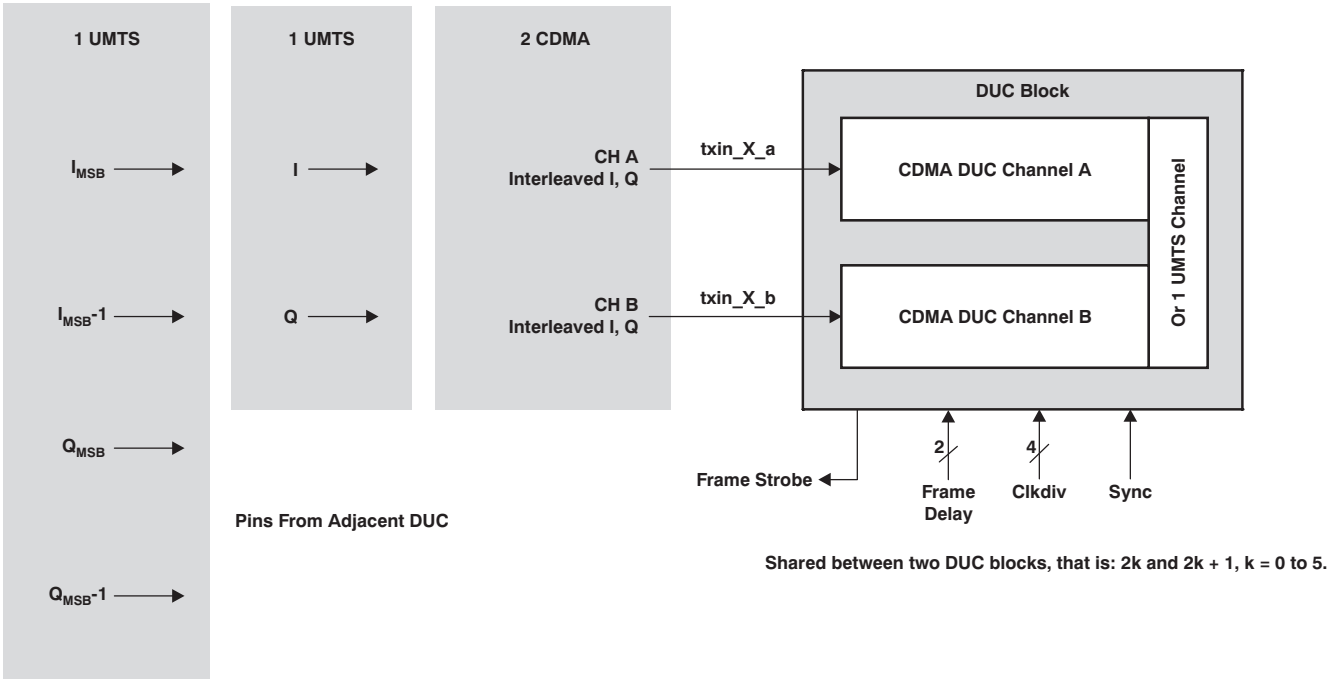


Figure 2-3. Transmit Serial Input Interface

Each DUC block has two serial input data pins; see Figure 2-3. These pins are used to transfer I/Q baseband data into the DUC channel for interpolation, filtering, and tuning to a carrier frequency. The channel configuration of the block determines how these pins are used.

When the block is configured for two CDMA channels, one pin (txin_X_a) accepts serial data for signal A; the other pin (txin_X_b) for signal B. Input I and Q data, programmable up to 18 bits, are multiplexed over the serial input pin starting with the most significant I bit. The maximum input bit rate is txclk. The interface can be programmed to accept up to 32 bits, but only the upper 18 bits will be used as input signal data.

The most significant bit is sent first.

When the block is configured for a single UMTS channel, the txin_a is for I data, and txin_b carries the Q data.

The four-pin mode is less common. It employs another two pins from the adjacent (2k + 1) DUC, sacrificing the use of that DUC ito allow reduced data rate on the serial pins. The I data (Imsb, Imsb-1) are carried on txin _(2k) _a and txin _(2k)_b, while the Q data (Qmsb Qmsb-1) are carried on txin _(2k + 1) _a and txin _(2k + 1) _b.

Each pair of blocks (2k and 2k + 1) shares the clock division, frame delay, sync generation, and a frame strobe output pin.

A programmable clock divider circuit can be used to specify the serial bit rate with respect to txclk. The divider is programmed as txclk / (1+serp_trans_clkdiv). The clock divider circuit is synchronized using a general sync block discussed in another section of this document.

The frame sync interval can be programmed from 1 to 127 bit-periods (which are divided clocks).

The number of bits in a word is set as (serp_tran_bits+1).

The frame strobe is an output from the GC5318 that indicates when the msb is expected. The frame strobe can be programmed to arrive from 0 to 3 bit clocks ahead of when the msb is expected via the serp_tran_fsdel parameter. The source must transmit all of its data before the next frame strobe is generated. Use of the frame strobe is optional. The sync (ssel_serial) parameter determines when the msb is expected.

The parameter chosen must satisfy the following constraints:

- serp_tran_fsinv $\times$ (serp_tran_clkdiv+1) = 4 $\times$ (cic_interp_decim+1)
- serp_tran_fsinv $\geq$ (serp_tran_bits+1)2 for CDMA mode
- serp_tran_fsinv $\geq$ (serp_tran_bits+1) for UMTS mode
- serp_tran_fsinv $\geq$ (serp_tran_bits+1)0.5 for four-pin mode

NOTE

For half-rate data (when serp_tran_clkdiv = 1), the MSB of the input data stream is captured on the fourth rising edge of txclk, after txsync occurs. For full-rate data (when serp_tran_clkdiv = 0), the MSB of the input data stream is captured on the third rising edge of txclk, after txsync occurs.

See Figure 2-4 for a diagram of the serial transmit input timing.

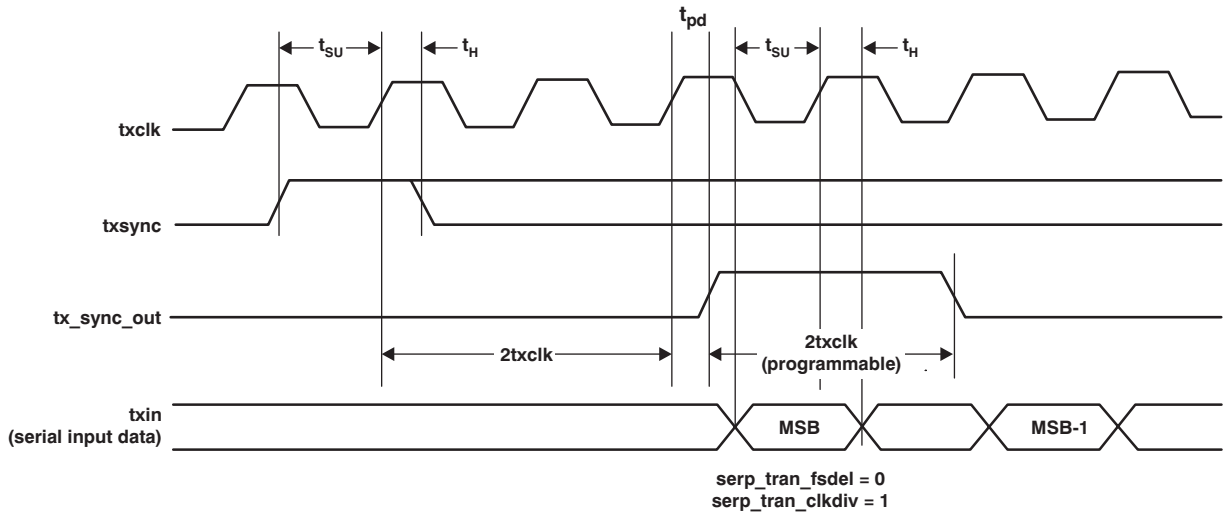


Figure 2-4. Serial Input Timing

Table 2-2. Programming

VARIABLE	DESCRIPTION
serp_tran_bits(4:0)	Number of serial input bits in a word – 1. That is, 10001 = 18 bits
serp_tran_fsinvl(6:0)	Frame sync interval in bits
serp_tran_fsdel(1:0)	The number of serial bits after frame strobe that the data MSB is expected.
serp_tran_4pin	0 = 2 pin input mode. Applies to UMTS mode for separate I and q data bits, as well as CDMA mode where one pin is for interleaved I/Q data for the CDMA A channel and another pin for interleaved I/Q data for the CDMA B channel. 1 = 4 pin mode. Applies to UMTS mode where the channel has two bits for I data (I_{msb} and I_{msb-1}) and two bits for Q data (Q_{msb} and Q_{msb-1})
serp_tran_clkdiv(3:0)	Serial input data bit clock divider factor – 1
ssel_serial(2:0)	Sync source

The parameters are set for a pair of DUC blocks; that is, for 2k and 2k + 1 DUCs, where k = 0 to 5.

2.1.2 Gain

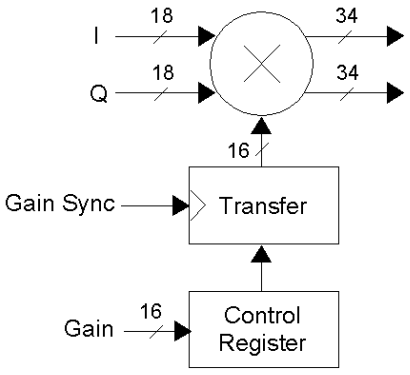


Figure 2-5. Gain Block

The transmit gain block, shown in Figure 2-5, is a multiplier that increases or decreases the level of the input data. The unsigned 16-bit gain word is interpreted with the binary point three bits down from the MSB. It multiplies the input data by (gain word/8192). The maximum gain is therefore 65535/8192. There are different gain registers for the A and B signals in CDMA mode.

A transfer register in combination with a sync (ssel_gain) synchronizes gain changes across multiple channels.

Table 2-3. Programming the Gain

VARIABLE	DESCRIPTION
gainfora(15:0)	Gain for the A-side DUC. Interpreted as gainfora/8192; unsigned.
gainforb(15:0)	Gain for the B-side DUC. Interpreted as gainforb/8192; unsigned.
ssel_gain(2:0)	Sync source

2.1.3 UMTS Pilot Code Insertion

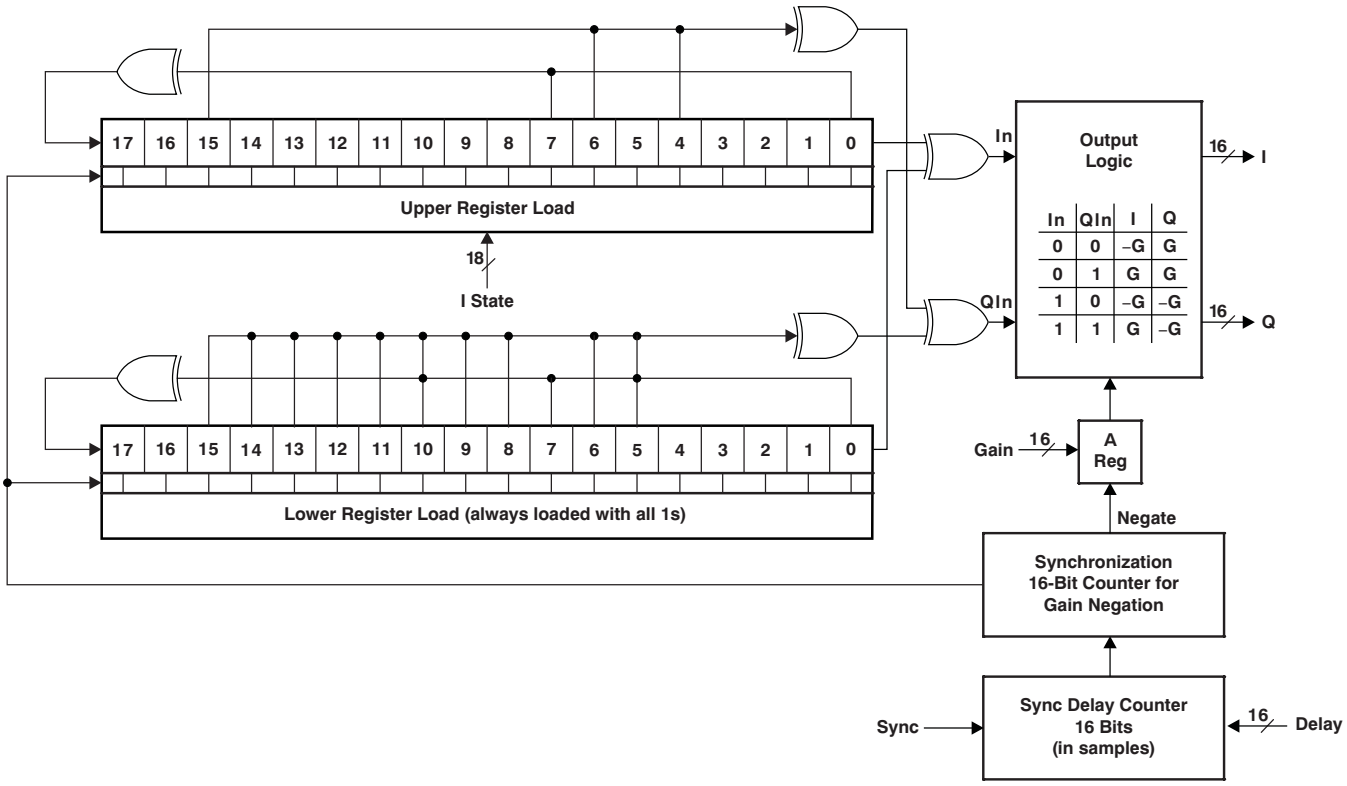


Figure 2-6. Pilot Code Insertion Logic

The pilot code insertion block, shown in Figure 2-6, generates UMTS pilot scrambling sequences and should be disabled by setting gain to zero when transmitting CDMA. The pilot sequence is summed with the UMTS input baseband data prior to PFIR filtering.

The pilot sequence is complex and generated from two 18-bit shift registers, each with a unique set of feedback taps. Specific taps are exclusive-or combined to form the I and Q streams. The streams are then modified by a user-programmed complex gain value. The gain word G is a signed 16-bit value. The output sequence is ±G. Setting gain to zero turns off pilot insertion.

NOTE

Gain MUST be set to zero for CDMA operation.

The upper 18-bit shift register is programmed with a starting sequence based on the desired primary scrambling code (PSC). There are 512 start sequences for all of the base station transceiver (BTS) codes. The lower register always starts with a string of all 1s.

When diversity channels are employed, a counter in the synchronization block toggles the sign of the gain value in a prescribed fashion. The UMTS frame starts with positive gain for 256 chips, then toggles to negative gain for 512 chips, then toggles again to positive gain for 512 chips, and so on until the end of the frame. The last 256 chips of the frame are negative gain. This sequence repeats for subsequent frames.

Table 2-4. Programming

VARIABLE	DESCRIPTION
pilot_psc(15:0)	Lower 16 bits of the 18-bit pilot LFSR initial sequence.
pilot_psc(17:16)	Upper two bits of the 18-bit pilot LFSR initial sequence.
pilot_diversity	Sets main or diversity pilot generation. 0 = main, 1 = diversity
pilot_delay(15:0)	Unsigned delay value (in chips) from sync event. 0 to 38399 chips.
pilot_gain_0(15:0)	Gain value. pilot_gain_0 and pilot_gain_1 must be set to the same value for proper operation. Must be set to 0 for CDMA operation.
pilot_gain_1(15:0)	Gain value. pilot_gain_0 and pilot_gain_1 must be set to the same value for proper operation. Must be set to 0 for CDMA operation.
ssel_pilot(2:0)	Sync source

2.1.4 RMS Power Meter

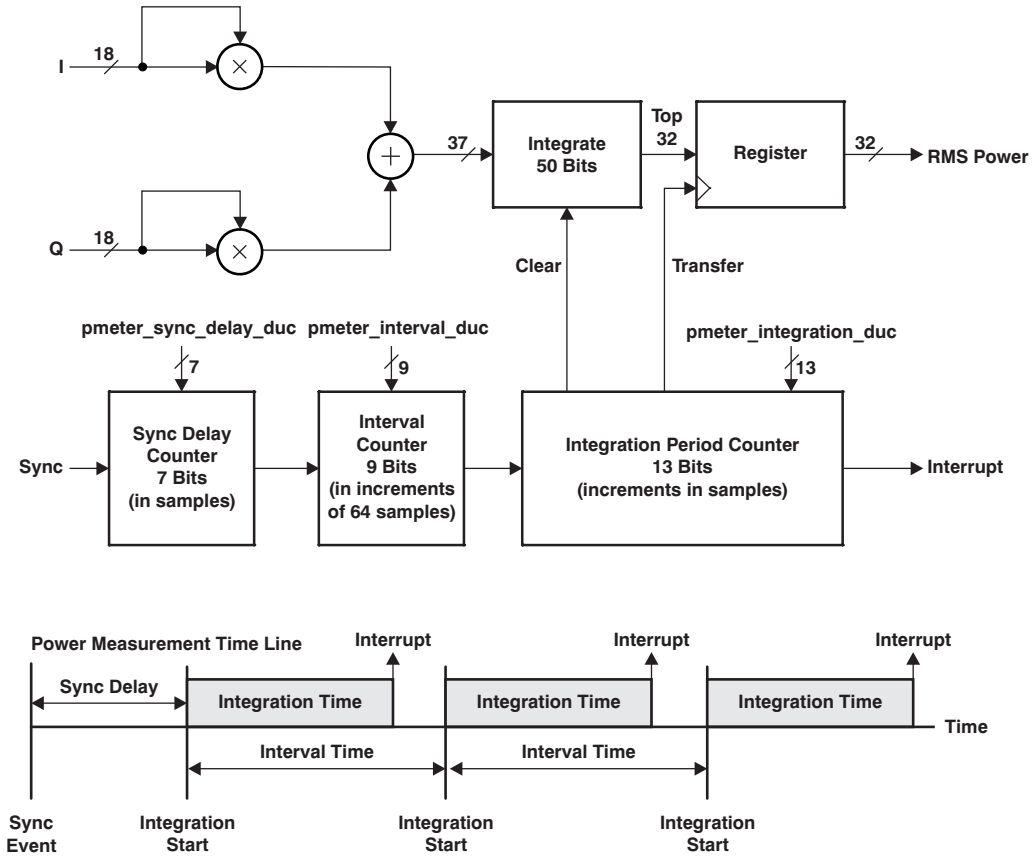


Figure 2-7. RMS Power Meter

Each transmit channel includes an RMS power meter used to measure the RMS power within the channel.

The RMS power meter samples the I and Q data stream before the PFIR filter; see Figure 2-7. Both 18-bit I and Q data are squared, summed, and then integrated over a time determined by pmeter_integration_duc (13 bits). The integration time = 4 x pmeter_integration_duc + 1 (in units of a sample period or generally a chip period).

A programmable 9-bit interval counter sets the interval over which power measurements are repeated. The timer counts in increments of 64 samples. The interval time = 64 (pmeter_interval_duc+1). The interval time must be greater than (not equal to) the integration time.

The power measurement process starts with a sync event (ssel_pmeter). The integration starts at sync event + 3 chips + sync_delay. The 7-bit delay register permits delays from three to 130 samples after sync. The integration continues until the integration count is met. At that point, the top 32 bits of the 50-bit accumulator are transferred to the read register and an interrupt is generated that indicates the power value is ready to read. The interval counter continues until the programmed interval count is reached. When reached, the integration counter and the interval counter start over again. Each time the integration count is reached the upper 32 bits are again transferred to the read register, overwriting the previous value and sending an interrupt signifying the power value can be read. Failure to read the data before the next interrupt signal results in overwriting the previous interval measurement.

Sync ssel_pmeter starts the process. Whenever a sync is received, all counters are reset to zero no matter what the status may be.

For UMTS, I and Q are calculated and the integrated power is read. In CDMA mode the power is calculated for both the A and B signals, producing two 32-bit results.

For CDMA mode, the integration time is slightly longer. The power read in CDMA mode with a dc input is:

- A power: $[I^2 \times (X \times 4 + 1) + Q^2 \times (X \times 4 + 0)] \times 2^{-18}$. ***Note:*** One Q sample is missing from the integration.
- B power: $[I^2 \times (X \times 4 + 1) + Q^2 \times (X \times 4 + 1)] \times 2^{-18}$

where X is the integration count.

Table 2-5. Programming

VARIABLE	DESCRIPTION
pmeter_result_a_lsb(15:0)	Lower 16 bits of the A channel power measurement.
pmeter_result_a_msb (31:16)	Upper 16 bits of the A channel power measurement.
pmeter_result_b_lsb (15:0)	Lower 16 bits of the B channel power measurement result. Only available in CDMA mode.
pmeter_integration_duc(12:0)	Integration time = 4 x pmeter_integration_duc + 1.
pmeter_sync_delay_duc(6:0)	Sync delay count in samples.
pmeter_interval_duc(9:0)	Interval time = 64 (pmeter_interval_duc + 1). Interval time must be greater than (not equal to) integration time.
ssel_pmeter(2:0)	Sync source options.
pmeter_sync_disable	Turns off sync to the channel's power meter

2.1.5 Filter Chain

GC5318 transmit filtering is performed in three stages:

- Interpolate by two pulse-shape filtering using the programmable FIR filter (PFIR)
- Interpolate by two compensation filtering using the programmable compensating FIR filter (CFIR)
- High-rate interpolation (4 to 32) using the six stage cascade-integrate comb filter (CIC)

Figure 2-8. DUC Filter Chain

The purpose of the transmit filter chain, shown in Figure 2-8, is to interpolate the input signal data up to the mixer clock rate, nominally 122.88 MHz. The following table provides two examples of how the interpolation can be allocated among the three different filters for both CDMA and UMTS.

Table 2-6. Example UMTS and CDMA2000 DUC Transmit Modes

	Input Rate Rate	PFIR Interpolation	CFIR Interpolation	CIC Interpolation	Overall Interpolation
CDMA	1.2288 MSPS	2	2	25	100
UMTS	3.84 MSPS	2	2	8	32

2.1.5.1 Programmable FIR Filter

The programmable FIR filter (PFIR) pulse shapes the baseband signal data and interpolates by a fixed factor of two.

The PFIR length is programmable. This permits turning off taps and saving power if short filters are appropriate. The maximum PFIR filter length is a function of GC5318 clock rate and input sample rate and is limited by the number of coefficient memory registers. The number of taps available in CDMA mode ranges from 31 to 63. In UMTS mode it ranges from 15 to 63. In both cases, the number of taps is one less than a multiple of four (31, 35, ... 59, 63).

Subject to the above range, the maximum number of taps available in each mode is:

- UMTS Mode: $2 \times$ (txclk $\times$ input sample rate)
- CDMA Mode: txclk $\times$ input sample rate

Assuming a txclk of 122.88 MHz, both UMTS (3.84 MSPS) and CDMA (1.2288 MSPS) modes provide 63 taps. The same PFIR coefficients are used for both the A and B channels in CDMA mode.

The PFIR filter consists of 32 forward and reverse data RAM cells each 36 bits in width. The coefficient memory provides storage for up to 63 unique 18-bit taps. A 19 x 18 multiplier and full-precision accumulator form the filter convolution. An optional (pfir_gain) up-shift of one follows. Finally, the output is hard-limited.

The PFIR gain is:

Gain = sum(coefficients) $\times$ 2^[cfir_gain-19]

Table 2-7. Programming

VARIABLE	DESCRIPTION
crastsrttap_pfir(4:0)	Number of DUC PFIR filter taps is (2 x crastarttap) + 1
cdma_mode	When set, puts the CFIR and PFIR blocks in CDMA2000 mode.
symmetric_pfir	Set to '1' if filter is symmetric. This value saves a modest amount of power.
	The 18-bit PFIR filter coefficients are loaded by the software cmd5318. The user must provide a coefficient file with one integer coefficient per line. Note that the PFIR filter coefficients are shared by the A and B signals in CDMA mode.

2.1.5.2 Compensating FIR Filter

The CFIR filter interpolates by a fixed factor of two and is usually programmed to compensate for the CIC filter roll-off.

The CFIR filter length is programmable. This programmable length permits turning off taps and saving power if short filters are appropriate. The maximum CFIR filter length is a function of GC5318 clock rate and input sample rate and is limited by the number of coefficient memory registers. The number of CFIR taps in CDMA mode is 31 to 47, while in UMTS mode it is 15 to 31. In both cases, the number of taps is one less than a multiple of four (31, 35, ... 59, 63).

Subject to the above minimum, maximum, and increment values, the maximum number of taps available is:

- UMTS Mode: txclk $\times$ input sample rate
- CDMA Mode: 0.5 x (txclk $\times$ input sample rate)

For example, a txclk of 122.88 MHz in UMTS mode (at 3.84 MSPS) provides 31 taps, while CDMA (1.2288 MSPS) mode provides 47 taps.

The CFIR coefficients are shared by the A and B signals in CDMA mode.

CFIR gain is:

Gain = sum(coefficients) x $2^{cfir\_gain-19}$

Table 2-8. Programming

VARIABLE	DESCRIPTION
crastsrttap_cfir(4:0)	These bits define the number of taps that CFIR uses for the filtering. DUC CFIR: (2 x crastarttap_cfir) +1. **Note:** crastarttap_cfir must be odd.
symmetric_cfir	Set to '1' if filter is symmetric. Saves a bit of power.
cfir_gain	CFIR gain adjustment.
	The 18-bit PFIR filter coefficients are loaded by the software cmd5318. The user must provide a coefficient file with one integer coefficient per line. Note that the PFIR filter coefficients are shared by the A and B signals in CDMA mode.

2.1.5.3 CIC Filter

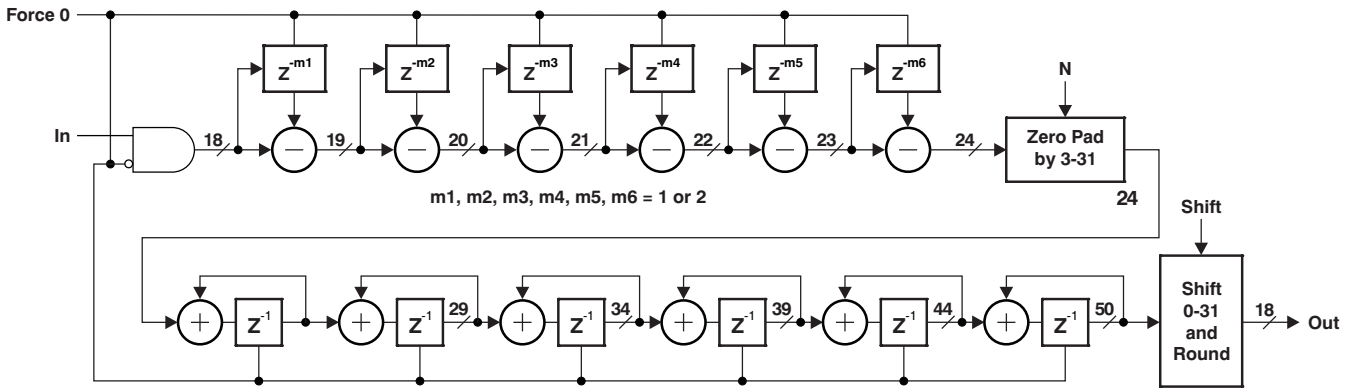


Figure 2-9. CIC Filter

The six stage CIC filter (as shown in Figure 2-9) interpolates over a programmable range from four to 32. The filter is made up of six banks of 24-bit subtractor sections followed by six banks of integrator sections. Each of the six subtractor sections can be independently programmed with a differential delay of one or two. A shift block follows the last integration stage and can shift the 50-bit accumulated data down by 31-TCIC_SHIFT bits yielding 18-bit output data.

The CIC filter exhibits a droop across its frequency response. Usually the preceding CFIR filter precompensates for the CIC droop with a gradually rising frequency response. However, it is also possible to provide the precompensation in the PFIR filter.

CIC interpolation filters can become unstable if an external event (such as a cosmic particle) disturbs a storage node in the CIC integrator section. This instability can add a bias that subsequently integrates out of control. The GC5318 CIC employs a patented method to first detect this bias, then automatically flush and reset the filter. Register bits are available to disable and to test this auto-flush feature. A maskable interrupt becomes active if a CIC error occurred.

The gain of the CIC filter is:

$$Ncic^5 \times 2^{(\text{number of stages where M=2})} \times 2^{(\text{CIC\_SCALE} - 31)}$$

where CIC_SCALE is 0 to 31. The CIC gain should have a value <1.0. Ncic is the interpolation ratio and is programmed as cic_interp_decim + 1.

Since the CIC output is full rate for both UMTS and CDMA, a complete hardware path is required for each of the signals A and B from this point on in the transmit signal path. For CDMA, there are four independent CIC filters (I/Q for signal A and I/Q for signal B). For UMTS, the two signal B CIC filters are disabled.

Table 2-9. Programming

VARIABLE	DESCRIPTION
cic_interp_decim(4:0)	The CIC interpolation is Ncic = cic_interp_decim + 1. This ratio applies to both A and B channels of the DUC block in CDMA mode. Legal values for cic_interp_decim are 3 to 31.
cic_scale_a(4:0)	The shift value for the A channel. A value of 0 is no shift; each increment in value increases the amplitude of the shifter output by a factor of 2.
cic_scale_b(4:0)	The shift value for the B channel. A value of 0 is no shift; each increment in value increases the amplitude of the shifter output by a factor of 2.
cic_m2_ena_a(5:0)	Sets the differential delay value M for each of the CIC subtractor stages for the A channel. Cic_m2_en_a(0) controls m1, cic_m2_en_a(5) controls the m5. A set bit programs the differential delay M to 2; if cleared, M is programmed to 1.
cic_m2_ena_b(5:0)	Sets the differential delay value M for each of the CIC subtractor stages for the B channel.
ssel_cic(2:0)	Sync source
cic_auto_flush_dis(3:0)	When set, disables the CIC auto-flush. Bits {0, 1, 2, 3} correspond to CICs for {CDMA-A I data, CDMA-A Q data, CDMA-B I data, CDMA-B Q data} sections.
cic_auto_flush_test(3:0)	On rising, forces a CIC overflow error. Program to 0, then to 1 for edge to occur. Bits {0, 1, 2, 3} correspond to CICs for {CDMA-A I data, CDMA-A Q data, CDMA-B I data, CDMA-B Q data} sections.
cic_auto_flush_clear(3:0)	On rising, clears a CIC overflow condition. Program to 0, then to 1 for edge to occur. Bits {0, 1, 2, 3} correspond to CICs for {CDMA-A I data, CDMA-A Q data, CDMA-B I data, CDMA-B Q data} sections.

2.1.6 Adjustable Channel Delay

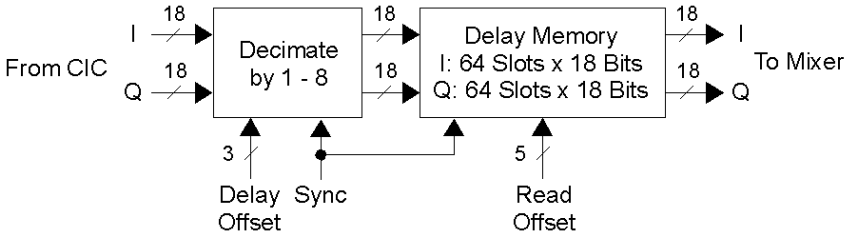


Figure 2-10. Delay Adjustment

The channel delay adjust function, shown in Figure 2-10, permits the user to add a programmable time delay in each of the upconverter paths. This function is used to calibrate time delays in multiple channels in the overall base transceiver system. The adjustable delay compensates for analog elements external to the digital upconversion such as cables, splitters, analog upconverters, filters, etc., and for differential delay between channels within the GC5318. There is an additional delay of two output sample times for each pair of DUC blocks to allow for pipelining of the sumchain (specifically, DUC0 and 1 have the same delay; DUCs 2 and 3 are the same but are two output sample times larger than DUC0 and 1, etc.).

There are two elements that need to be considered with respect to programming the delay: the decimation and delay memory blocks.

The decimation function reduces the sample rate from txclk to the desired output rate. Output decimation is required for CDMA mode, and is also used for Interleaved IQ outputs. The decimation amount is set by parameter (tadj_interp_decim+1). Phasing of the decimation operation permits finer delay resolution. The 3-bit delay offset parameter permits finer delay resolution in steps of the reciprocal of the GC5318 tx clock rate. At 122.88 MHz, this value would equate to a time delay resolution of 8.1 ns (1/32 chip for UMTS, 1/100 of a chip for CDMA). The offset may be set from 0 to tadj_interp_decim.

The coarse delay adjustment is done using a delay memory of 64 memory locations by 36 bits (18 for I and 18 for Q). Read and write pointers in the memory are separated by tadj_offset_coarse. Data written into a location is read out tadj_offset_coarse output sample times later. 24 locations are needed to equalize the time delay within the GC5318 for various channels. The remaining 40 locations provide a total delay of up to about 1.3 µs when the DUC output data rate is 30.72 MSPS.

A sync signal permits the decimation operation to be synchronized over multiple channels.

Table 2-10. Programming

VARIABLE	DESCRIPTION
tadj_offset_coarse_a(5:0)	Read offset into the 64-element memory for the A channel DUC. When tadj_offset_coarse_a = 62, then the delay is –2. When tadj_offset_coarse_a = 63, then the delay is –1. For all other values, the resulting delay is equal to the value.
tadj_offset_coarse_b(5:0)	Read offset into the 64-element memory for the B channel DUC when in CDMA mode. **Note:** When tadj_offset_coarse_b = 62, then the delay is –2. When tadj_offset_coarse_b = 63, then the delay is –1. For all other values, the resulting delay is equal to the value.
tadj_offset_fine_a(2:0)	Controls the zero offset (fine adjust) for the A side of the DUC. The fine adjust is mapped differently.
tadj_offset_fine_b(2:0)	Controls the zero offset (fine adjust) for the B side of the DUC when in CDMA mode. The fine adjust is mapped differently.
tadj_interp_decim(2:0)	The decimation value (1, 2, 4, or 8) for the DUC. Same for A and B channels when in CDMA mode.
ssel_tadj_fine(2:0)	Selects the sync source for the fine time adjust.
ssel_tadj_coarse(2:0)	Selects the sync source for the coarse time delay adjust.

For a decimation value of 1, the only legal setting is 0; there is no fine adjustment since there is no decimation moment.

tadj_offset_fine = 0 → fine delay by 0

For a decimation value of 2:

tadj_offset_fine = 0 → fine delay by 0
tadj_offset_fine = 1 → fine delay by 1

For a decimation value of 4:

tadj_offset_fine = 0 → fine delay by 0
tadj_offset_fine = 1 → fine delay by –1
tadj_offset_fine = 2 → fine delay by –2
tadj_offset_fine = 3 → fine delay by 1

For a decimation value of 8:

tadj_offset_fine = 0 → fine delay by 0
tadj_offset_fine = 1 → fine delay by –1
tadj_offset_fine = 2 → fine delay by –2
tadj_offset_fine = 3 → fine delay by –3
tadj_offset_fine = 4 → fine delay by –4
tadj_offset_fine = 5 → fine delay by –5
tadj_offset_fine = 6 → fine delay by –6
tadj_offset_fine = 7 → fine delay by 1

2.1.7 Mixer

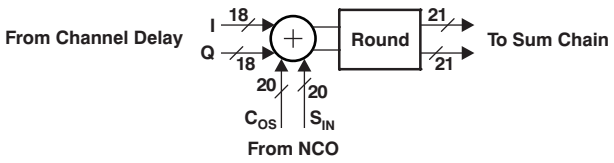


Figure 2-11. Mixer

The mixer is a complex multiplier which takes the baseband I and Q data that has been previously pulse-shaped and interpolated, and translates to a carrier frequency programmed into the NCO. The mixer data size is 18 bits for the signal path and 20 bits for the NCO path, as shown in Figure 2-11.

The gain through the mixer is –12 dB. It can be increased by 6 dB through a control bit. It is recommended that this extra gain always be used. The output is then rounded to 21 bits.

Mixer gain = $2^{mixer\_gain - 2}$

The mixer output of each channel is combined in daisy-chain fashion in four sum chain adder blocks that are described in a subsequent section.

For CDMA, the maximum output rate is txclk/2. The maximum output rate for UMTS is txclk.

Table 2-11. Programming

VARIABLE	DESCRIPTION
mixer_gain	When asserted, adds 6 dB of gain in the mixer. Should always be set.

2.1.8 NCO

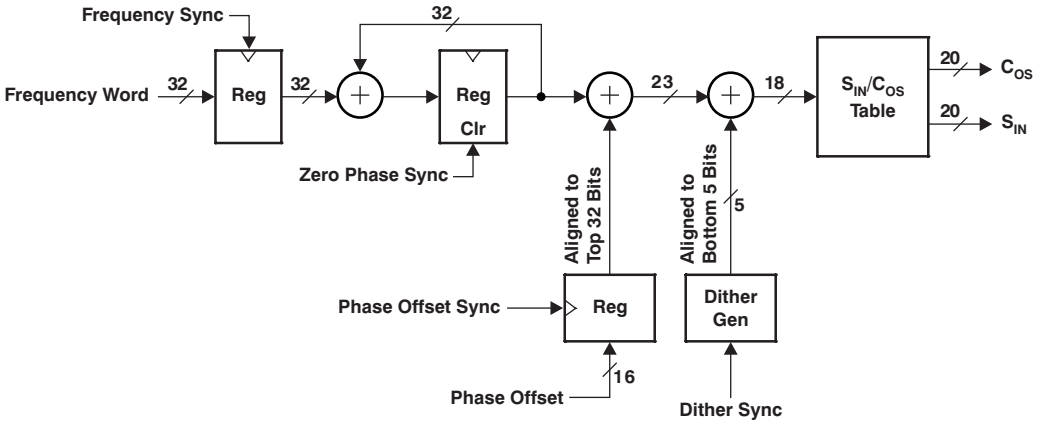


Figure 2-12. NCO

The NCO, shown in Figure 2-12, is a digital complex oscillator that translates (or upconverts) interpolated and filtered baseband signals to a programmable carrier frequency.

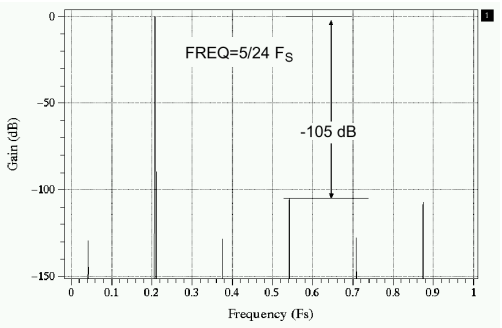
The block produces programmable complex digital sinusoids by accumulating a delta phase frequency word that is programmed by the user. A phase offset can be added to the accumulated value if desired for channel calibration purposes. The output of the accumulator is a phase value that indexes into a Sin/Cos ROM table which produces the complex sinusoid.

A 5-bit dither generator is provided, and generates a small level of digital pseudo-noise that is added to the phase accumulated value. It is useful for reducing NCO spurious outputs.

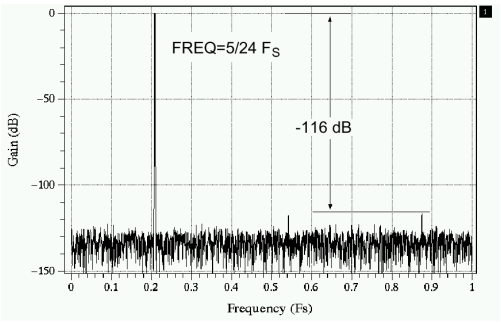
Table 2-12. Programming

VARIABLE	DESCRIPTION
dither_ena	When set, turns dither on. Clearing turns dither off.

The NCO spurious levels are shown in Figure 2-13 and Figure 2-14. Added phase dither randomizes the ROM lookup slightly, thereby creating the ROM lookup error—spreading the spurious energy around rather than concentrating it in a few frequencies. The phase dither is added below the LSB of the ROM lookup. If the tuning frequency has no high bits more than 17 bits below the msb, the phase dither has no effect. If the tuning frequency is a multiple of Fs/96, then an initial phase offset of four often reduces NCO spurs. Figure 2-13 and Figure 2-14 show the spur level performance of the NCO without dither, with dither, and with a phase offset value.

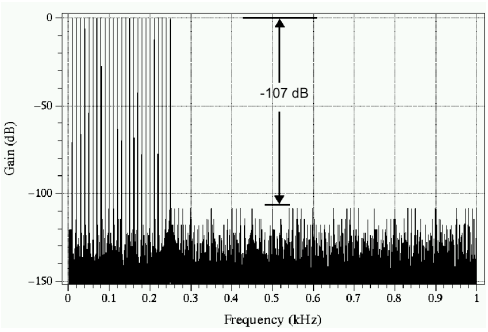


a) Worst Case Spectrum Without Dither

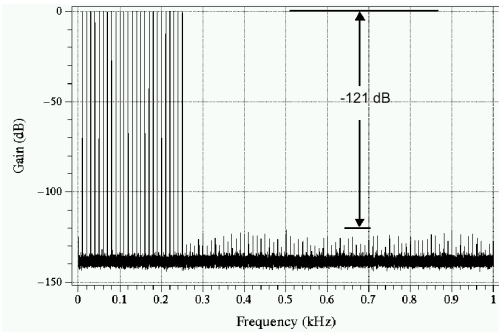


b) Spectrum With Dither (Tuned to Same Frequency)

Figure 2-13. Example NCO Spurs With and Without Dithering



a) Plot Without Dither or Phase Initialization



b) Plot With Dither and Phase Initialization

Figure 2-14. NCO Peak Spur Plot

The tuning frequency is specified as a 32-bit frequency word and is programmed as two sequential 16-bit words over the control port. The NCO operates at the same speed as the txclk/(tadj_interp_decim + 1). The frequency resolution is simply the $F_{CLK}/ 2^{32}$. The NCO frequency resolution is simply the $F_{CLK}/ 2^{32}$. As an example, at an input clock rate of 61.44 MHz, the frequency step size would be approximately 14 MHz. The frequency word is determined by the formula:

Frequency word (in decimal) = 2^{32} x Tuning Frequency/F_{CLK}

NOTE

Frequency tuning words can be positive or negative valued. Specifying a positive frequency value translates baseband frequencies upward. Specifying a negative tuning frequency translates baseband frequencies downwards.

Table 2-13. Programming

VARIABLE	DESCRIPTION
phase_add_a(31:0)	32-bit tuning frequency word for the A signal when in CDMA mode. Also for UMTS mode.
phase_add_b(31:0)	32-bit tuning frequency word for the B signal when in CDMA mode. Not used in UMTS mode.

The phase of the NCO Sin/Cos output can be adjusted relative to the phase of other channel NCOs by specifying a phase offset. The phase offset is programmed as a 16-bit word, yielding a step size of about 5.5 milliDegrees. The phase offset word is determined by the following formula:

Phase Offset Word = 2^{16} x Offset_in_Degrees / 360; or,

Phase Offset Word = 2^{16} x Offset_in_Radians / 2π

Table 2-14. Programming

VARIABLE	DESCRIPTION
phase_offset_a(15:0)	16-bit phase offset word for the A signal when in CDMA mode. Also for UMTS mode.
phase_offset_b(15:0)	16-bit phase offset word for the B signal when in CDMA mode. Not used in UMTS mode.

Various synchronization signals are available that are used to synchronize the NCOs of all channels with respect to each other. Frequency sync and phase offset sync determine when frequency and phase offset changes occur. For example, generating a frequency sync after programming the two frequency words causes the NCO (or multiple NCOs) to change frequency at that time, rather than after each of the three frequency words is programmed over the control bus. The NCO accumulator reset sync signal is used to force the sine and cosine oscillators to their zero phase state. Dither sync can be used to synchronize the dither generators of multiple NCOs.

Table 2-15. Programming

VARIABLE	DESCRIPTION
ssel_nco(2:0)	Sync source for NCO accumulator reset
ssel_dither(2:0)	Sync source for NCO dither reset
ssel_freq(2:0)	Sync source for NCO frequency register loading
ssel_phase(2:0)	Sync source for NCO phase register loading

2.1.9 Sum Chain

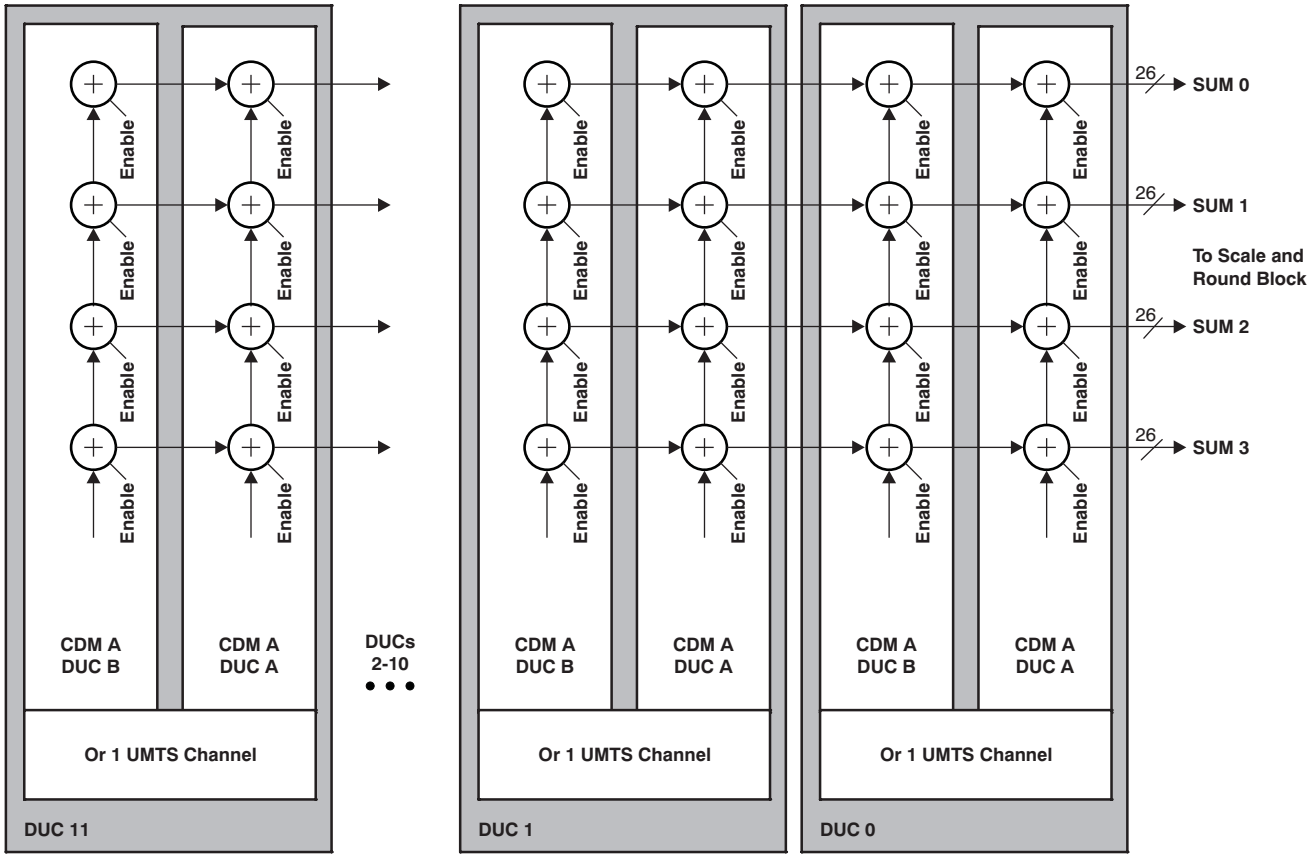


Figure 2-15. Sum Chain

The sum chain is a daisy-chain of all DUC outputs into four independent composite output streams. Each DUC output drives four complex adders, each summing the DUC contribution into the sum chain.

The DUC output data driving the adders is 21 bits. The sum chain partial sum outputs are 26 bits wide to allow for word growth. Each DUC output can contribute to any of the four sum chains via programmable enable lines. The output of the last daisy-chained sum is then the composite of all of the 24 CDMA or 12 UMTS channels. There must be no DUCs powered down within a sum chain that have lower numbers than those that are active. This condition would break the chain. For example, if DUCs 3-5 are used and active, DUCs 0-2 must not be powered down.

As shown in Figure 2-15, each DUC contains a portion of the sumchain. Individual sum chain outputs can be summed together using the parameters below.

Table 2-16. Programming

VARIABLE	DESCRIPTION
sumchn_sel_a(3:0)	Enable bits for signal A contribution to the four sum chain outputs. Signal A Out 0000 Signal A added to no busses 0001 Signal A I/Q to bus0 0010 Signal A I/Q to bus1 0100 Signal A I/Q to bus2 1000 Signal A I/Q to bus3 Note: Signal A output can contribute to any combination of the four sumchain outputs. The above 4-bit code can range from 0 to 15.
sumchn_sel_b(3:0)	Enable bits for signal B contribution to the four sum chains (only when in CDMA mode). Signal B Out 0000 Signal B added to no busses 0001 Signal B I/Q to bus0 0010 Signal B I/Q to bus1 0100 Signal B I/Q to bus2 1000 Signal B I/Q to bus3 Note: Signal B output can contribute to any combination of the four sumchain outputs. The above 4-bit code can range from 0 to 15.

2.2 Sum Chain Shifting and Rounding

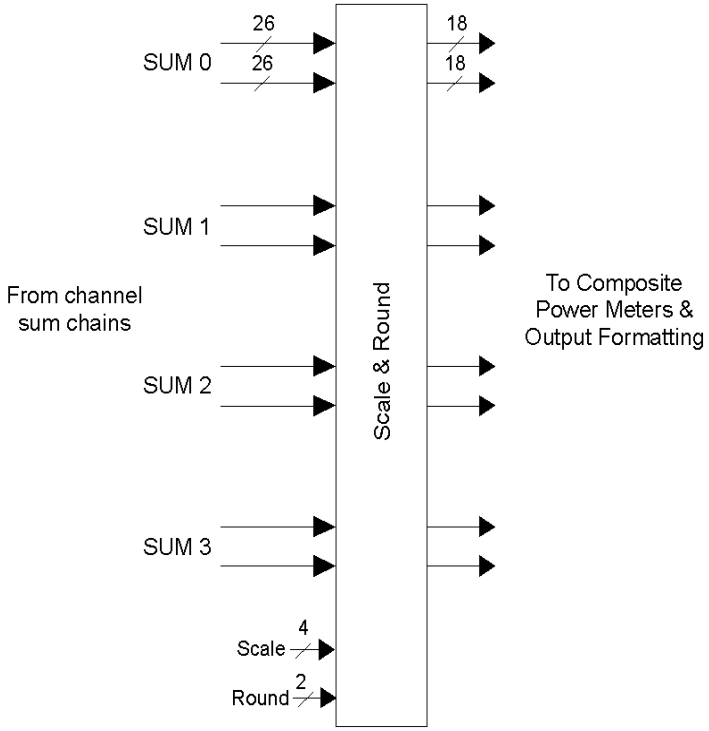


Figure 2-16. Final Sum Chain Scale and Round Block

Summed data is scaled from 26 bits down to 18 bits, as shown in Figure 2-16. The desired 18 bits can be taken anywhere over the 26-bit sum chain output window via a programmable register. These 18 bits can range from sumchain(25:8) on the top end to sumchain(17:0) on the bottom end of the 26-bit output.

The scaled data is then saturated to 18, 16, 14, or 12 bits. Rounded data is MSB-justified with the bottom bits zeroed. For example, 12-bit rounding would output data to the top 12 bits of the 18-bit word and the bottom 6 bits would be zeroed.

Gain = $2^{interf\_scale-5}$

Table 2-17. Programming

VARIABLE	DESCRIPTION
interf_scale_0(3:0) interf_scale_1(3:0) interf_scale_2(3:0) interf_scale_3(3:0)	Selects the sum chain scale value for each of the four sum chains. The 18-bit output can be slid anywhere across the 26-bit window. 0000 = sumchain(25:8) 0001 = sumchain(24:7) … 0111 = sumchain(18:1) 1000 = sumchain(17:0)
interf_round(1:0)	Specifies the rounding of all four sum chains. 00 = 18 bits 01 = 16 bits 10 = 14 bits 11 = 12 bits

2.2.1 Power Meters

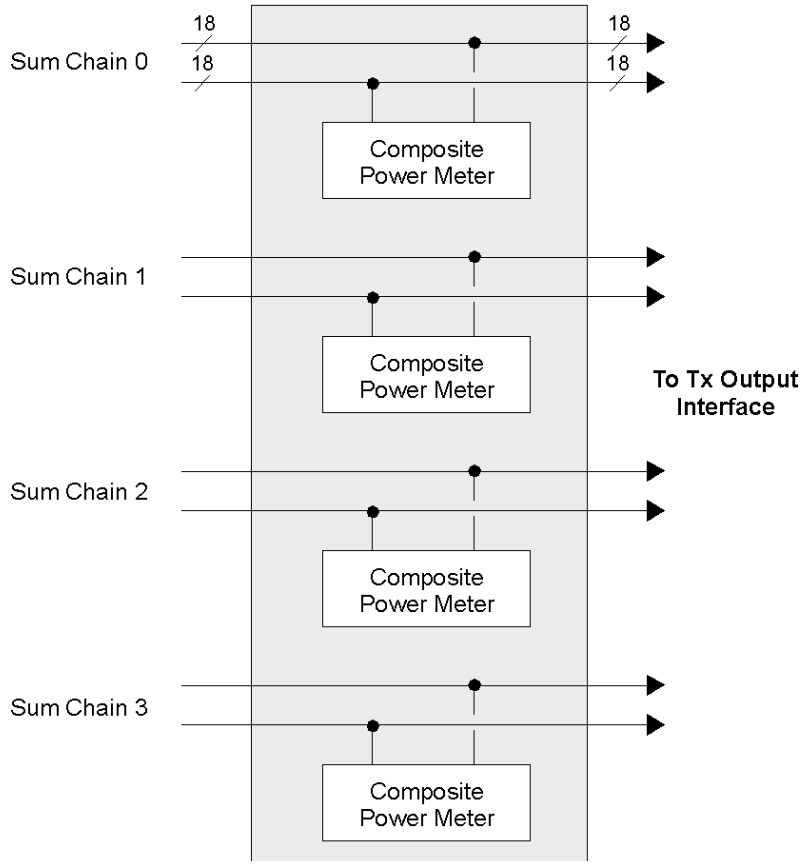


Figure 2-17. Power Meter Block

The composite power in each of the four sum chains can be measured using power meters similar to those used in the individual DUC blocks.

There are four composite RMS power meters, one for each of the four sum chains, as shown in Figure 2-17. Each of the above power meters is independently programmable with respect to the measurement period, interval, and delay from sync. The following two sections describe the sum chain power meters in more detail.

2.2.1.1 Composite RMS Power Meter

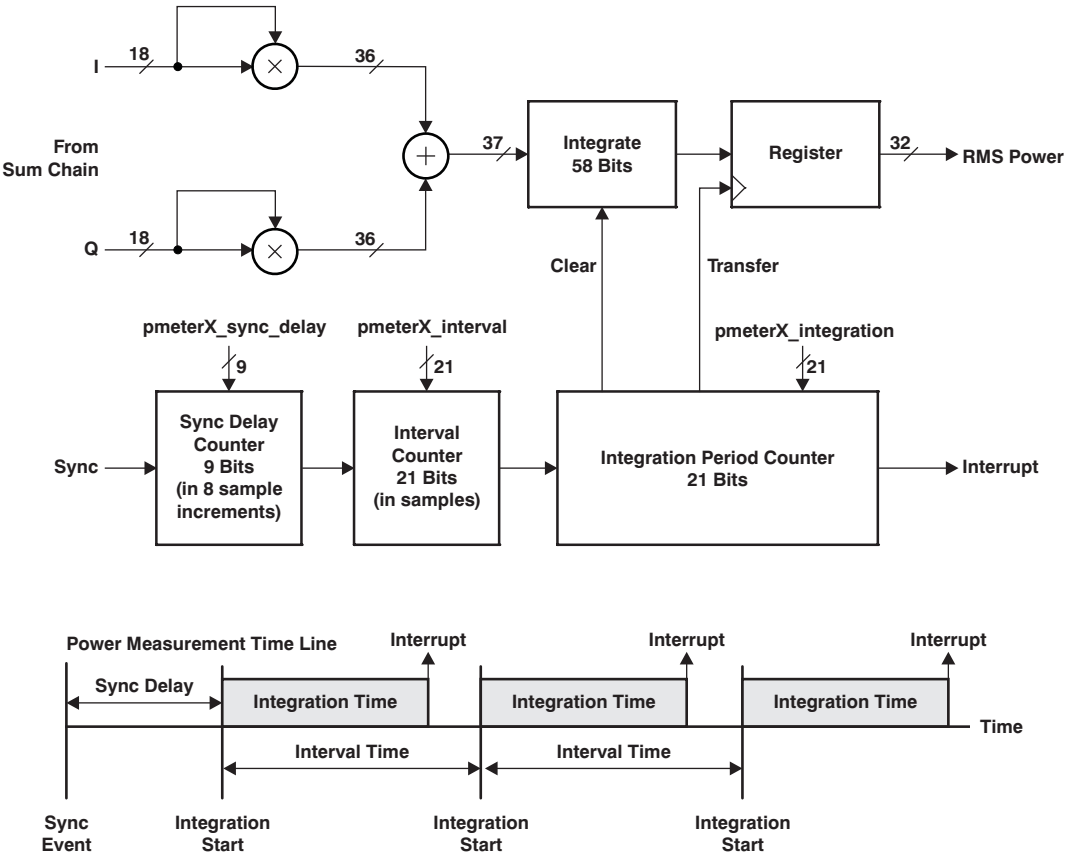


Figure 2-18. RMS Power Meter

The GC5318 provides four independent output ports, each of which is the sum of a number of individual carriers (a sum chain). Four composite RMS power meters measure the RMS power of the combined carriers in each of the four sum chains. These power meters are similar to those used to measure the RMS power of each individual channel, but have different counter lengths.

The input to the power meter is the scaled and rounded output of a sum chain. Power is calculated by squaring each 18-bit I and Q sample, summing and then integrating the summed-squared results into a 58-bit accumulator. The integration time is pmeter_integration (maximum of 21 bits) output sample periods.

There is a programmable 21-bit interval counter that sets the interval over which power measurements are repeated. The interval time = pmeter_interval + 1. The interval time must be greater than (not equal to) the integration time. A measurement integration period is started at the beginning of each interval time.

The process begins with a sync event starting the 9-bit delay counter. After the delay count + 2 samples, the integration interval is started. The power is calculated for each I and Q sample and added to the 58-bit accumulator. The integration continues until the integration count is met, at which point the upper 32 bits of the 58-bit integrator are transferred to the read register and an interrupt is generated. A new measurement period starts at the end of the interval period.

NOTE

Each of the four composite RMS power meter blocks has its own delay sync, interval, and integration period counters, as well as separate sync source registers.

Table 2-18. Programming

VARIABLE	DESCRIPTION
comp_pmeterX_result_lsb(15:0)	Lower 16 bits of the composite power measurement for sum chain X. X = 0, 1, 2, or 3
comp_pmeterX_result_msb(31:16)	Upper 16 bits of the composite power measurement for sum chain X. X = 0, 1, 2, or 3
comp_pmeterX_integration_lsb(15:0)	Lower 16 bits of the 21-bit integration period. X = 0, 1, 2, or 3
comp_pmeterX_integration_msb(20:16)	Upper five bits of the 21-bit integration period. X = 0, 1, 2, or 3
comp_pmeterX_sync_delay(8:0)	Power meter delay sync period. X = 0, 1, 2, or 3
comp_pmeterX_interval_lsb(15:0)	Lower 16 bits of the 21-bit measurement interval. X = 0, 1, 2, or 3
comp_pmeterX_interval_msb(20:16)	Upper five bits of the 21-bit measurement interval. The Interval time must be greater than the integration time for each of the four composite power meters. X = 0, 1, 2, or 3
ssel_comp_pmeter_X(2:0)	Sync source. X = 0, 1, 2, or 3

2.3 GC5318 Output Interface

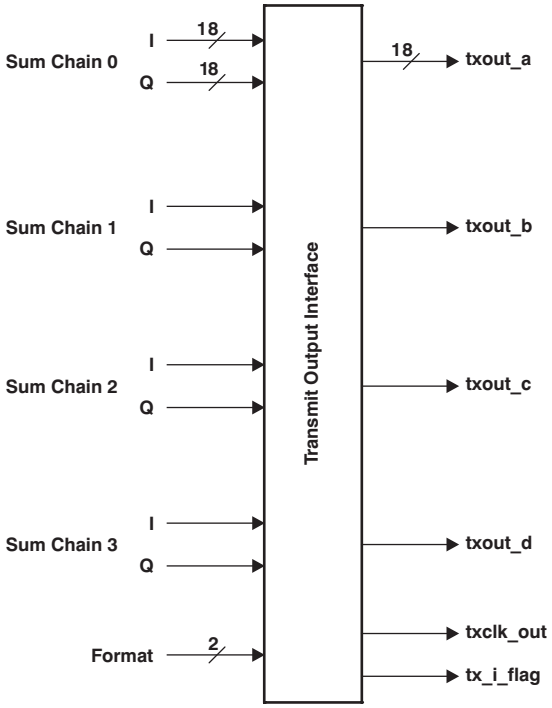


Figure 2-19. Output Interface

The GC5318 provides four output signal data ports, as shown in Figure 2-19. Each port can be enabled or disabled. Disabled ports are held low and can also be tri-stated.

Each 18-bit port outputs the sum of the carriers contributing to the composite signal stack. Output data can be real or complex valued. Complex I/Q data can be output either interleaved over a single output port or over two ports separately.

Real output data would generally be selected driving a single D/A converter to an IF frequency. Complex output data would be selected when subsequent post-processing such as power amplifier predistortion is employed. Complex outputs can also be used to drive a pair of D/A converters (one for I, the other for Q) for direct I/Q upconversion using a quadrature modulator device.

I and Q complex output data can be interleaved over a single 18-bit port or simultaneously over two separate output ports at half the rate. Signal tx_I_flag is active when I data is being output when in complex output interleaved mode. When complex output data is noninterleaved, I data is output on port 0 and Q data is output on port 1 for sum chain 0. For sum chain 1, I data is output on port 2 and Q data is output on port 3.

Real output data is output over a single 18-bit port. For CDMA mode, the maximum real output rate is txclk/2. The maximum real output rate for UMTS mode is txclk.

The maximum complex output rate with I and Q data on separate outputs is txclk/2 for CDMA mode and txclk for UMTS mode. If the complex output data is interleaved on a single bus, the maximum rate is txclk/2 for both UMTS and CDMA and the toggle rate between I and Q samples is txclk.

NOTE

The tx_clk_out signal cannot be at full rate (txclk rate) if the mixer is not at full rate (for CDMA mode, the mixer cannot be at full rate). If a full-rate clock output signal is desired, the tst_clk signal can be used, with the tst_rate parameter programmed to 0.

Table 2-19. Programming

VARIABLE	DESCRIPTION
interf_ena(3:0)	When bits are set, enables the corresponding outputs. When cleared, outputs are disabled and held low.
interf_real	When set, outputs are real. When cleared, outputs are complex.
interf_interl	When set, complex data is output interleaved.
3-state(3)	When set, turns on tx_data_out3 outputs.
3-state(2)	When set, turns on tx_data_out2 outputs as well as sync_tst, aflag_tst, and clk_tst.
3-state(1)	When set, turns on tx_data_out1 outputs.
3-state(0)	When set, turns on tx_data_out0 outputs as well as tx_iflag and tx_clk_out.
trt_rate	The value here controls the output clock rate on the clk_tst pin. A value of 0 gives a full-rate output clock (txclk rate); a 1 gives half-rate output clock; a 3 gives 1/4th rate output clock, and so on. The number of txclk cycles for which the clk_tst signal is high + low = 1 + tst_rate.

3 GC5318 General Control

The GC5318 is configured over a bidirectional 16-bit parallel data microprocessor control port. The control port permits access to the control registers that configure the chip. The control registers are organized using a paged-access scheme using six address lines. Half of the 64 addresses (address 32 through address 63) represent global registers. The other 32 (address 0 through address 31) are paged registers. This arrangement permits accessing a large number of control registers using relatively few address lines.

Global address 33 is the page register. Writing a 16-bit value to this register sets the page on which future write or read operations are performed. These paged registers contain the actual parameters that configure the chip and are accessed by writing/reading address 0 through address 31.

Global registers (address 32 through address 63) are used to read/write GC5318 parameters that are global in nature and can benefit from single-cycle read/write operations. Examples include chip status, reset, sync options, checksum ramp parameters, and the page register.

3.1 Control Data, Address, and Strobes

The control bus consists of 16 bidirectional control data lines C[0:15], six address lines A[0:5], a read enable line $\overline{RD}$, a write enable line $\overline{WR}$, and a chip enable line $\overline{CE}$. These lines usually interface to a microprocessor or DSP chip and are intended to look like a block of memory.

Data is written by:

1. Setting up the desired address A[0:5]
2. Setting $\overline{CE}$ low,
3. Setting the desired data on C[0:15], and then
4. Pulsing $\overline{WR}$ low. Data is written when $\overline{WR}$ returns high.

3.2 MPU Timing Diagrams

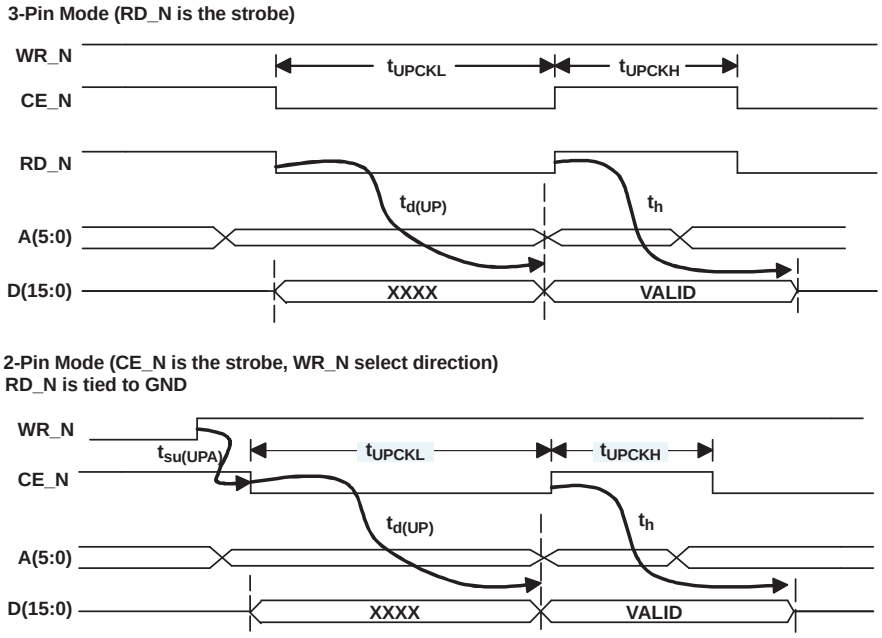


Figure 3-1. Read Diagrams

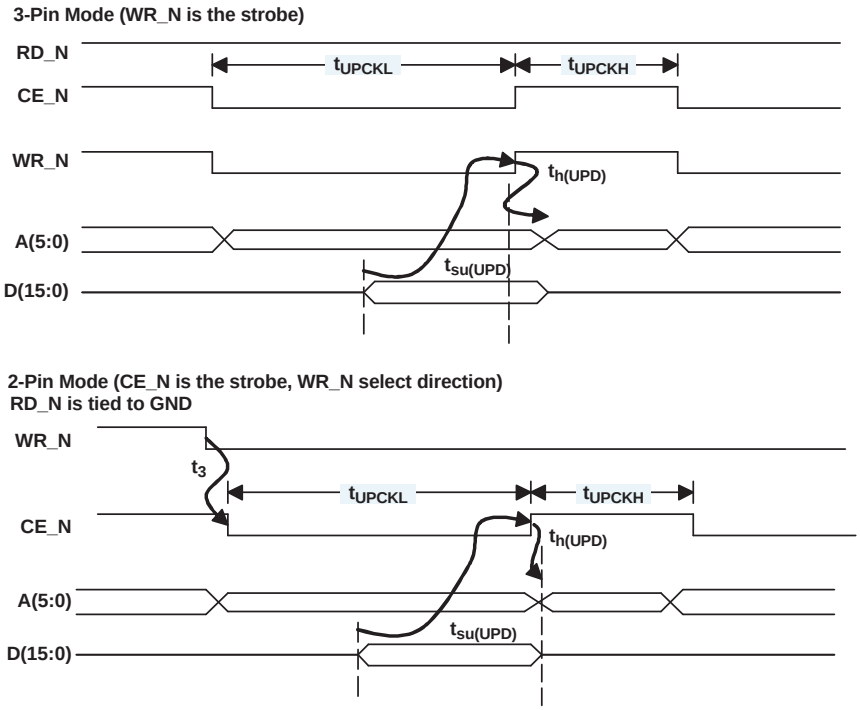


Figure 3-2. Write Diagrams

3.3 Interrupt Handling

When a GC5318 block sets an interrupt, the interrupt pin goes active if the interrupt source is not masked. The microprocessor should then read the three interrupt flag registers to determine the source of the interrupt. The microprocessor then has to read the interrupt source circuits register(s) to clear the interrupt pin and interrupt flag register bit. The three interrupt registers are listed in the global registers part of the control registers section.

3.4 Sync Signals

Various function blocks within the GC5318 need to be synchronized in order to realize predictable results. The GC5318 provides a flexible system where each function block that requires synchronization can be independently synchronized either from device pins or from a software one-shot. The one-shot option is setup and triggered through control registers. There are four hardware sync input pins available. These sync pins are qualified on the chip rising clock edge.

Table 3-1 shows the different sync modes available.

Table 3-1. Sync Modes Available

MODE	Transmit Sync Source
0	TxSyncA
1	TxSyncB
2	TxSyncC
3	TxSyncD
4	DUC sync counter TC
5	DUC sync triggered by one-shot
6	0 (always off)
7	1 (always on)

Table 3-2 and Table 3-3 summarize the blocks that have functions which can be synchronized using the above eight sync options:

Table 3-2. Common Syncs

VARIABLE	DESCRIPTION
ssel_comp_pmeter	Initializes the xmit composite power meter
ssel_duc_counter	Initializes the xmit common sync counter
ssel_duc_serp	Initializes the xmit serial interface
ssel_duc_gain	Updates the gain register
ssel_duc_pilot	Initializes the xmit pilot generator and updates the pilot gain
ssel_duc_tadj	Updates the delay adjust register
ssel_duc_pmeter	Initializes the xmit channel power meter

Table 3-3. Channel Syncs

VARIABLE	DESCRIPTION
ssel_duc_nco	Resets the NCO accumulator
ssel_duc_freq	Updates the NCO frequency registers
ssel_duc_phase	Updates the NCO phase register
ssel_duc_dither	Resets the NCO dither

3.5 Initialization

Chip initialization procedures are available from Texas Instruments.

3.6 GC5318 Board Diagnostics

The GC5318 contains built-in test features that can be used to confirm that the chip is operating correctly and to help users debug their boards and systems that contain the GC5318.

The diagnostic and board test procedures can be downloaded from the web at www.ti.com as the GC5318 Diagnostics Designer's Kit.

4 GC5318 Programming

The GC5318 contains over 3,000 control and coefficient registers, many of which must be initialized in order to fully configure the chip. Rather than program each of these registers individually, Texas Instruments supplies a configuration program called **cmd5318** that accepts top-level configuration information for the chip and then generates the full register map and control writes required to program the chip.

The cmd5318 program, its user's guide, and example configuration files can be downloaded from the web at www.ti.com as the GC5318 Configuration Designer's Kit.

The configuration controls have been defined in the functional description of each section of the chip. The following tables summarize these controls and identify which register and which bits within the registers they occupy.

Each control register table has a column identifying whether the variable must be specified by the user in cmd5318 (U), is typically left at the default value and does not need to be specified (D), is computed by cmd5318 and should not be set (C), or is for expert use only (E).

Tables are also included that show the top level page mapping for the chip controls, the status and measurement result registers, and additional controls that are used with the GC101/GC5318 DIMM evaluation platform.

4.1 cmd5318 Keywords

These keywords are used by the cmd5318 program to set general configuration parameters.

Name	Argument	Use	Description
print	config	Global	Tells cmd5318 to generate a configuration output file for general use.
print	gc101	Global	Tells cmd5318 to generate a configuration output file for GC101 use.
print	analysis	Global	Tells cmd5318 to generate a analysis output file
print	table	Global	Tells cmd5318 to generate a table output file
print	power	Global	Tells cmd5318 to generate an approximate power consumption output file.
txclk	clock frequency in MHz	Global	Used to calculate transmit tuning frequencies
duc	channel_number	DUC Channels	All controls after this keyword apply to this DUC channel
copy_ducchan	channel_number	DUC Channels	Copy the DUC channel commands from the specified channel to the current channel
freqa	tuning frequency in MHz	DUCs	Sets the NCO tuning frequency for the UMTS channel or for the a-path in the current channel if in CDMA mode.
freqb	tuning frequency in MHz	DUCs	Sets the NCO tuning frequency for the b-path in the current channel if in CDMA mode.
pfir_coeff	filename for pfir taps	DUCs	Specifies the filename containing the pfir taps
cfir_coeff	filename for cfir taps	DUCs	Specifies the filename containing the cfir taps
overall_gaina	overall channel gain	DUCs	Optional—Specifies the overall gain for the UMTS channel or the a-path in the current channel if in CDMA mode.
overall_gainb	overall channel gain	DUCs	Optional—Specifies the overall gain for the b-path in the current channel if in CDMA mode.

4.1.1 GC5318 DIMM Keywords

These keywords are used to control how the GC5318 DIMM operates in the GC101 evaluation board.

Name	Argument	Type	Default	Use	Description
loopback	0 or 1	G	0	GC5318 DIMM	EVM signal select control must be set to 0.
spin0	0 or 1	G	0	GC5318 DIMM	EVM signal select control-txin_[0:5]_[a:b] ports.
spin1	0 or 1	G	0	GC5318 DIMM	EVM signal select control-txin_[6:11]_[a:b] ports.
sigout0	0-3	G	3	GC5318 DIMM	00 = txout_a enabled, 01 – txout_c enabled, 10—not used, 11—not used.

Name	Argument	Type	Default	Use	Description
sigout1	0-3	G	3	GC5318 DIMM	00 = txout_b enabled, 01 – txout_d enabled, 10—not used, 11—not used.
txout_lsb	0 or 1	G	0	GC5318 DIMM	When asserted, the 2 LSBs each of active txout are output to GC101, else the various strobes/syncouts are output.
sel_syncout	0-3	G	3	GC5318 DIMM	(if txout_lsb = 0) selects which signals are output. 00-tx_sync_out + tx_i_flag, 01–sync_tst + aflag_tst, 10-tx_sync_out0 + interrupt.
res_op_en	0-3	G	3	GC5318 DIMM	(if txout_lsb = 0) when 00, test 9 + test11 is output , test7 + test8 data is output.
sel_clkout	0-3	G	0	GC5318 DIMM	Selects the output clock source. 00 – txclk_out, 01-clk_tst, 10-clkout+.
adcclk_set	0 or 1	G	0	GC5318 DIMM	Not used.

4.1.2 Page Map

This page map describes which pages and what registers within the pages are used. All other pages are unused. This table is provided for reference only. The registers and the bits within the registers are described in the following control register tables.

Pages	Address	Description
BASE+000 and BASE+020	00–1F	PFIR Coefficients, 2 LSBs
BASE+040 and BASE+060	00–1F	PFIR Coefficients, 16 MSBs
BASE+080 and BASE+0A0	00–1F	CFIR Coefficients, 2 LSBs
BASE+040 and BASE+0E0	00–1F	CFIR Coefficients, 16 MSBs
BASE+100	00–1F	Channel Control Registers
BASE+120	00–1D	Channel Control Registers
Where BASE is (DUCn x 0200) for DUCn from 0 to 11, and is (DDCn x 0200 + 2000) for DDCn from 0 to 11		
1800	00–09	Reserved
1800	0A–1F	Reserved
1820	00–04	Reserved
1820	06	Reserved
1C00	00–11 and 1A–1E	General Transmit Control Registers
1C20	00–07 and 0C	General Transmit Control Registers

4.1.3 Status and Read-Only Registers

These registers can be accessed by the user to read status or read measurement results from the chip. These register names are not used in cmd5318.

Name	Page	Address	LSB Position	Bit Width	Description
Version	Global	20	0	5	A 5-bit read only register indicating the current GC5318 revision status
inter_pmeter	Global	25	12	4	Indicates which transmit composite power meter generated the interrupt
inter_tx_pmeter	Global	26	4	12	Indicates which transmit power meter generated the interrupt
inter_tx_cic	Global	28	0	12	Indicates which transmit cic overflow detect generated the interrupt
comp_pmeter0_lsb	1C20	00	0	16	16 LSBs of composite power meter 0
comp_pmeter0_msb	1C20	01	0	16	16 MSBs of composite power meter 0
comp_pmeter1_lsb	1C20	02	0	16	16 LSBs of composite power meter 1
comp_pmeter1_msb	1C20	03	0	16	16 MSBs of composite power meter 1
comp_pmeter2_lsb	1C20	04	0	16	16 LSBs of composite power meter 2
comp_pmeter2_msb	1C20	05	0	16	16 MSBs of composite power meter 2
comp_pmeter3_lsb	1C20	06	0	16	16 LSBs of composite power meter 3
comp_pmeter3_msb	1C20	07	0	16	16 MSBs of composite power meter 3
tx_chk_sum	1C20	0C	0	16	Transmit checksum result

4.1.4 Global Control Variables

These registers contain global controls for the GC5318. These registers are not paged and are accessed directly using addresses 32–63 (20–3f hex)

Variable Name	Type	Address	LSB Position	Bit Width	Default	Description
page	E	21	0	16	0	The page register selects which page addresses 00-1F (0-31) will access.
slf_tst_ena	D	22	15	1	0	(TESTING PURPOSES) Turns on the checksum LFSR.
tst_sel_chan	E	22	1	2	0	(TESTING PURPOSES) In each slice, these bits control which tst_out is sent to the transmit block. (which duc in the slice)
tst_on	E	22	0	1	0	(TESTING PURPOSES) When asserted the testbus is active; txout_c (17:0), and txout_d (17:0) form the 36-bit test word output.
						The following tristates are active low; 0 turns the output on; 1 tristates it.
3-state_10	E	23	10	1	1	Reserved outputs for test; must be set to 1 (tristate)
3-state_9	C	23	9	1	1	This bit turns on the slice5 tx_sync.
3-state_8	C	23	8	1	1	This bit turns on the slice4 tx_sync.
3-state_7	C	23	7	1	1	This bit turns on the slice3 tx_sync.
3-state_6	C	23	6	1	1	This bit turns on the slice2 tx_sync.
3-state_5	C	23	5	1	1	This bit turns on the slice1 tx_sync.
3-state_4	C	23	4	1	1	This bit turns on the slice0 tx_syncand tx_sync_out.
3-state_3	C	23	3	1	1	This turns on the txout_d outputs.
3-state_2	C	23	2	1	1	This turns on the txout_c CLK_TST, IFLAG_TST, and SYNC_TST outputs.
3-state_1	C	23	1	1	1	This turns on the txout_b outputs.
3-state_0	C	23	0	1	1	This turns on the txout_a, TX_IFLAG, and TXCLK_OUT outputs.
tx_oneshot	D	24	15	1	0	When set, a one-shot pulse is sent to the transmit blocks for syncing. This option works only if the blocks are programmed to see the oneshot. To use the one-shot again, it must be programmed back to a '0' and then back to a '1'.
imask_comp_pmeter	D	29	12	4	0	Interrupt mask bits for the transmit composite power meter
imask_tx_pmeter	D	2A	4	12	0	Interrupt mask bits for the composite power meter
imask_tx_cic	D	2C	0	12	0	Interrupt mask bits for overflow detection in the transmit cics

4.1.5 General Controls

These registers control the transmit output interface from the channels.

Variable Name	Type	Page	Address	LSB Position	Bit Width	Default	Description
tst_sel_slice	E	1C00	00	13	3	0	(TESTING PURPOSES) This value selects the slice block that is generating the tst_out data. (Which DUC)
tst_rate	E	1C00	05	11	5	0	The value here controls the output clock rate on the clk_tst pin. A value of 0 gives a full-rate output clock (txclk rate), a 1 gives half-rate output clock, a 3 gives 1/4th rate output clock, and so on. The number of txclk cycles for which the clk_tst signal is high + low = 1 + tst_rate.
interf_round	D	1C00	00	8	2	0	Controls round point on the transmit output data; {00 = 18b, 01 = 16b, 10 = 14b, 11 = 12b}. Rounded output data is MSB justified. For example, a 12b round point causes the output data to be presented on the output pins (17:6), and the output pins (5:0) to be held low.
interf_ena	D	1C00	00	4	4	15	Enables the individual transmit output busses 3 through 0. Disabled busses are always held low.
interf_interl	U	1C00	00	1	1	0	Enables interleaved I/Q data when asserted.
interf_real	U	1C00	00	0	1	1	Enables real only outputs when asserted. Complex data is output when cleared.
interf_scale_3	U	1C00	01	12	4	0	Selects the scaling between the sumchain output signals and the transmit output pins and transmit composite power meters. Appropriate limiting and rounding is performed as required by the programmed round point. Gain = $2^{(interf\_scale)}$. For sumchain 3.
interf_scale_2	U	1C00	01	8	4	0	Selects the scaling between the sumchain output signals and the transmit output pins and transmit composite power meters. Appropriate limiting and rounding is performed as required by the programmed round point. Gain = $2^{(interf\_scale)}$. For sumchain 2
interf_scale_1	U	1C00	01	4	4	0	Selects the scaling between the sumchain output signals and the transmit output pins and transmit composite power meters. Appropriate limiting and rounding is performed as required by the programmed round point. Gain = $2^{(interf\_scale)}$. For sumchain 1
interf_scale_0	U	1C00	01	0	4	0	Selects the scaling between the sumchain output signals and the transmit output pins and transmit composite power meters. Appropriate limiting and rounding is performed as required by the programmed round point. Gain = $2^{(interf\_scale)}$. For sumchain 0
comp_pmeter0_count_lsb	D	1C00	02	0	16	0	This is the number of sample sets to accumulate for a power measurement. Ia and Qa (signal) are each squared and accumulated. Each pair of I and Q are equal to one integration count. The accumulation interval is initiated when the sync is asserted and the programmed sync_delay has expired or when the interval start time is reached. When the integration count is reached, the accumulated powers are made available for MPU access and an interrupt is generated. Bits 0–15
comp_pmeter0_count_msb	D	1C00	03	0	5	0	Bits 16–20 of the number of sample sets to accumulate for a power measurement. (Used in conjunction with the previous variable.)
comp_pmeter0_sync_delay	D	1C00	03	7	9	0	Programmable start delay from sync, in eight output sample units.

Variable Name	Type	Page	Address	LSB Position	Bit Width	Default	Description
comp_pmeter0_interval_lsb	D	1C00	04	0	16	0	This is the interval over which the integration is restarted and must be greater than the integration count. The interval start counter and RMS power accumulation is started at the sync pulse after the programmed delay and every time the interval counter reaches its limit. Bits 0–15
comp_pmeter0_interval_msb	D	1C00	05	0	5	0	Bits 16–20 of the interval over which the integration is restarted. (Used in conjunction with the previous variable.)
comp_pmeter1_count_lsb	D	1C00	06	0	16	0	See description for pmeter0
comp_pmeter1_count_msb	D	1C00	07	0	5	0	See description for pmeter0
comp_pmeter1_sync_delay	D	1C00	07	7	9	0	See description for pmeter0
comp_pmeter1_interval_lsb	D	1C00	08	0	16	0	See description for pmeter0
comp_pmeter1_interval_msb	D	1C00	09	0	5	0	See description for pmeter0
comp_pmeter2_count_lsb	D	1C00	0A	0	16	0	See description for pmeter0
comp_pmeter2_count_msb	D	1C00	0B	0	5	0	See description for pmeter0
comp_pmeter2_sync_delay	D	1C00	0B	7	9	0	See description for pmeter0
comp_pmeter2_interval_lsb	D	1C00	0C	0	16	0	See description for pmeter0
comp_pmeter2_interval_msb	D	1C00	0D	0	5	0	See description for pmeter0
comp_pmeter3_count_lsb	D	1C00	0E	0	16	0	See description for pmeter0
comp_pmeter3_count_msb	D	1C00	0F	0	5	0	See description for pmeter0
comp_pmeter3_sync_delay	D	1C00	0F	7	9	0	See description for pmeter0
comp_pmeter3_interval_lsb	D	1C00	10	0	16	0	See description for pmeter0
comp_pmeter3_interval_msb	D	1C00	11	0	5	0	See description for pmeter0
duc_counter_lsb	D	1C00	1A	0	16	65535	32-bit interval timer common to all DUC sync inputs. This timer may be programmed to any interval count, and each DUC synchronization input can select this counter as a source. This counter increments on every TXCLK rising edge. Bits 0–15
duc_counter_msb	D	1C00	1B	0	16	65535	Bits 16-31 of the above mentioned 32-bit interval timer.
ssel_duc_counter	U	1C00	1C	8	3	0	Selects the sync source for the DUC sync counter.
duc_counter_width	D	1C00	1C	0	8	0	Sets the width of the counter generated sync pulse in TX clock cycles, from 1 to 256. The width of this pulse must be long enough to be captured by the slowest block to use the DUC counter sync.
ssel_comp_pmeter_0	U	1C00	1D	12	3	0	Selects the sync source for composite power meter 0.
ssel_comp_pmeter_1	U	1C00	1D	8	3	0	Selects the sync source for composite power meter 1.
ssel_comp_pmeter_2	U	1C00	1D	4	3	0	Selects the sync source for composite power meter 2.
ssel_comp_pmeter_3	U	1C00	1D	0	3	0	Selects the sync source for composite power meter 3.
ssel_txsync_out	U	1C00	1E	0	3	0	Selects the sync source for the TXSYNC_OUT pin.

4.1.6 DUC Channel Controls

These controls follow the duc <channel_number> keywords in the cmd5318 configuration file.

Variable Name	Type	Page	Address (HEX)	LSB Position	Bit Width	Default	Description
cdma_mode	U	0100	00	15	1	1	When asserted the block is in the dual channel CDMA2000 mode.
crastarttap_pfir	C	0100	00	8	5	0	These bits define the number of taps that PFIR uses for the filtering. Another way of looking at these bits is that this value is the location in the RAM of the center tap. PFIR: (2 x crastarttap_pfir) +1. Note: crastarttap_pfir must be odd.
crastarttap_cfir	C	0100	00	3	5	0	These bits define the number of taps that CFIR uses for the filtering. CFIR: (2 x crastarttap_cfir) +1. Note: crastarttap_cfir must be odd.
symmetric_pfir	C	0100	00	14	1	0	When asserted the block PFIR is symmetric.
symmetric_cfir	C	0100	00	13	1	0	When asserted the block CFIR is symmetric.
pfir_gain	U	0100	01	13	3	0	this is the gain for the PFIR. 0 = 2e – 18, 1= 2e – 17.
cfir_gain	U	0100	01	5	1	0	This is the gain for the CFIR. 0 = 2e – 19, 1 = 2e – 18.
pmeter_integration_duc	D	0100	02	0	13	0	This is the number of four sample sets to accumulate for a power measurement. In CDMA mode, one sample set is the I and Q of the signal and diversity. Ia and Qa (signal) are each squared and accumulated and Ib and Qb (diversity) are squared and accumulated. In UMTS mode, each I and Q pair are squared and accumulated. Four samples are equal to one integration count. The count is initiated when the sync is asserted or when the interval start time is reached. When the integration count is reached, the accumulated powers are made available for MPU access and an interrupt is generated.
pmeter_sync_delay_duc	D	0100	03	9	7	0	The delay from selected sync source to when the power calculation starts.
pmeter_interval_duc	D	0100	03	0	9	0	The start interval timer is the interval over which the integration is restarted and must be greater than the integration count. The interval start counter and RMS power accumulation is started at the sync pulse after the programmed delay and every time the interval counter reaches its limit. This value is in 64 sample units.
pilot_gain_0	D	0100	04	0	16	0	Pilot channel gain word, aligned with MSB of the input data. 0xFFFF generates a full scale complex pilot signal added to the user signal. Setting the gain to 0x0000 causes no pilot signal to be added. Only valid for UMTS, should be set to 0x0000 for CDMA.
pilot_gain_1	D	0100	05	0	16	0	This value MUST be set to the same value as pilot_gain_0.
pilot_psc_lsb	D	0100	06	0	16	1	The lower 16 bits of the 18-bit pilot X LFSR initial value. This 18b word is loaded on pilot sync event. The value loaded here that corresponds to 3gpp primary scrambling code (PSC) 0 is 0x00001. Users must calculate the correct initial value to implement the other 511 PSCs.
pilot_psc_msb	D	0100	07	14	2	0	The upper 2 bits of the 18-bit pilot X LFSR initial value. This 18b word is loaded on pilot sync events. The value loaded here that corresponds to 3gpp primary scrambling code (PSC) 0 is 0x00001. Users must calculate the correct initial value to implement the other 511 PSCs.
pilot_diversity	D	0100	07	13	1	0	Select between main and diversity pilot symbol generation. (0 = main, 1 = diversity)
pilot_delay	D	0100	08	0	16	0	Unsigned delay value in chips from the pilot sync event, from 0 to 38399 chips.
ssel_pmeter	U	0120	0B	8	3	0	Selects the sync source for the channel power meter.
ssel_serial	U	0120	0B	0	3	0	Selects the sync source for the DUC serial interface state machines.
ssel_tadj_fine	U	0120	0C	12	3	0	Selects the sync source for the fine time adjust decimation (DUC).

Variable Name	Type	Page	Address (HEX)	LSB Position	Bit Width	Default	Description
ssel_tadj_coarse	U	0120	0C	8	3	0	Selects the sync source for the course time adjust delay selection.
ssel_gain	U	0120	0C	4	3	0	Selects the sync source for the DUC gain register.
gainfora	U	0100	0C	0	16	8192	This is the unsigned gain that is multiplied with the CDMA channel A or UMTS channel input signal. The gain multiply is calculated as gainfora/8192.
gainforb	U	0100	0D	0	16	8192	This is the unsigned gain that is multiplied with the CDMA channel B input signal.
ssel_nco	U	0120	0D	12	3	0	Selects the sync source for the NCO accumulator reset.
ssel_dither	U	0120	0D	8	3	0	Selects the sync source for the NCO phase dither generator reset.
ssel_freq	U	0120	0D	4	3	0	Selects the sync source for the NCO frequency register.
ssel_phase	U	0120	0D	0	3	0	Selects the sync source for the NCO phase offset register.
cic_scale_a	U	0100	0E	11	5	0	This sets the gain shift at the output of the CDMA A channel (or UMTS channel) CIC. 0x00 is no shift; each increment by 1 increases the signal amplitude by 2X.
cic_scale_b	U	0100	0E	6	5	0	This sets the gain shift at the output of the CDMA B channel CIC. 0x00 is no shift; each increment by 1 increases the signal amplitude by 2X.
cic_interp_decim	U	0100	0E	0	5	24	Sets the CIC interpolation, where interpolation is cic_interp_decim + 1 in the digital up converters.
cic_m2_ena_a	D	0100	0F	10	6	0	Programs the CDMA A channel (or UMTS channel) CIC fir sections M value to 2 when set, 1 when cleared. cic_m2_ena_a(0) controls the M value for the first comb section and cic_m2_ena_a(5) controls the M value for the last comb section.
cic_m2_ena_b	D	0100	0F	4	6	0	Programs the CDMA B channel CIC fir sections M value to 2 when set, 1 when cleared. cic_m2_ena_b(0) controls the M value for the first comb section and cic_m2_ena_b(5) controls the M value for the last comb section.
cic_auto_flush_dis	E	0100	10	12	4	0	Disables the automatic flush feature in the CIC accumulators.
cic_flush_test	E	0100	10	8	4	0	Forces an overflow detection in the CIC only on a rising edge of this bit, therefore it must be programmed to '0' and then back to `1' for the edge to occur.
cic_flush_clear	E	0100	10	4	4	0	Clears an overflow error manually when set, again only on a rising edge does this occur.
tadj_offset_coarse_a	D	0100	11	10	6	0	This is part of the time delay adjust. This is the coarse offset and is really an offset from the write address in the delay ram. This value affects the A channel if CDMA mode is being used, or the UMTS channel. Each LSB is one more offset between input to the course delay block and the output of the course block.
tadj_offset_coarse_b	D	0100	11	4	6	0	This is part of the time delay adjust. This is the coarse offset and is really an offset from the write address in the delay ram. This value affects the B channel if CDMA mode is being used. Each LSB is one more offset between input to the course delay block and the output of the course block.
tadj_offset_fine_a	D	0100	12	13	3	0	This is part of the time delay adjust. This is the fine adjust value. It adjusts the time delay at the clock rate. This value affects the A channel if CDMA mode is being used, or the UMTS channel.
tadj_offset_fine_b	D	0100	12	10	3	0	This is part of the time delay adjust. This is the fine adjust value. It adjusts the time delay at the clock rate. This value affects the B channel if CDMA mode is being used.
tadj_interp_decim	U	0100	12	7	3	1	This is the decimation or interpolation value for the fine time adjust block. Decimation or interpolation can be from 1 to 8. This value affects both the A and B channels if CDMA mode is being used, or the UMTS channel.

Variable Name	Type	Page	Address (HEX)	LSB Position	Bit Width	Default	Description
phase_add_a_lsb	C	0100	13	0	16	0	This 32 bit word is used to control the frequency of the NCO. Derived from the keyword freqa by cmd5318. (for CDMA channel A or UMTS channel). Lower 16 bits.
phase_add_a_msb	C	0100	14	0	16	0	Upper 16 bits of the above 32-bit word.
phase_add_b_lsb	C	0100	15	0	16	0	This 32-bit word is used to control the frequency of the NCO. Derived from the keyword freqb by cmd5318. (for CDMA channel B). Lower 16 bits.
phase_add_b_msb	C	0100	16	0	16	0	Upper 16 bits of the above 32-bit word.
phase_offset_a	D	0100	17	0	16	0	This is the fixed phase offset added to the output of the frequency accumulator for sinusoid generation in the NCO. (UMTS mode and A channel in CDMA mode)
phase_offset_b	D	0100	18	0	16	0	This is the fixed phase offset added to the output of the frequency accumulator for sinusoid generation in the NCO for CDMA B channel.
dither_ena	D	0100	19	15	1	0	This bit controls whether or not dither is turned on(1) or off(0).
test_bits_1	E	0100	19	13	2	0	TEST BITS. Set to 0 for normal operation.
pmeter_sync_disable	D	0100	19	12	1	0	Turns off the sync to the channel power meter. This can be used to individually turn off syncs to a channels power meter, while still having syncs to other power meters on the chip.
ddc_duc_ena	U	0100	19	11	1	0	When set this turns on the DUC.
mixer_gain	U	0100	19	9	1	0	Adds a fixed –6 dB of gain to the mixer output(before round and limiting) when asserted. Else adds –12-dB gain when deasserted.
mpu_ram_read	E	0100	19	8	1	0	(TESTING PURPOSES) Allows the coefficient RAMs in the PFIR/CFIR to be read out the mpu data bus. This cannot be done during normal operation and must be done when the state of the output data is not important. THIS BIT MUST BE SET ONLY DURING THE READ OPERATION.
sumchn_sel_b	U	0100	19	4	4	2	This word controls the second set of additions for the CDMA B signal in the sumchn output. The selection bits are not mutually exclusive.
sumchn_sel_a	U	0100	19	0	4	1	This word controls the first set of additions for the CDMA A signal (or UMTS signal) in the sumchn output. The selection bits are not mutually exclusive.
tst_sel_block	E	0100	1A	0	6	0	(TESTING PURPOSES) This is the selection of which signal comes out the test bus. When a constant `0' is selected this also reduces power by preventing the data at the input of the test block from changing. Howeve,rit does not stop the clock.
serp_tran_bits	U	0100	1B	11	5	17	Number of input bits per sample-1; for 18 bits, this is set to {10001}.
serp_tran_fsdel	D	0100	1B	8	2	1	Delay between frame sync output and MSB of serial data {3, 2, 1, 0}.
serp_tran_4pin	D	0100	1B	7	1	0	Selects 2-pin mode when cleared and 4-pin mode when set.
serp_tran_fsinvl	U	0100	1B	0	7	50	Transmit serial interface frame sync interval in bit clocks.
serp_tran_clkdiv	U	0100	1C	0	4	1	Transmit serial interface clock divider rate-1; 0 is full rate, and 15 divides the clock by 16. For example, to run the serial interface at 1/4 the transmit clock, set serp_tran_clkdiv(3:0) = 0011.
ssel_pilot	U	0120	0B	4	3	0	Selects the sync source for the DUC pilot code generator.

5 GC5318 Pin Description

5.1 Signals

Signal Name	Ball Desig	Type	Description
txclk	K26	input	Transmit clock input
txin_0_a	T23	input	DUC 0 serial in data. CDMA A: I/Q UMTS: I
txin_1_a	U25	input	DUC 1 serial in data. CDMA A: I/Q UMTS: I
txin_0_b	T24	input	DUC 0 serial in data. CDMA B: I/Q UMTS: Q
txin_1_b	U26	input	DUC 1 serial in data. CDMA B: I/Q UMTS: Q
txin_2_a	W26	input	DUC 2 serial in data. CDMA A: I/Q UMTS: I
txin_3_a	V25	input	DUC 3 serial in data. CDMA A: I/Q UMTS: I
txin_2_b	U24	input	DUC 2 serial in data. CDMA B: I/Q UMTS: Q
txin_3_b	V26	input	DUC 3 serial in data. CDMA B: I/Q UMTS: Q
txin_4_a	Y26	input	DUC 4 serial in data. CDMA A: I/Q UMTS: I
txin_5_a	W25	input	DUC 5 serial in data. CDMA A: I/Q UMTS: I
txin_4_b	V24	input	DUC 4 serial in data. CDMA B: I/Q UMTS: Q
txin_5_b	U23	input	DUC 5 serial in data. CDMA B: I/Q UMTS: Q
txin_6_a	W23	input	DUC 6 serial in data. CDMA A: I/Q UMTS: I
txin_7_a	AA26	input	DUC 7 serial in data. CDMA A: I/Q UMTS: I
txin_6_b	Y25	input	DUC 6 serial in data. CDMA B: I/Q UMTS: Q
txin_7_b	W24	input	DUC 7 serial in data. CDMA B: I/Q UMTS: Q
txin_8_a	Y23	input	DUC 8 serial in data. CDMA A: I/Q UMTS: I
txin_9_a	AB26	input	DUC 9 serial in data. CDMA A: I/Q UMTS: I
txin_8_b	AA25	input	DUC 8 serial in data. CDMA B: I/Q UMTS: Q
txin_9_b	Y24	input	DUC 9 serial in data. CDMA B: I/Q UMTS: Q
txin_10_a	AA23	input	DUC 10 serial in data. CDMA A: I/Q UMTS: I
txin_11_a	AC26	input	DUC 11 serial in data. CDMA A: I/Q UMTS: I
txin_10_b	AB25	input	DUC 10 serial in data. CDMA B: I/Q UMTS: Q
txin_11_b	AA24	input	DUC 11 serial in data. CDMA B: I/Q UMTS: Q
tx_sync_out_0	AB24	output	Transmit serial interface strobe for DUC 0, 1 (txin_[0,1]_[a,b])
tx_sync_out_1	AC25	output	Transmit serial interface strobe for DUC 2, 3 (txin_[2,3]_[a,b])
tx_sync_out_2	AD26	output	Transmit serial interface strobe for DUC 4, 5 (txin_[4,5]_[a,b])
tx_sync_out_3	AB23	output	Transmit serial interface strobe for DUC 6, 7 (txin_[6,7]_[a,b])
tx_sync_out_4	AC24	output	Transmit serial interface strobe for DUC 8, 9 (txin_[8,9]_[a,b])
tx_sync_out_5	AD23	output	Transmit serial interface strobe for DUC 10, 11 (txin_[10,11]_[a,b])
tx_synca	K24	input	Transmit sync input
tx_syncb	J25	input	Transmit sync input
tx_syncc	H26	input	Transmit sync input
tx_syncd	K23	input	Transmit sync input
tx_sync_out	F23	output	Transmit general purpose output sync
txclk_out	E23	output	Transmit output clock
tx_i_flag	D24	output	Transmit output iflag
txout_a_17	B19	output	Transmit output bus a MSB
txout_a_16	A20	output	Transmit output bus a
txout_a_15	C19	output	Transmit output bus a
txout_a_14	B20	output	Transmit output bus a
txout_a_13	A21	output	Transmit output bus a
txout_a_12	D19	output	Transmit output bus a
txout_a_11	C20	output	Transmit output bus a

Signal Name	Ball Desig	Type	Description
txout_a_10	B21	output	Transmit output bus a
txout_a_9	A22	output	Transmit output bus a
txout_a_8	D20	output	Transmit output bus a
txout_a_7	C21	output	Transmit output bus a
txout_a_6	B22	output	Transmit output bus a
txout_a_5	A23	output	Transmit output bus a
txout_a_4	C22	output	Transmit output bus a
txout_a_3	B23	output	Transmit output bus a
txout_a_2	A24	output	Transmit output bus a
txout_a_1	D22	output	Transmit output bus a
txout_a_0	C23	output	Transmit output bus a LSB
txout_b_17	B14	output	Transmit output bus b MSB
txout_b_16	C14	output	Transmit output bus b
txout_b_15	D14	output	Transmit output bus b
txout_b_14	A15	output	Transmit output bus b
txout_b_13	B15	output	Transmit output bus b
txout_b_12	C15	output	Transmit output bus b
txout_b_11	A16	output	Transmit output bus b
txout_b_10	B16	output	Transmit output bus b
txout_b_9	A17	output	Transmit output bus b
txout_b_8	C16	output	Transmit output bus b
txout_b_7	B17	output	Transmit output bus b
txout_b_6	D16	output	Transmit output bus b
txout_b_5	A18	output	Transmit output bus b
txout_b_4	C17	output	Transmit output bus b
txout_b_3	B18	output	Transmit output bus b
txout_b_2	A19	output	Transmit output bus b
txout_b_1	D17	output	Transmit output bus b
txout_b_0	C18	output	Transmit output bus b LSB
txout_c_17	C9	output	Transmit output bus c MSB
txout_c_16	D10	output	Transmit output bus c
txout_c_15	A8	output	Transmit output bus c
txout_c_14	B9	output	Transmit output bus c
txout_c_13	C10	output	Transmit output bus c
txout_c_12	A9	output	Transmit output bus c
txout_c_11	D11	output	Transmit output bus c
txout_c_10	B10	output	Transmit output bus c
txout_c_9	C11	output	Transmit output bus c
txout_c_8	A10	output	Transmit output bus c
txout_c_7	B11	output	Transmit output bus c
txout_c_6	A11	output	Transmit output bus c
txout_c_5	C12	output	Transmit output bus c
txout_c_4	B12	output	Transmit output bus c
txout_c_3	A12	output	Transmit output bus c
txout_c_2	D13	output	Transmit output bus c
txout_c_1	C13	output	Transmit output bus c
txout_c_0	B13	output	Transmit output bus c LSB
txout_d_17	C4	output	Transmit output bus d MSB

Signal Name	Ball Desig	Type	Description
txout_d_16	D5	output	Transmit output bus d
txout_d_15	A3	output	Transmit output bus d
txout_d_14	B4	output	Transmit output bus d
txout_d_13	C5	output	Transmit output bus d
txout_d_12	A4	output	Transmit output bus d
txout_d_11	B5	output	Transmit output bus d
txout_d_10	C6	output	Transmit output bus d
txout_d_9	D7	output	Transmit output bus d
txout_d_8	A5	output	Transmit output bus d
txout_d_7	B6	output	Transmit output bus d
txout_d_6	C7	output	Transmit output bus d
txout_d_5	D8	output	Transmit output bus d
txout_d_4	A6	output	Transmit output bus d
txout_d_3	B7	output	Transmit output bus d
txout_d_2	C8	output	Transmit output bus d
txout_d_1	A7	output	Transmit output bus d
txout_d_0	B8	output	Transmit output bus d LSB

5.2 Microprocessor Signals

Signal Name	Ball Desig	Type	Description
d0	AD8	input/output	MPU register interface data bus LSB
d1	AE7	input/output	MPU register interface data bus
d2	AF6	input/output	MPU register interface data bus
d3	AC8	input/output	MPU register interface data bus
d4	AD7	input/output	MPU register interface data bus
d5	AE6	input/output	MPU register interface data bus
d6	AF5	input/output	MPU register interface data bus
d7	AC7	input/output	MPU register interface data bus
d8	AD6	input/output	MPU register interface data bus
d9	AE5	input/output	MPU register interface data bus
d10	AF4	input/output	MPU register interface data bus
d11	AD5	input/output	MPU register interface data bus
d12	AE4	input/output	MPU register interface data bus
d13	AF3	input/output	MPU register interface data bus
d14	AC5	input/output	MPU register interface data bus
d15	AD4	input/output	MPU register interface data bus MSB
a0	AB4	input	MPU register interface address bus LSB
a1	AD1	input	MPU register interface address bus
a2	AC2	input	MPU register interface address bus
a3	AB3	input	MPU register interface address bus
a4	AA4	input	MPU register interface address bus
a5	AC1	input	MPU register interface address bus MSB
rd_n	Y4	input	MPU register interface read—active low
wr_n	AA3	input	MPU register interface write—active low
ce_n	AB2	input	MPU register interface chip enable—active low
reset_n	R24	input	Chip reset—active low
interrupt	AC3	output	Chip interrupt

5.3 JTAG Signals

Signal Name	Ball Desig	Type	Description
tdi	N23	input	JTAG test data in
tms	M26	input	JTAG test mode select
trst_n	M25	input	JTAG test reset (same as trst—the "_n" is for consistency, being active low)
tck	M24	input	JTAG test clock
tdo	L26	output	JTAG test data out

5.4 Factory Test and No Connect Signals

Signal Name	Ball Desig	Type	Description
testmode0	R26	Input	Do not connect
testmode1	P24	Input	Do not connect
scanen	P25	Input	Do not connect
aflag_tst	E24	Output	Do not connect
sync_tst	D25	Output	Do not connect
clk_tst	C26	Output	Do not connect
fa002_scan	T26	Input	Do not connect
fa002_clk	R23	Input	Do not connect
fa002_out	T25	Output	Do not connect
zero	N25	Input	Do not connect
rxclk	L24	Input	Ground
adcclk	D3	Input	Ground
	F26, G24, G25, H23, L23	Input	Tie each pin high through 100Ω resistors to VPAD
	K25, M23, L25, D26, E25, E26, F24, F25, G23, J26	No connect	Do not connect
	C1, D1, D2, E1–E4, F1–F4, G1– G4, G26, H1–H4, H24, H25	No connect	Do not connect
	J1–J3, K1, J24, K2–K4, L1– L4, M1–M4, N2, N3, P2–P4	No connect	Do not connect
	R1– R4, T1–T4, U1– U4, V1–V3, W1– W4, Y1–Y3	No connect	Do not connect
	AA1, AA2, AB1, AC10, AC11, AC13, AC14, AC16, AC17, AC19, AC20, AC22, AD9–AD22	No connect	Do not connect
	AE8–AE23, AF7–AF12, AF15–AF24	No connect	Do not connect

5.5 Power and Ground Signals

Signal Name	Ball Desig	Description
GND	A1, A2, A13, A14, A25, A26, B1, B3, B24, B26, C2, C25, N1, N26, P1, P26, AD2, AD25, AE1, AE24, AE3, AE26, AF1, AF2, AF13, AF14, AF25, AF26, L11, L12, L13, L14, L15, L16, M11–M16, N11–N16, P11–P16, R11–R16, T11–T16	Ground
VCORE	B2, D4, N4, AC4, AE2, B25, D23, P23, AC23, AE25, C3, J4, V4, AD3, C24, J23, V23, AD24	Core power
VPAD	D6, D12, D18, AC6, AC12, AC18, D9, D15, D21, AC9, AC15, AC21	I/O power

5.6 Power Monitoring

Signal Name	Ball Desig	Description
vcoremon	N24	These pins monitor the internal power distribution. They cannot carry significant current and should not be connected to normal power and ground. It is recommended that this pin be brought to a small probe point for future monitoring/debugging purposes.
gndmon	R25	It is recommended that this pin be brought to a probe point for future monitoring/debugging purposes.

5.7 JTAG

The JTAG standard for boundary scan testing is implemented for board testing purposes. Internal scan test is not be supported. Five device pins are dedicated for JTAG support: tdi, tdo, tms, tck, and trst_n. The BSDL file is available on the web.

6 Specifications

6.1 Absolute Maximum Ratings(1)

		VALUE	UNIT
V_{PAD}	Pad ring supply voltage	–0.3 to +4	V
V_{CORE}	Core supply voltage	–0.3 to +1.8	V
V_{IN}	Input voltage (undershoot and overshoot)	–0.5 to V_{PAD} + 0.5	V
	Clamp current for an input or output	–20 to +20	mA
T_{stg}	Storage temperature	–65 to +140	°C
T_J	Junction temperature	+105	°C
	Lead soldering temperature (10 seconds)	+300	°C
	ESD classification	Class 2 (Passed 2.5-kV HBM, 500-V CDM, 150-V MM)	
	Moisture sensitivity	Class 4 (Four days' floor life at 30°C/60%H)	
	Reflow conditions	JEDEC standard, 240°C max	

(1) Exceeding the absolute maximum ratings (min or max) may cause permanent damage to the part. These are stress only ratings and are not intended for operation.

6.2 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{PAD}	Pad ring supply voltage	3	3.6	V
V_{CORE}	Core supply voltage	1.5	1.65	V
$V_{PAD} – V_{CORE}$	Supply voltage difference		2	V
T_A	Temperature ambient, no air flow(1)	–40	+85	°C
T_J	Junction temperature(2)		+105	°C

(1) Chips specifications in Section 6.3 and Section 6.5 are production tested to +100°C case temperature. QA tests are performed at +85°C.
(2) Thermal management will be required for full rate operation; see the following table. The circuit is designed for junction temperatures up to +125°C. Sustained operation at elevated temperatures reduces long-term reliability. Lifetime calculations based on maximum junction temperature of +105°C.

6.3 Thermal Characteristics

THERMAL CONDUCTIVITY[1]		388 BGA	UNIT
θ_{JA}	Theta junction-to-ambient (still air)	13.5	°C/W
θ_{JA2m}	Theta junction-to-ambient (2m/s estimated)	9.3	°C/W
θ_{JC}	Theta junction-to-case	2.4	°C/W

(1) Air flow reduces θ_{JA} and is highly recommended.

6.4 Power Consumption

The maximum power consumption is a function of the operating mode of the chip. The cmd5318 estimates the typical power supply current for the chip in a specific configuration. The *AC Characteristics* table provides maximum current in a maximum configuration used in production test.

Current consumption on the pad supply is primarily due to the external loads and follows C x V x F. Internal loads are estimated at 2 pF per pin. Data outputs have a transition density of going from a zero to a one, once per four clocks, while clock outputs transition every cycle. The frame strobes consume negligible power due to the low transition frequency. In general:

Ipad = Σ DataPad/4 x C x F x V + Σ ClockPad x C x F x V

A worst case current would be all transmit ports operating at 125 MHz.

Ipad = (1+(4 x 18 + 4 x 2 x 6)/4) x (C + 2pF) x Fout x Vpad = 31 x 22 pF x 125 MHz x 3.3 V = 280 mA.

A more typical application with two ports active would use roughly 150 mA.

6.5 DC Operating Conditions

At –40°C to +85°C case, unless otherwise noted.

PARAMETER		VPAD = 3 V to 3.6 V			UNIT
		MIN	TYP	MAX	
V_{IL}	Voltage input low[1][2]			0.8	V
V_{IH}	Voltage input high[1][2]	2			V
V_{OL}	Voltage output low[1][2] (I_{OL} = 2 mA)			0.5	V
V_{OH}	Voltage output high[1][2] (I_{OH} = –2 mA)	2.4		V_{PAD}	V
$\lvert I_{PU} \rvert$	Pullup current (V_{IN} = 0 V) (tdi, tms, trst_n, reset_n) (nominal 20 µA)[1][2]	5		35	µA
$\lvert I_{PD} \rvert$	Pulldown current (V_{IN} = V_{PAD}) (all other inputs and bidirs) (nominal 20 µA)[2]	5		35	µA
$\lvert I_{IN} \rvert$	Leakage (V_{IN} = V_{PAD}) (tdi, tms, trst_n, reset_n)[2]			2	µA
	Leakage (V_{IN} = 0) (all other inputs and bidirs)[2]			2	
	Leakage (V_{IN} = 0 or V_{PAD}) (all outputs)[2]			2	
I_{CCQ}	Quiescent supply current, I_{CORE}[2]			8	mA
C_{IN}	Capacitance for inputs[3]		5		pF
C_{BI}	Capacitance for bidirectionals[3]		5		pF

(1) Voltages are measured at low speed. Output voltages are measured with the indicated current load.
(2) Each part is tested at +100°C case temperature for the given specification. Lots are sample tested at –40°C.
(3) Controlled by design and process and not directly tested.

6.6 AC Characteristics

PARAMETER[1]		MIN	MAX	UNIT
F_{CK}	Clock frequency (txclk) in selected modes[2] [3]		125	MHz
	Clock frequency (txclk) unrestricted[2]		80	
t_{TXCKL}	Clock low period (below V_{IL}) (txclk)[2]	3		ns
t_{TXCKH}	Clock high period (above V_{IH}) (txclk)[2]	3		ns
t_r, t_f	Clock rise and fall times (V_{IL} to V_{IH}) (txclk)[4]		2	ns
$t_{su(TX)}$	Input setup (txin_[0–11]_[a–b], tx_sync[a–d]) before txclk rises[2]	2.2		ns
$t_{h(TX)}$	Input hold (txin_[0–11]_[a–b], tx_sync[a–d]) after txclk rises[2]	1.1		ns
$t_{d(TX)}$	Data output delay (tx_sync_out_[0–5], tx_iflag, txout_[a–d]_[0–17]) after txclk rises[2]		6.5	ns
$t_{OH(TX)}$	Data output hold (tx_sync_out_[0–5], tx_iflag, txout_[a–d]_[0–17]) after txclk rises[2]	1.5		ns
F_{JCK}	JTAG clock frequency (tck)[2]		40	MHz
t_{JCKL}	JTAG clock low period (below V_{IL}) (tck)[2]	8		ns
t_{JCKH}	JTAG clock high period (above V_{IH}) (tck)[2]	8		ns
$t_{su(J)}$	JTAG input (tdi or tms) setup before tck goes high[2]	2		ns
$t_{h(J)}$	JTAG input (tdi or tms) hold time after tck goes high[2]	9		ns
$t_{d(J)}$	JTAG output (tdo) delay from falling edge of tck[2]		6	ns
$t_{su(UPA)}$	Microprocessor address setup to falling edge of controls[2]	2.5		ns
$t_{h(UPA)}$	Microprocessor address hold from rising edge of controls[2]	2		ns
$t_{su(UPD)}$	Microprocessor data setup to rising edge of controls during writes[2]	12		ns
$t_{h(UPD)}$	Microprocessor data hold from rising edge of controls during writes[2]	2.6		ns
t_h	Microprocessor data output hold from rising edge of controls (read)([5]	0		ns
$t_{d(UP)}$	Microprocessor data output delay from falling edge of controls (read)[2]		36	ns
t_{UPCKL}	Microprocessor control low time[2]	30		ns
t_{UPCKH}	Microprocessor control high time[2]	8.4		ns

(1) Timing is measured from the respective clock at $V_{PAD}/2$ to input or output at $V_{PAD}/2$. Output loading is a 50-Ω transmission line whose delay is calibrated out.
(2) Each part is tested at +90°C case temperature for the given specification. Lots are sample tested at –40°C.
(3) Excluding tx_sync_out, tx_sync_out_[1–5].
(4) Recommended practice.
(5) Controlled by design and process and not directly tested. Verified on initial part evaluation.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
8/07	A	42	Section 5.4	In Table 5.4, removed the *No Connect* designations from ADCCLK, RXCLK, VCOREMON, and GNDMON signals (balls N24, R25, D3, and L24).

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
GC5318IZED	ACTIVE	BGA	ZED	388	40	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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