

FEATURES

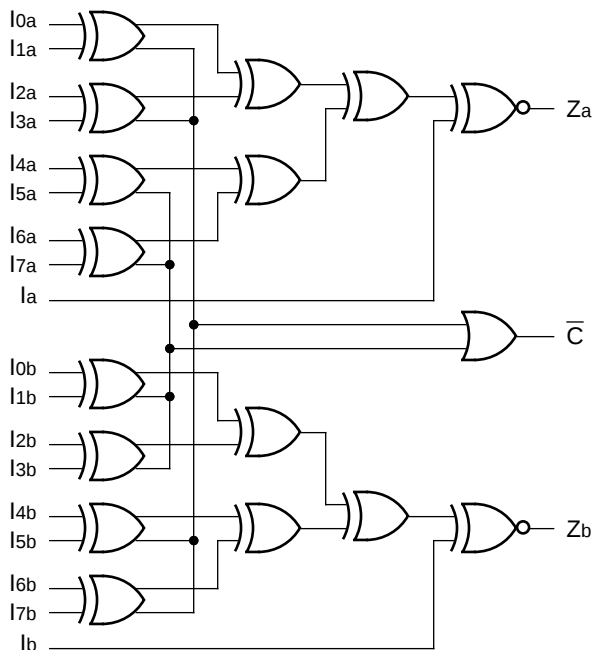
- Max. propagation delay of 2200ps
- IEE min. of -70mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- 15% faster than Fairchild 300K
- Approximately 30% lower power than Fairchild 300K
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

DESCRIPTION

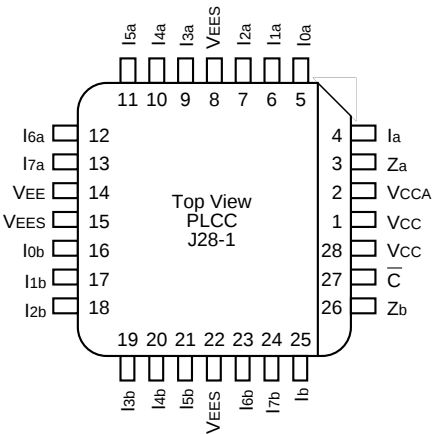
The SY100S360 is a dual parity checker/generator and is designed for use in high-performance ECL systems. The inputs are segmented into two groups of nine inputs each and the parity output is at a logic LOW when an even number of inputs are at a logic HIGH. In each group, one of the nine inputs (Ia, Ib) has a shorter propagation delay and, therefore, is ideal as the expansion input for parity generation of wider data.

A Compare output ($\bar{C}$) is also provided which allows comparison of two 8-bit words. A logic LOW on the $\bar{C}$ output indicates a match. The inputs on this device have 75kΩ pull-down resistors.

BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S360JC	J28-1	Commercial	SY100S360JC	Sn-Pb
SY100S360JCTR ⁽¹⁾	J28-1	Commercial	SY100S360JC	Sn-Pb
SY100S360JZ ⁽²⁾	J28-1	Commercial	SY100S360JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S360JZTR ^(1, 2)	J28-1	Commercial	SY100S360JZ with Pb-Free bar-line indicator	Matte-Sn

- Notes:
- 1. Tape and Reel.
 - 2. Pb-Free package is recommended for new designs.

PIN NAMES

Pin	Function
1a, 1b, 1na, 1nb	Data Inputs (n = 1...7)
Za – Zb	Parity Odd Outputs
C	Compare Output
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

TRUTH TABLE⁽¹⁾

Sum of High Inputs	Output Z
Even	HIGH
Odd	LOW

- Note:
1. Comparator Function:
- $$\overline{C} = (10a \oplus 11a) + (12a \oplus 13a) + (14a \oplus 15a) + (16a \oplus 17a) + (10b \oplus 11b) + (12b \oplus 13b) + (14b \oplus 15b) + (16b \oplus 17b)$$

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

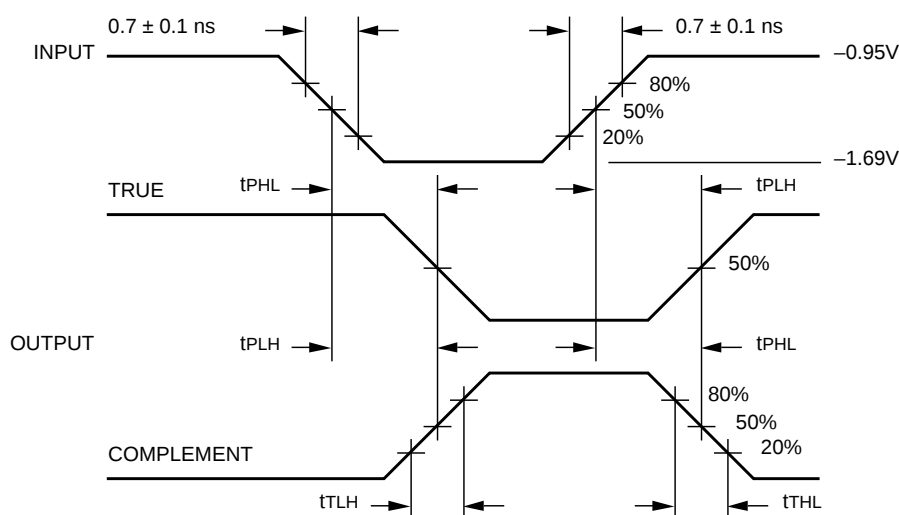
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current I_a, I_b I_{na}, I_{nb}	—	—	300 200	μA	$V_{IN} = V_{IH} (Max.)$
I_{EE}	Power Supply Current	-70	-45	-30	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	500	2200	500	2200	500	2200	ps	
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to $\bar{C}$	500	1700	500	1700	500	1700	ps	
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	300	900	300	900	300	900	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM

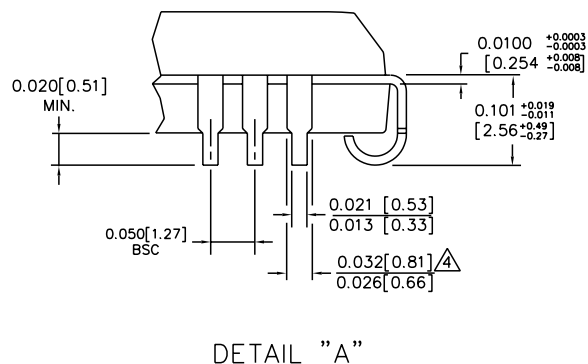
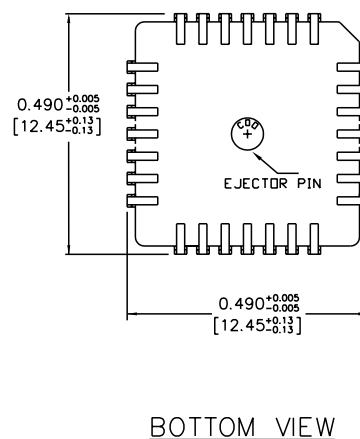
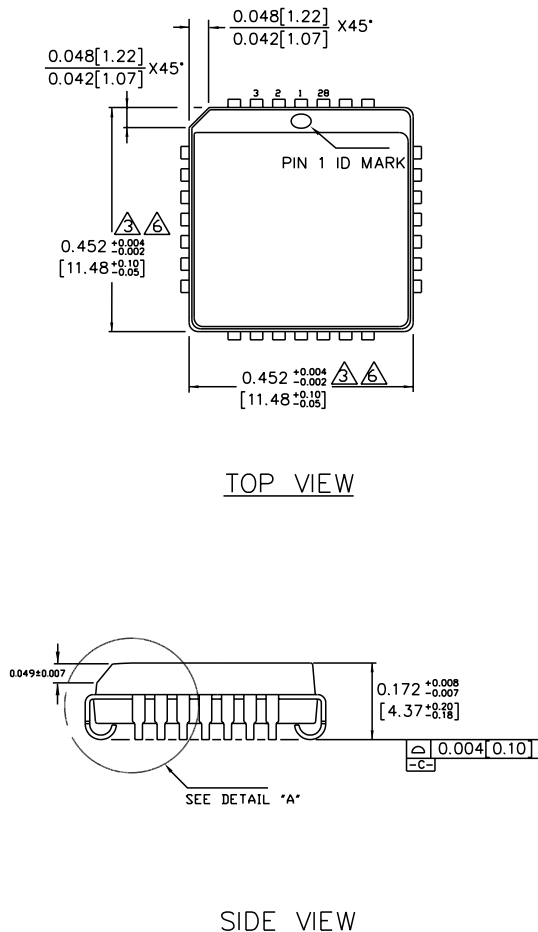


Propagation Delay and Transition Times

NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

28-PIN PLCC (J28-1)



NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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