

FCH35N60

N-Channel SuperFET® MOSFET

600 V, 35 A, 98 mΩ

Features

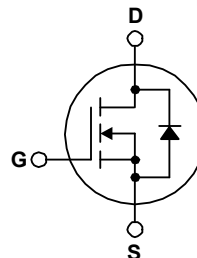
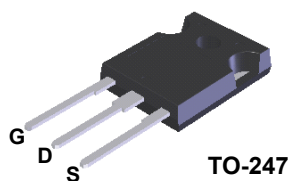
- 650 V @ $T_J = 150^\circ\text{C}$
- $\text{Typ. } R_{DS(on)} = 79 \text{ m}\Omega$
- Ultra Low Gate Charge ($\text{Typ. } Q_g = 139 \text{ nC}$)
- Low Effective Output Capacitance ($\text{Typ. } C_{oss(\text{eff.})} = 340 \text{ pF}$)
- 100% Avalanche Tested

Application

- Solar Inverter
- AC-DC Power Supply

Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCH35N60	Unit
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate-Source voltage	± 30	V
I_D	Drain Current	-Continuous ($T_C = 25^\circ\text{C}$)	A
		-Continuous ($T_C = 100^\circ\text{C}$)	
I_{DM}	Drain Current	- Pulsed (Note 1)	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	mJ
I_{AR}	Avalanche Current	(Note 1)	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	W
		- Derate above 25°C	$W/^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

*Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FCH35N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.4	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	42	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH35N60	FCH35N60	TO-247	-	-	30

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μ A, V _{GS} = 0 V, T _J = 25°C	600	-	-	V
		I _D = 250 μ A, V _{GS} = 0 V, T _J = 150°C	-	650	-	V
Δ BV _{DSS} / Δ T _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μ A, Referenced to 25°C	-	0.6	-	V/°C
BV _{DS}	Drain-Source Avalanche Breakdown Voltage	V _{GS} = 0 V, I _D = 16 A	-	700	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	-	-	1	μ A
		V _{DS} = 480 V, T _C = 125°C	-	-	10	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = $\pm$ 30 V, V _{DS} = 0 V	-	-	$\pm$ 100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μ A	3.0	-	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 17.5 A	-	0.079	0.098	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 17.5 A	-	28.8	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V f = 1 MHz	-	4990	6640	pF
C _{oss}	Output Capacitance		-	2380	3170	pF
C _{rss}	Reverse Transfer Capacitance		-	140	-	pF
C _{oss}	Output Capacitance	V _{DS} = 480 V, V _{GS} = 0 V, f = 1.0 MHz	-	113	-	pF
C _{oss eff.}	Effective Output Capacitance	V _{DS} = 0 V to 480 V, V _{GS} = 0 V	-	340	-	pF
Q _g	Total Gate Charge at 10V	V _{DS} = 480 V, I _D = 35 A V _{GS} = 10 V (Note 4)	-	139	181	nC
Q _{gs}	Gate to Source Gate Charge		-	31	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	69	-	nC
ESR	Equivalent Series Resistance (G-S)	Drain Open, F = 1 MHz	-	1.4	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	V _{DD} = 300 V, I _D = 35 A R _G = 4.7 Ω (Note 4)	-	34	78	ns
t _r	Turn-On Rise Time		-	120	250	ns
t _{d(off)}	Turn-Off Delay Time		-	105	220	ns
t _f	Turn-Off Fall Time		-	73	155	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	35	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	105	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 35 A	-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 35 A dI _F /dt = 100 A/μs	-	614	-	ns
Q _{rr}	Reverse Recovery Charge		-	16.3	-	μC

Notes:

- 1: Repetitive Rating: Pulse-width limited by maximum junction temperature.
- 2: I_{AS} = 17.5 A, V_{DD} = 50 V, R_G = 25 Ω , starting T_J = 25°C
- 3: I_{SD} $\leq$ 35 A, di/dt $\leq$ 200 A/ μ s, V_{DD} $\leq$ BV_{DSS}, starting T_J = 25°C
- 4: Essentially independent of operating temperature.

Typical Characteristics

Figure 1. On-Region Characteristics

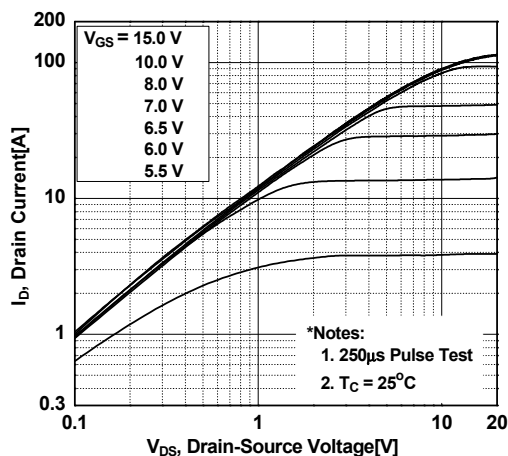


Figure 2. Transfer Characteristics

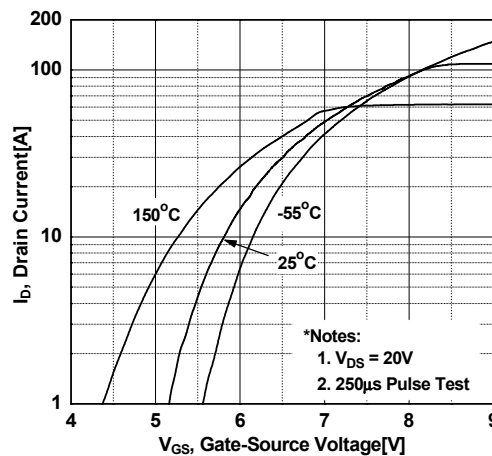


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

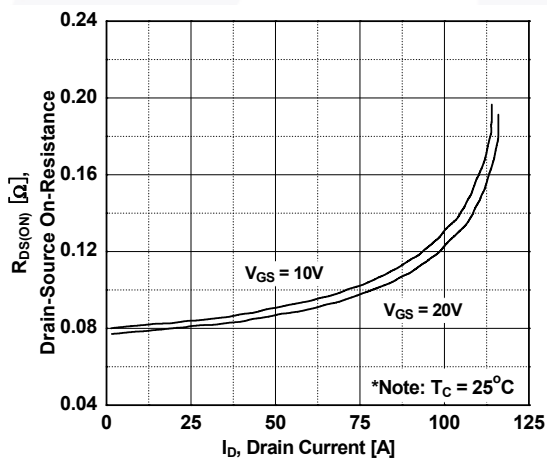


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

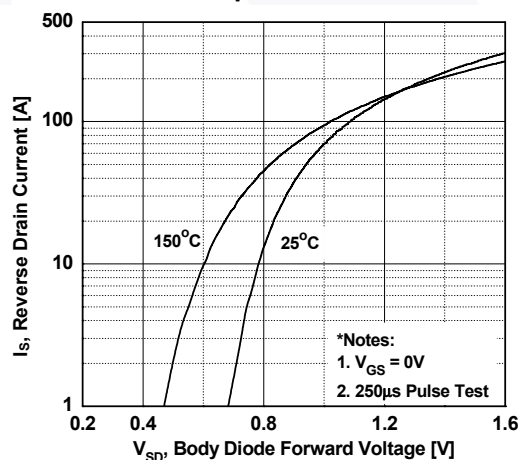


Figure 5. Capacitance Characteristics

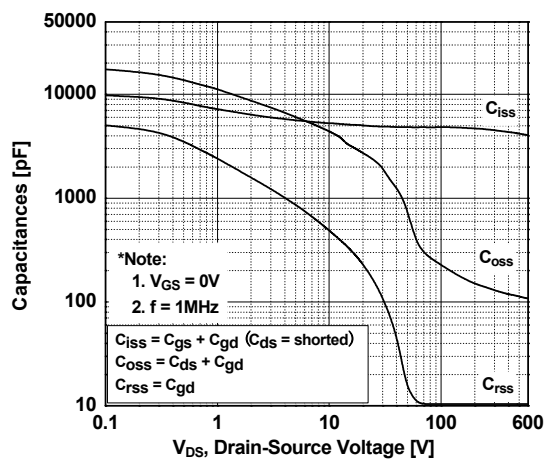
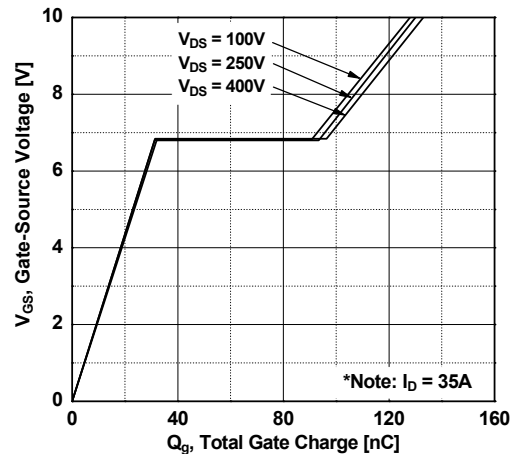


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

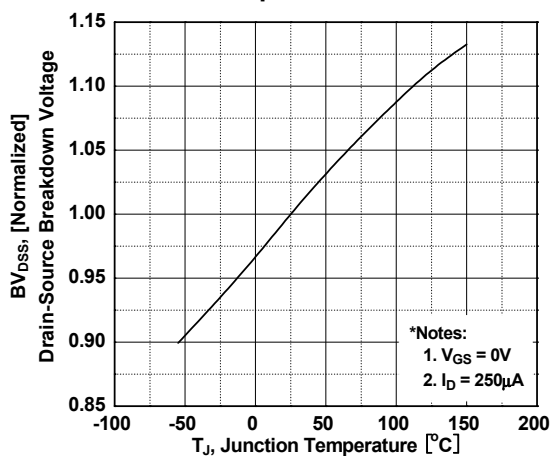


Figure 8. On-Resistance Variation vs. Temperature

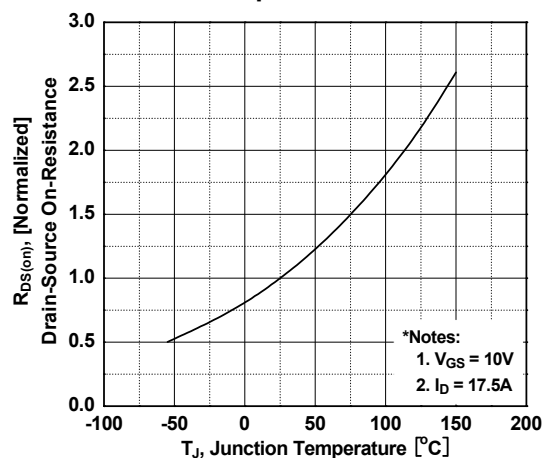


Figure 9. Maximum Safe Operating Area

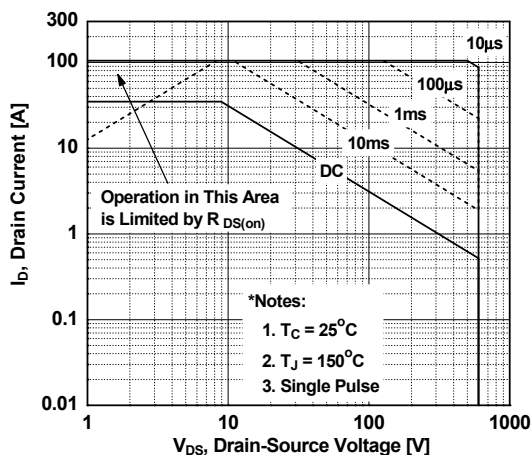


Figure 10. Maximum Drain Current vs. Case Temperature

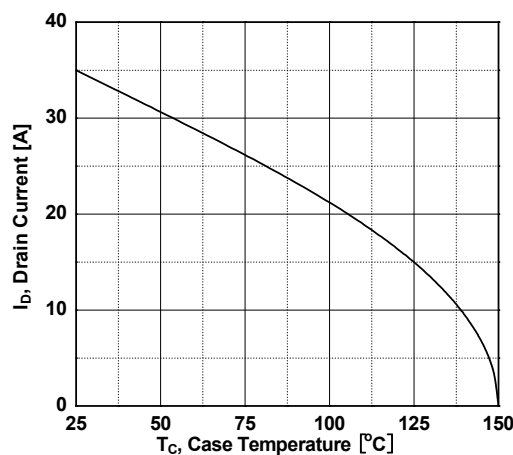


Figure 11. Transient Thermal Response Curve

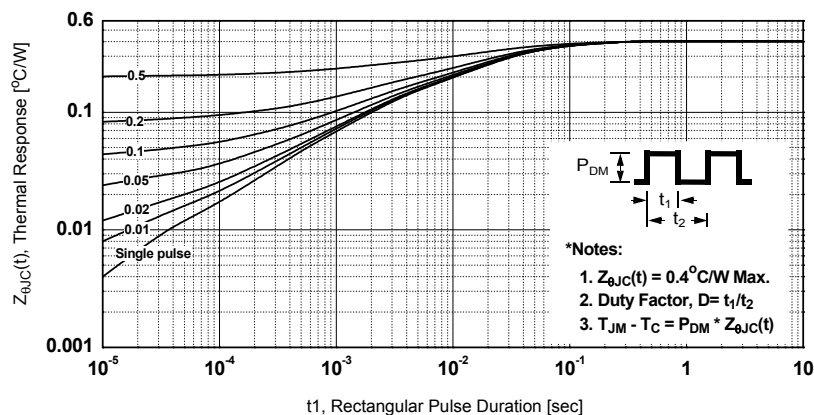


Figure 12. Gate Charge Test Circuit & Waveform

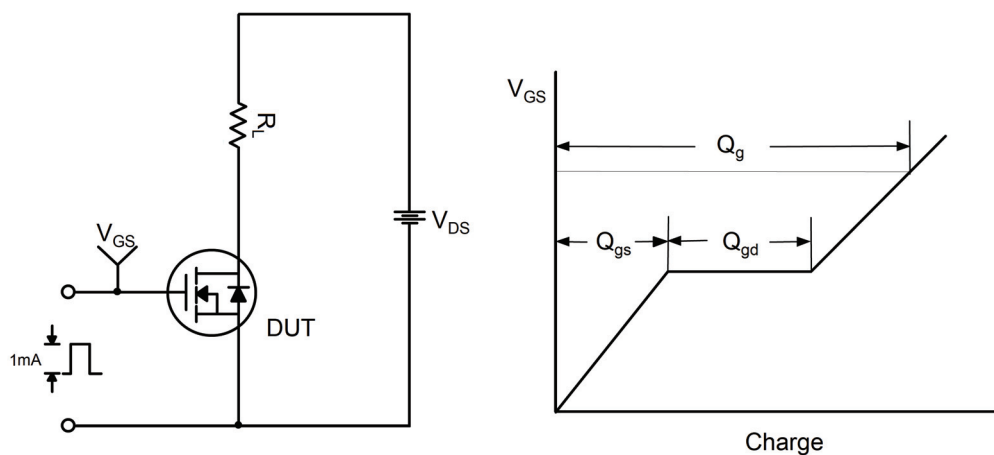


Figure 13. Resistive Switching Test Circuit & Waveforms

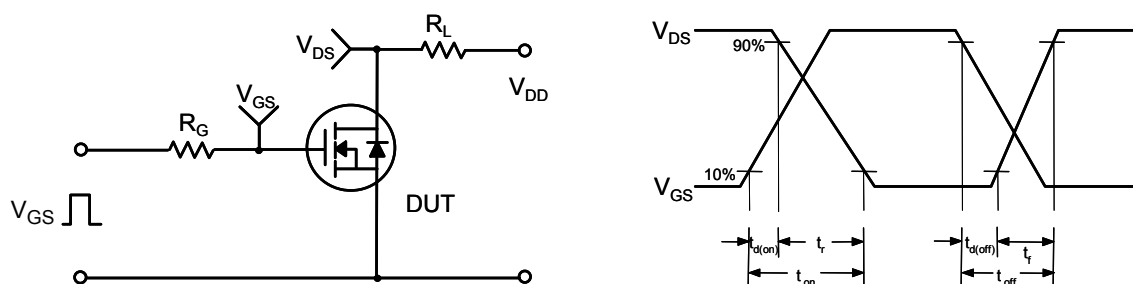


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

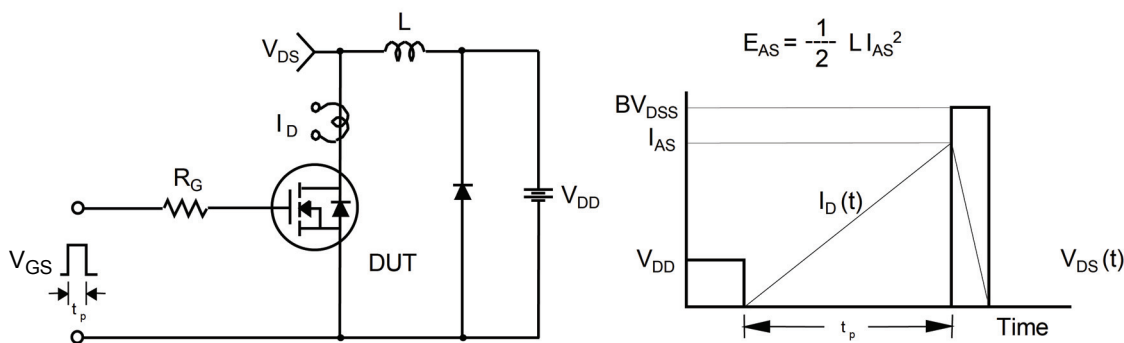
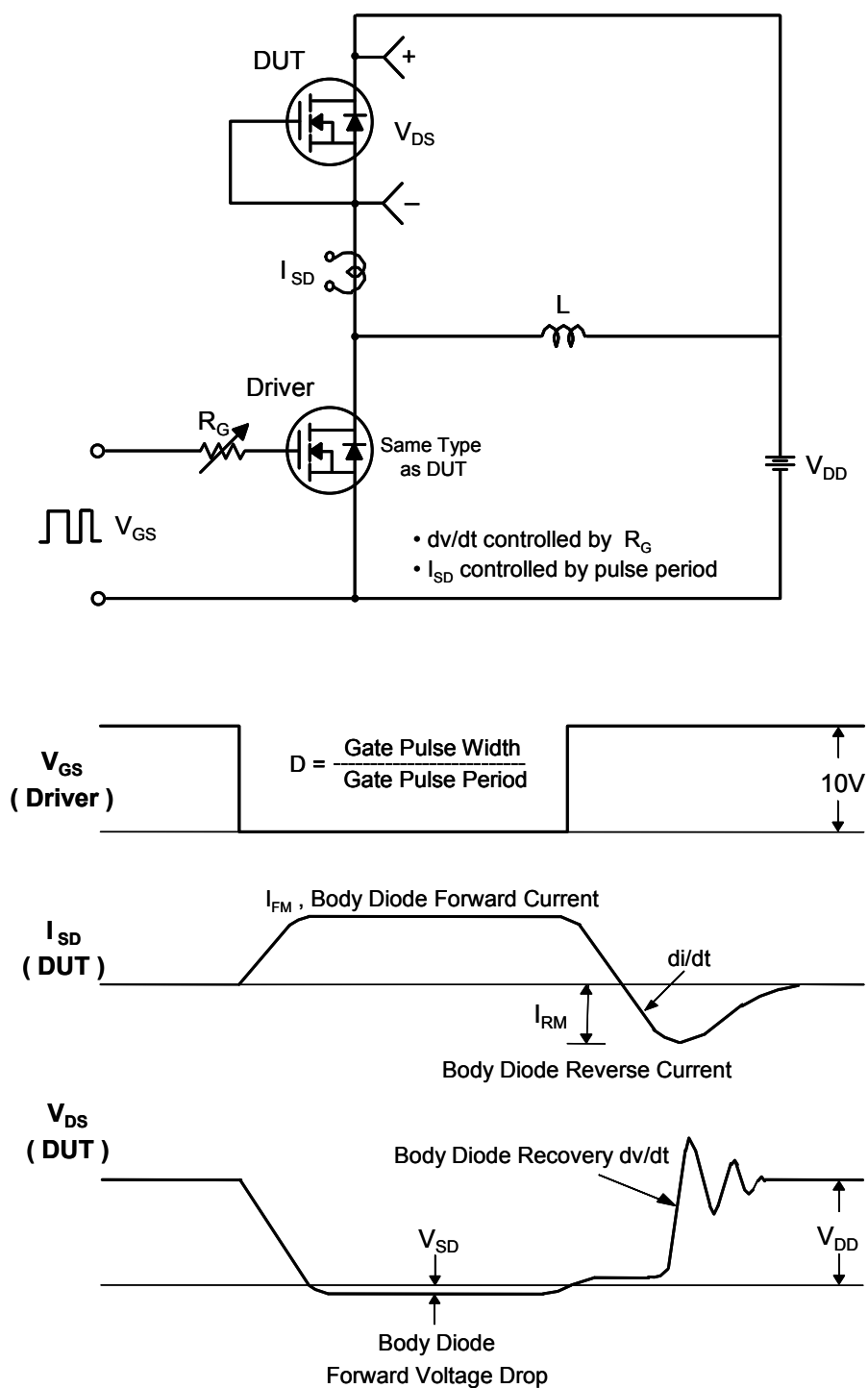
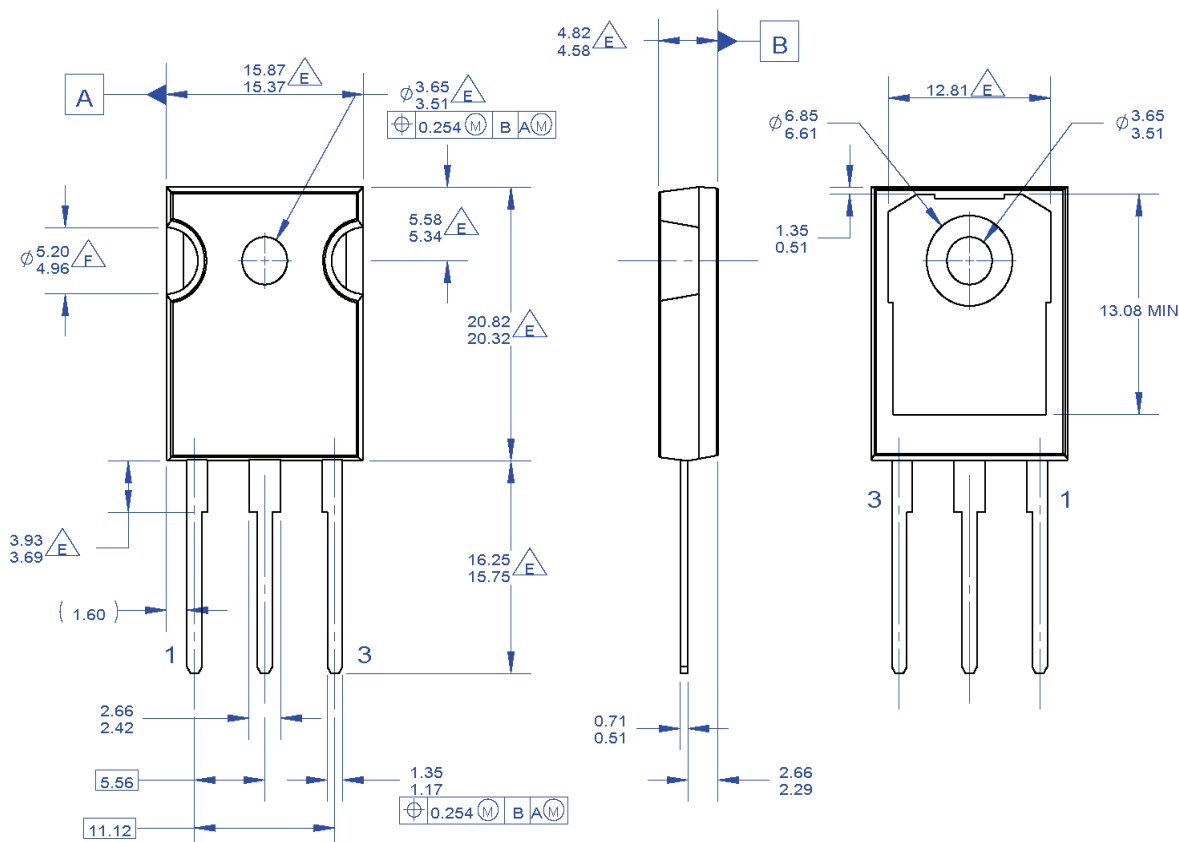


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-247 3L



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

$\triangle E$ DOES NOT COMPLY JEDEC STANDARD VALUE

$\triangle F$ NOTCH MAY BE SQUARE

G. DRAWING FILENAME: MKT-TO247A03_REV03

Figure ... TO-247, Molded, 3 Lead, Jedec Variation AB

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