

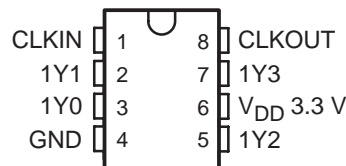
# CDCVF2505

## 3.3-V CLOCK PHASE-LOCK LOOP CLOCK DRIVER

SCAS640E – JULY 2000 – REVISED MARCH 2005

- Phase-Lock Loop Clock Driver for Synchronous DRAM and General-Purpose Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 24 MHz to 200 MHz
- Low Jitter (Cycle-cycle):  $<|150\text{ ps}|$  Over the Range 66 MHz–200 MHz
- Distributes One Clock Input to One Bank of Five Outputs (CLKOUT Is Used to Tune the Input-Output Delay)
- Three-States Outputs When There Is no Input Clock
- Operates From Single 3.3-V Supply
- Available in 8-Pin TSSOP and 8-Pin SOIC Packages
- Consumes Less Than 100  $\mu\text{A}$  (Typically) in Power Down Mode
- Internal Feedback Loop Is Used to Synchronize the Outputs to the Input Clock
- 25- $\Omega$  On-Chip Series Damping Resistors
- Integrated RC PLL Loop Filter Eliminates the Need for External Components

D OR PW PACKAGE  
(TOP VIEW)



### description

The CDCVF2505 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the output clocks (1Y[0–3] and CLKOUT) to the input clock signal (CLKIN). The CDCVF2505 operates at 3.3 V. It also provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of five outputs provides low-skew, low-jitter copies of CLKIN. Output duty cycles are adjusted to 50 percent, independent of duty cycle at CLKIN. The device automatically goes in power-down mode when no input signal is applied to CLKIN.

Unlike many products containing PLLs, the CDCVF2505 does not require an external RC network. The loop filter for the PLLs is included on-chip, minimizing component count, space, and cost.

Because it is based on the PLL circuitry, the CDCVF2505 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN, and following any changes to the PLL reference.

The CDCVF2505 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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CDCVF2505  
3.3-V CLOCK PHASE-LOCK LOOP CLOCK DRIVER

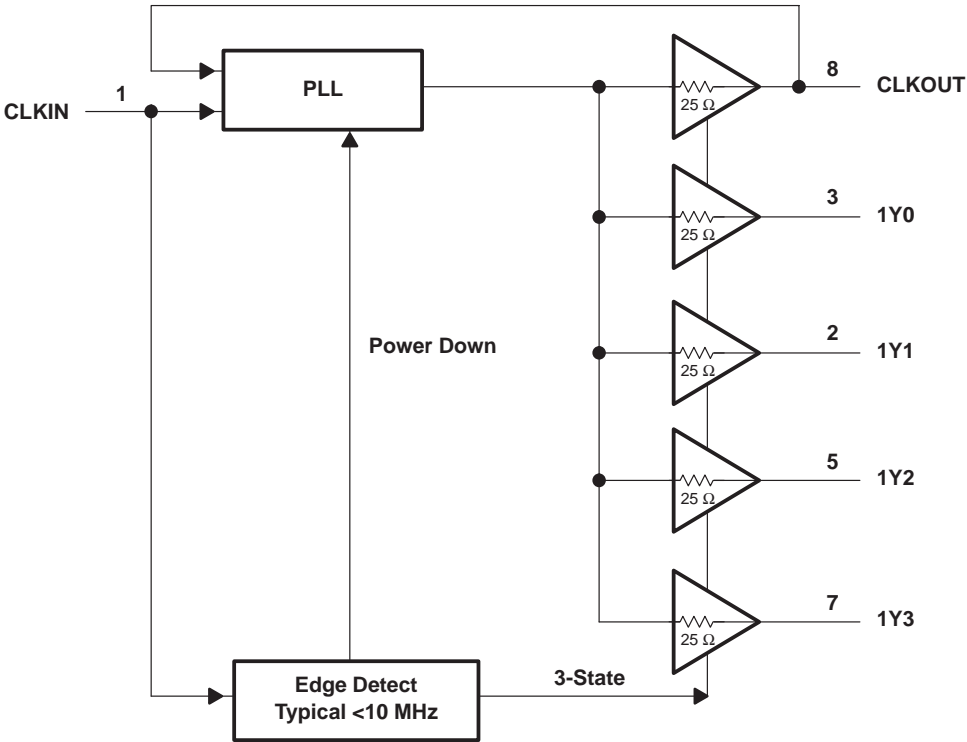
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FUNCTION TABLE

INPUT	OUTPUTS	
	1Y (0:3)	CLKOUT
L	L	L
H	H	H
<10 MHz†	Z	Z

† Typically, below 2 MHz the device goes in power-down mode in which the PLL is turned off and the outputs enter into Hi-Z mode. If a >10-MHz signal is applied at CLKIN the PLL turns on, reacquires lock, and stabilizes after approximately 100 μs. The outputs will then be enabled.

functional block diagram



# CDCVF2505

## 3.3-V CLOCK PHASE-LOCK LOOP CLOCK DRIVER

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### Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
1Y[0–3]	2, 3, 5, 7	O	Clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25- $\Omega$ series damping resistor.
CLKIN	1	I	Clock input. CLKIN provides the clock signal to be distributed by the CDCVF2505 clock driver. CLKIN is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid signal is applied, a stabilization time (100 $\mu$ s) is required for the PLL to phase lock the feedback signal to CLKIN.
CLKOUT	8	O	Feedback output. CLKOUT completes the internal feedback loop of the PLL. This connection is made inside the chip and an external feedback loop should NOT be connected. CLKOUT can be loaded with a capacitor to achieve zero delay between CLKIN and the Y outputs.
GND	4	Power	Ground
V <sub>DD</sub> 3.3V	6	Power	3.3-V Supply

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>DD</sub>	–0.5 V to 4.3 V
Input voltage range, V <sub>I</sub> (see Notes 1 and 2)	–0.5 V to V <sub>DD</sub> + 0.5 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	–0.5 V to V <sub>DD</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DD</sub> )	±50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DD</sub> )	±50 mA
Continuous total output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>DD</sub> )	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package	165.5°C/W
PWR package	230.5°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This value is limited to 4.3 V maximum.  
3. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>DD</sub>	3	3.3	3.6	V
High-level input voltage, V <sub>IH</sub>	0.7 V <sub>DD</sub>			V
Low-level input voltage, V <sub>IL</sub>		0.3 V <sub>DD</sub>		V
Input voltage, V <sub>I</sub>	0	V <sub>DD</sub>		V
High-level output current, I <sub>OH</sub>			–12	mA
Low-level output current, I <sub>OL</sub>			12	mA
Operating free-air temperature, T <sub>A</sub>	–40		85	°C



# CDCVF2505

## 3.3-V CLOCK PHASE-LOCK LOOP CLOCK DRIVER

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### timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	NOM	MAX	UNIT
$f_{clk}$	Clock frequency	24		200	MHz
Input clock duty cycle	24 MHz – 85 MHz (see Note 4)	30%		85%	
	86 MHz – 200 MHz	40%	50%	60%	
Stabilization time (see Note 5)				100	$\mu$ s

NOTES: 4. Ensured by design but not 100% production tested.

5. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{DD}$	MIN	TYP <sup>†</sup>	MAX	UNIT
$V_{IK}$	Input voltage	$I_I = -18$ mA	3 V		-1.2	V
$V_{OH}$	High-level output voltage	$I_{OH} = -100$ $\mu$ A	MIN to MAX	$V_{DD}-0.2$		V
		$I_{OH} = -12$ mA	3 V	2.1		
		$I_{OH} = -6$ mA	3 V	2.4		
$V_{OL}$	Low-level output voltage	$I_{OL} = 100$ $\mu$ A	MIN to MAX		0.2	V
		$I_{OL} = 12$ mA	3 V		0.8	
		$I_{OL} = 6$ mA	3 V		0.55	
$I_{OH}$	High-level output current	$V_O = 1$ V	3 V	-27		mA
		$V_O = 1.65$ V	3.3 V	-36		
$I_{OL}$	Low-level output current	$V_O = 2$ V	3 V	27		mA
		$V_O = 1.65$ V	3.3 V	40		
$I_I$	Input current	$V_I = 0$ V or $V_{DD}$			$\pm 5$	$\mu$ A
$C_i$	Input capacitance	$V_I = 0$ V or $V_{DD}$	3.3 V	4.2		pF
$C_o$	Output capacitance	$V_I = 0$ V or $V_{DD}$	3.3 V		2.8	pF
					5.2	

<sup>†</sup> All typical values are at respective nominal  $V_{DD}$  and 25°C.

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 25$ pF, $V_{DD} = 3.3$ V $\pm$ 0.3 V (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>†</sup>	MAX	UNIT
$t_{pd}$	Propagation delay (normalized (see Figure 3))	CLKIN to Yn, $f = 66$ MHz to 200 MHz	-150	150	ps
$t_{sk(o)}$	Output skew (see Note 6)	Yn to Yn		150	ps
$t_{c(jit\_cc)}$	Jitter (cycle to cycle) (see Figure 5)	$f = 66$ MHz to 200 MHz	70	150	ps
		$f = 24$ MHz to 50 MHz	200	400	
odc	Output duty cycle (see Figure 4)	$f = 24$ MHz to 200 MHz at 50% $V_{DD}$	45%	55%	
$t_r$	Rise time	$V_O = 0.4$ V to 2 V	0.5	2	ns
$t_f$	Fall time	$V_O = 2$ V to 0.4 V	0.5	2	ns

<sup>†</sup> All typical values are at respective nominal  $V_{DD}$  and 25°C.

NOTE 6: The  $t_{sk(o)}$  specification is only valid for equal loading of all outputs.



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# CDCVF2505

## 3.3-V CLOCK PHASE-LOCK LOOP CLOCK DRIVER

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### ESD information

ESD MODELS	LIMIT
Human Body Model (HBM)	2.0 kV
Machine Model (MM)	300 V
Charge Device Model (CDM)	1 kV

### thermal information

CDCVF2505 8-PIN SOIC			THERMAL AIR FLOW (CFM)				UNIT
			0	150	250	500	
R <sub>θJA</sub>	High K		97	87	83	77	°C/W
R <sub>θJA</sub>	Low K		165	126	113	97	°C/W
R <sub>θJC</sub>	High K	39					°C/W
R <sub>θJC</sub>	Low K	42					°C/W

CDCVF2505 8-PIN TSSOP			THERMAL AIR FLOW (CFM)				UNIT
			0	150	250	500	
R <sub>θJA</sub>	High K		149	142	138	132	°C/W
R <sub>θJA</sub>	Low K		230	185	170	150	°C/W
R <sub>θJC</sub>	High K	65					°C/W
R <sub>θJC</sub>	Low K	69					°C/W

### TYPICAL CHARACTERISTICS

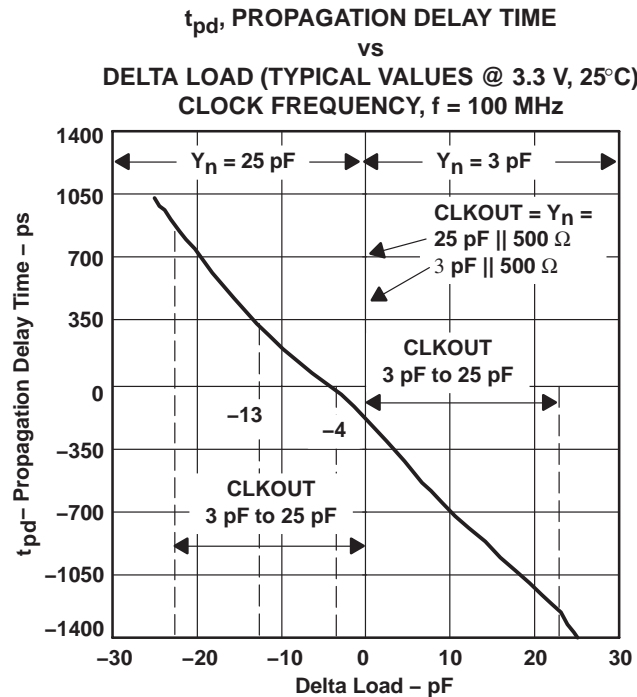


Figure 1

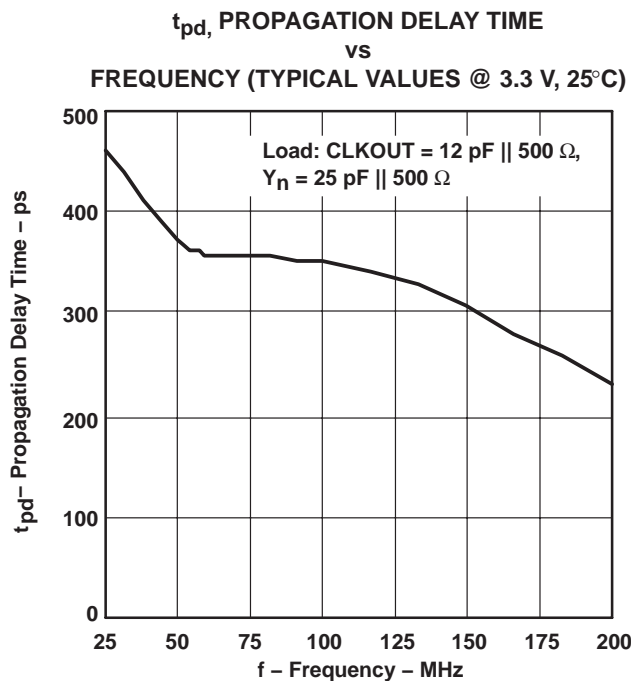


Figure 2

NOTE: Delta Load = CLKOUT Load – Yn Load

# CDCVF2505

## 3.3-V CLOCK PHASE-LOCK LOOP CLOCK DRIVER

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### TYPICAL CHARACTERISTICS

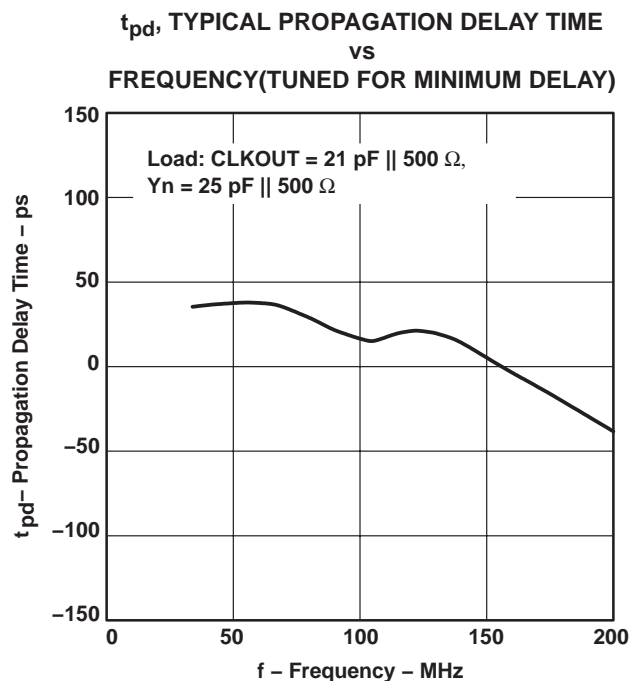


Figure 3

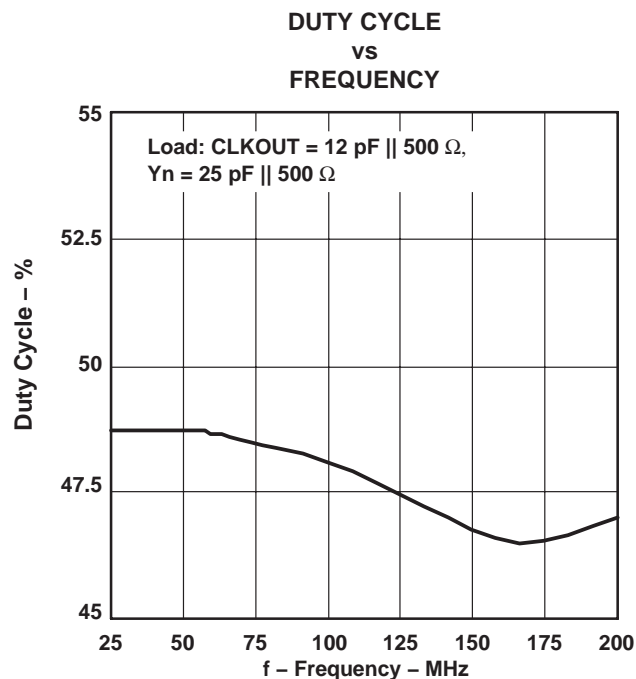


Figure 4

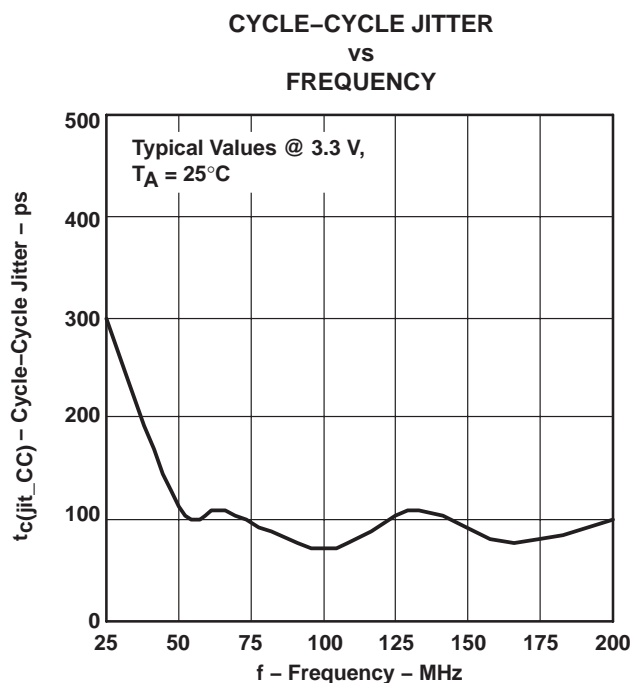


Figure 5

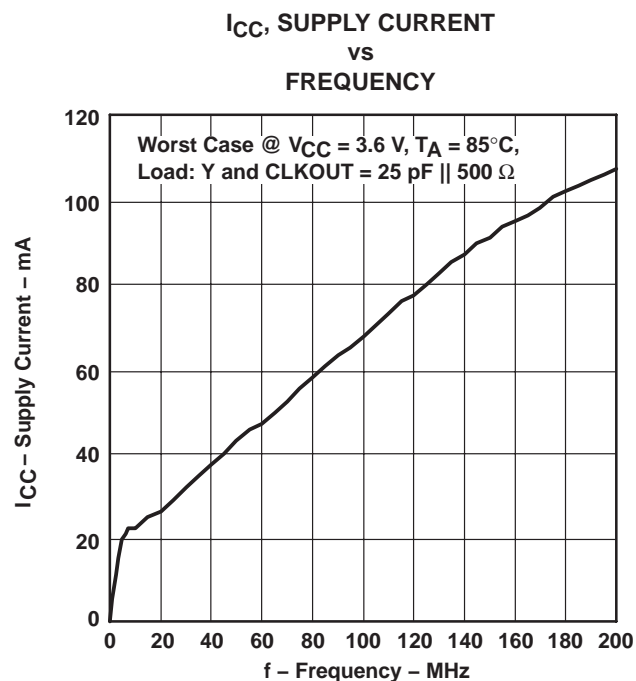
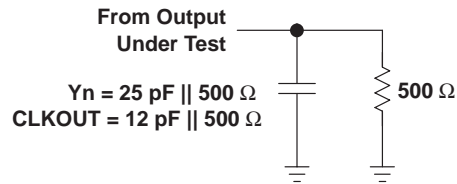
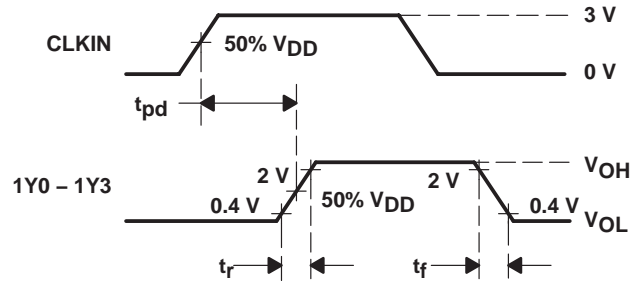


Figure 6

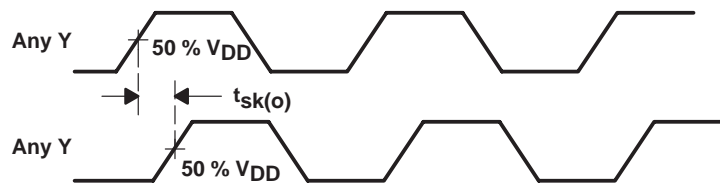
## PARAMETER MEASUREMENT INFORMATION



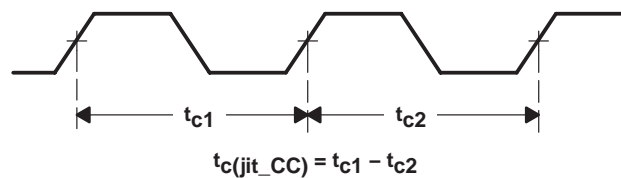
**Figure 7. Test Load Circuit**



**Figure 8. Voltage Threshold for Measurements, Propagation Delay ( $t_{pd}$ )**



**Figure 9. Output Skew**



**Figure 10. Cycle-to-Cycle Jitter**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCVF2505D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV05	<a href="#">Samples</a>
CDCVF2505DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV05	<a href="#">Samples</a>
CDCVF2505DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV05	<a href="#">Samples</a>
CDCVF2505DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV05	<a href="#">Samples</a>
CDCVF2505PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV05	<a href="#">Samples</a>
CDCVF2505PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV05	<a href="#">Samples</a>
CDCVF2505PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV05	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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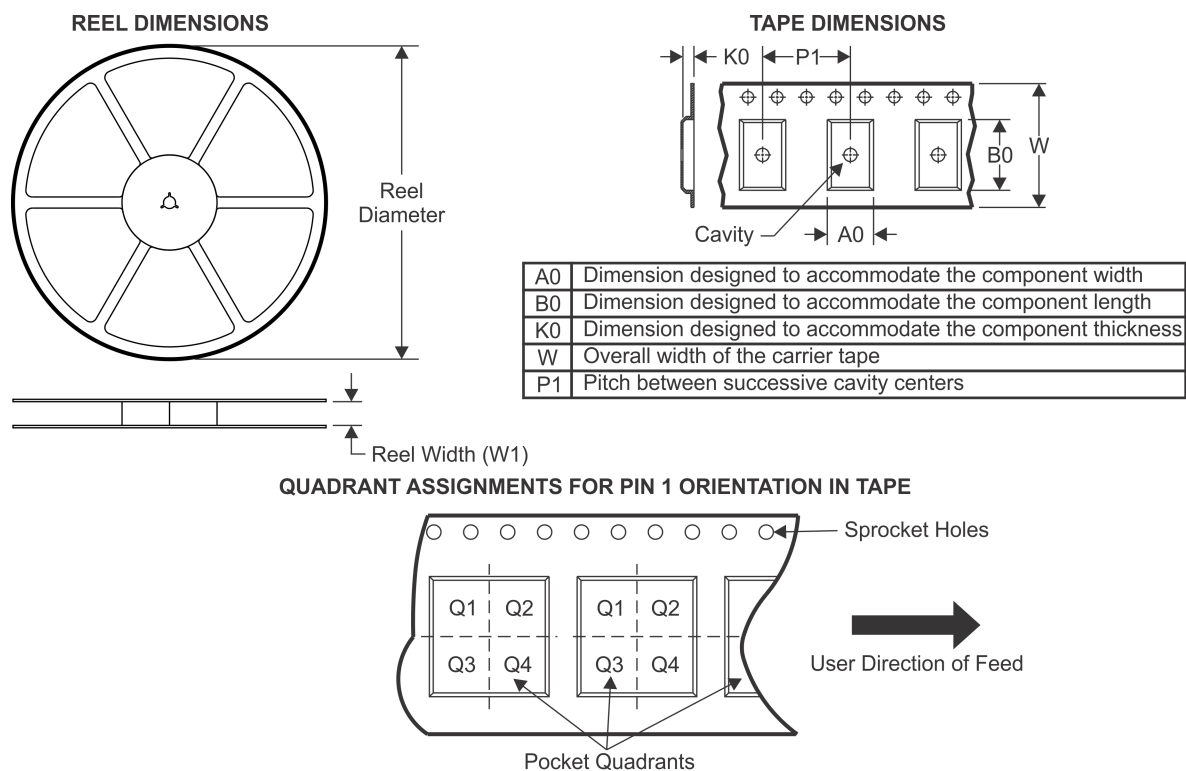
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**OTHER QUALIFIED VERSIONS OF CDCVF2505 :**

- Automotive: [CDCVF2505-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF2505DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
CDCVF2505PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

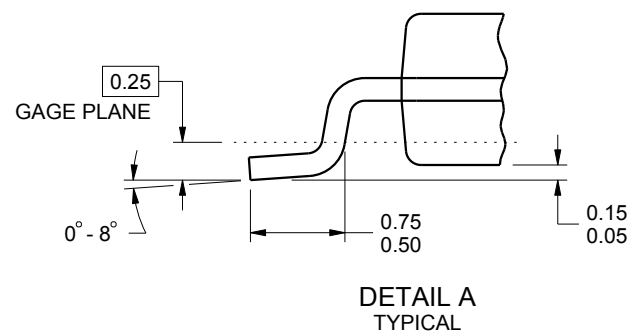
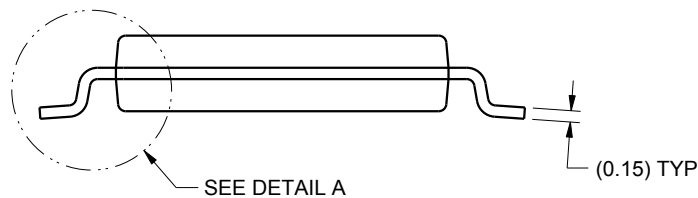
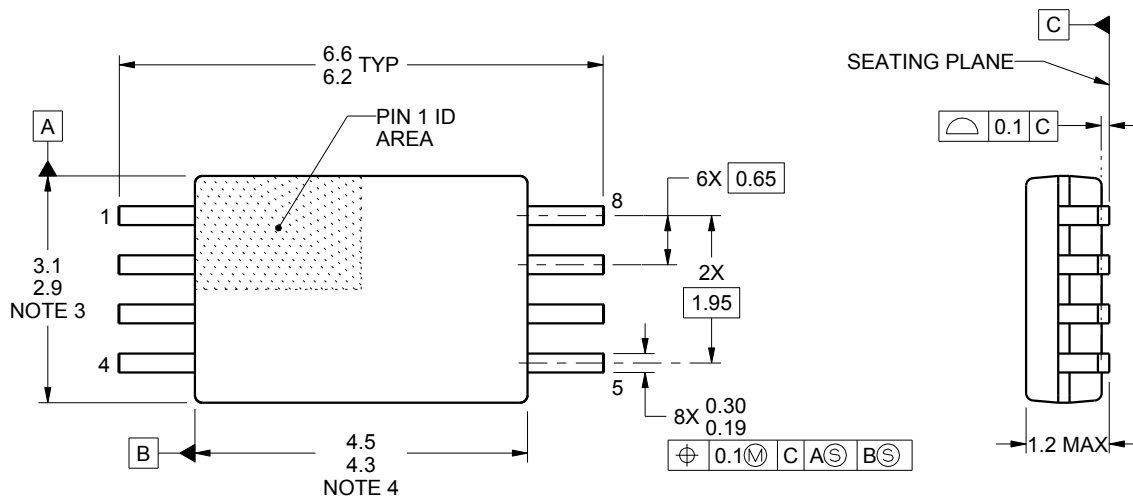
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF2505DR	SOIC	D	8	2500	367.0	367.0	35.0
CDCVF2505PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

**PW0008A**

## PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

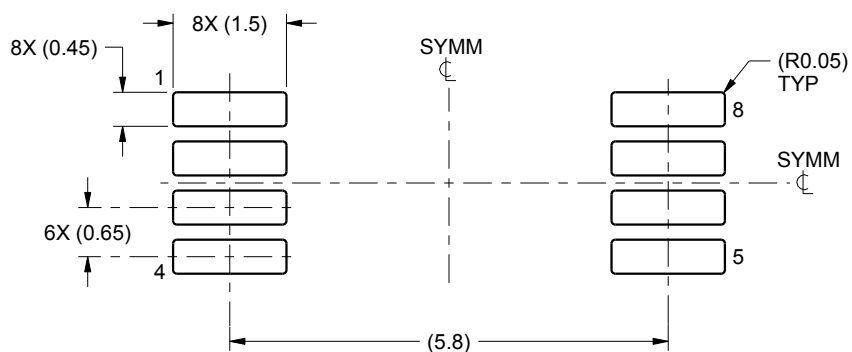
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

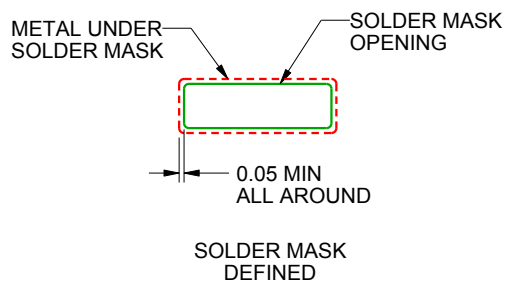
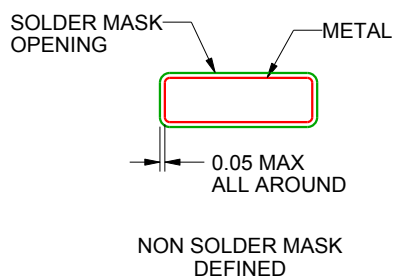
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

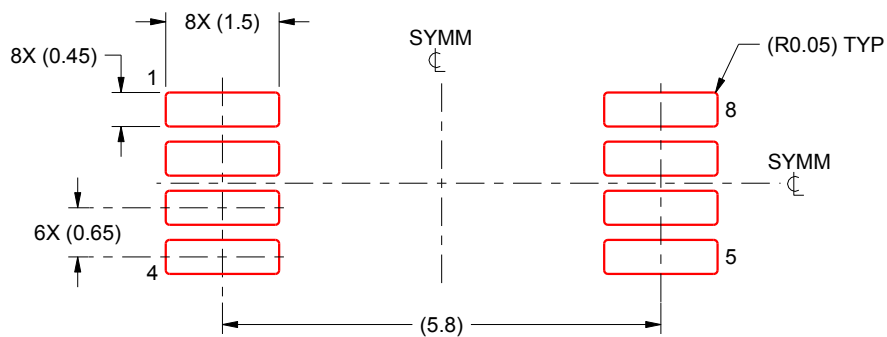
6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**PW0008A**

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

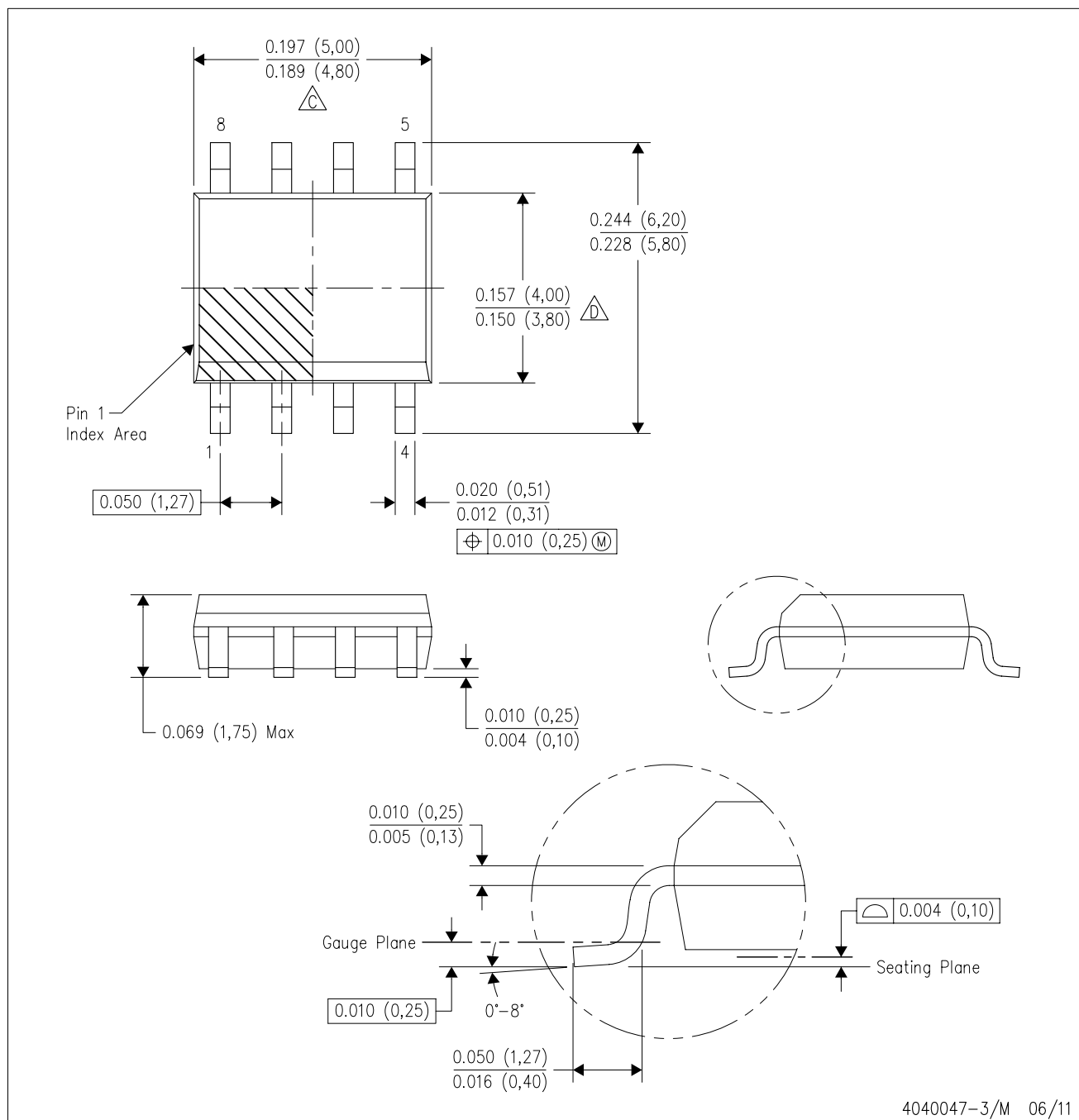
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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G8)

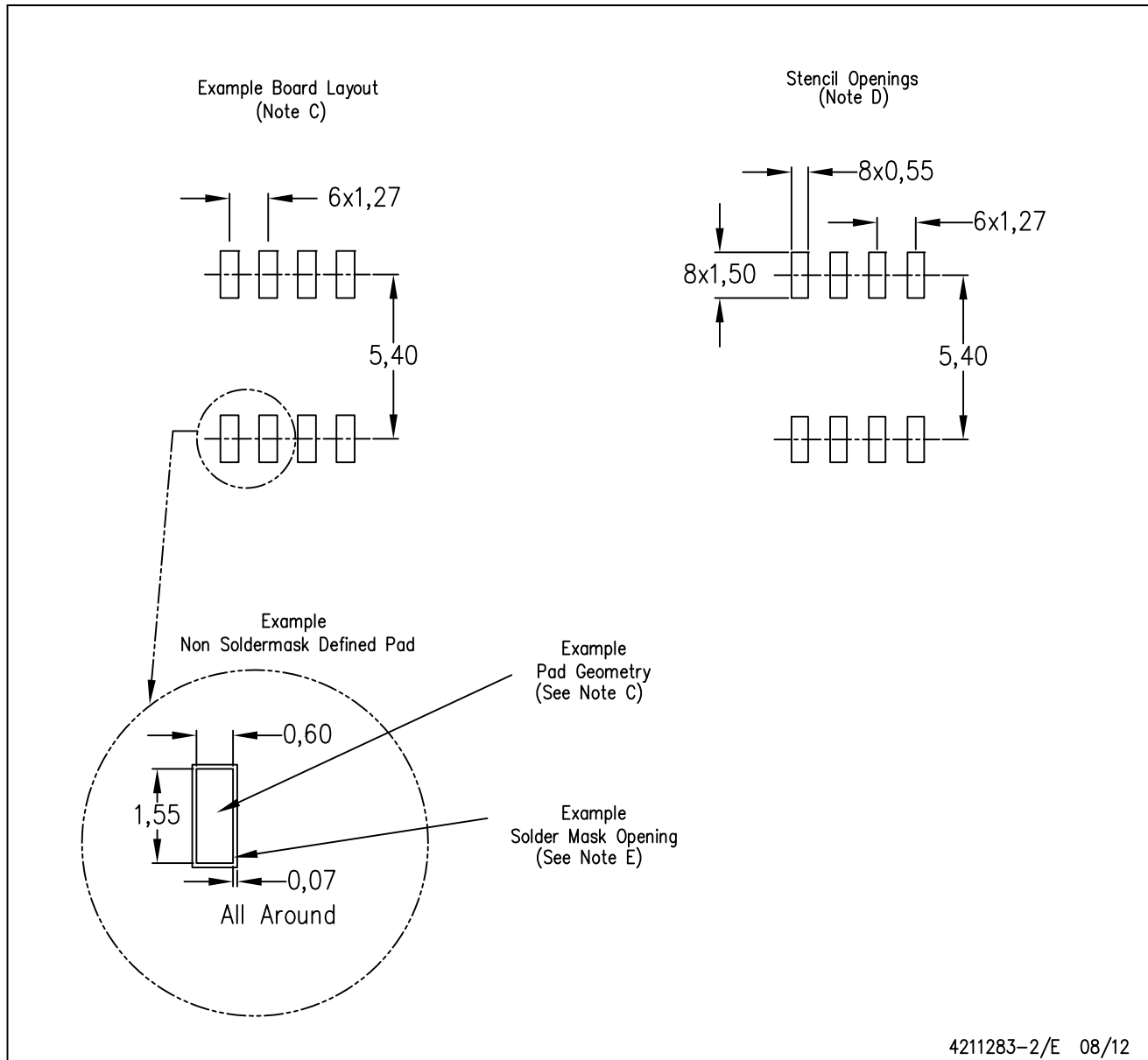
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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