



0.05 $\mu\text{V}/^\circ\text{C}$ max, SINGLE-SUPPLY CMOS OPERATIONAL AMPLIFIERS Zero-Drift Series

FEATURES

- **LOW OFFSET VOLTAGE:** 5 μV (max)
- **ZERO DRIFT:** 0.05 $\mu\text{V}/^\circ\text{C}$ (max)
- **QUIESCENT CURRENT:** 285 μA
- **SINGLE-SUPPLY OPERATION**
- **SINGLE AND DUAL VERSIONS**
- **SHUTDOWN**
- **MicroSIZED PACKAGES**

APPLICATIONS

- **TRANSDUCER APPLICATIONS**
- **TEMPERATURE MEASUREMENT**
- **ELECTRONIC SCALES**
- **MEDICAL INSTRUMENTATION**
- **BATTERY-POWERED INSTRUMENTS**
- **HANDHELD TEST EQUIPMENT**

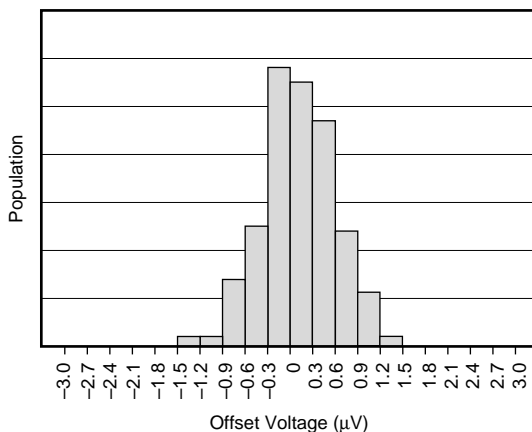
DESCRIPTION

The OPA334 and OPA335 series of CMOS operational amplifiers use auto-zeroing techniques to simultaneously provide very low offset voltage (5 μV max), and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high input impedance and rail-to-rail output swing. Single or dual supplies as low as +2.7V ($\pm 1.35\text{V}$) and up to +5.5V ($\pm 2.75\text{V}$) may be used. These op amps are optimized for low-voltage, single-supply operation.

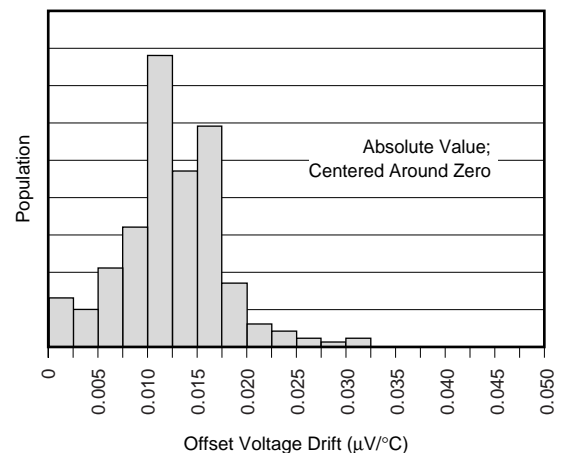
The OPA334 family includes a shutdown mode. Under logic control, the amplifiers can be switched from normal operation to a standby current of 2 μA . When the Enable pin is connected high, the amplifier is active. Connecting Enable low disables the amplifier, and places the output in a high-impedance state.

The OPA334 (single version with shutdown) comes in *MicroSIZED* SOT23-6. The OPA335 (single version without shutdown) is available in SOT23-5, and SO-8. The OPA2334 (dual version with shutdown) comes in *MicroSIZED* MSOP-10. The OPA2335 (dual version without shutdown) is offered in the MSOP-8 and SO-8 packages. All versions are specified for operation from -40°C to $+125^\circ\text{C}$.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION



OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage	+7V
Signal Input Terminals, Voltage ⁽²⁾	-0.5V to (V+) + 0.5V
Current ⁽²⁾	±10mA
Output Short Circuit ⁽³⁾	Continuous
Operating Temperature	-40°C to +150°C
Storage Temperature	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these, or any other conditions beyond those specified, is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

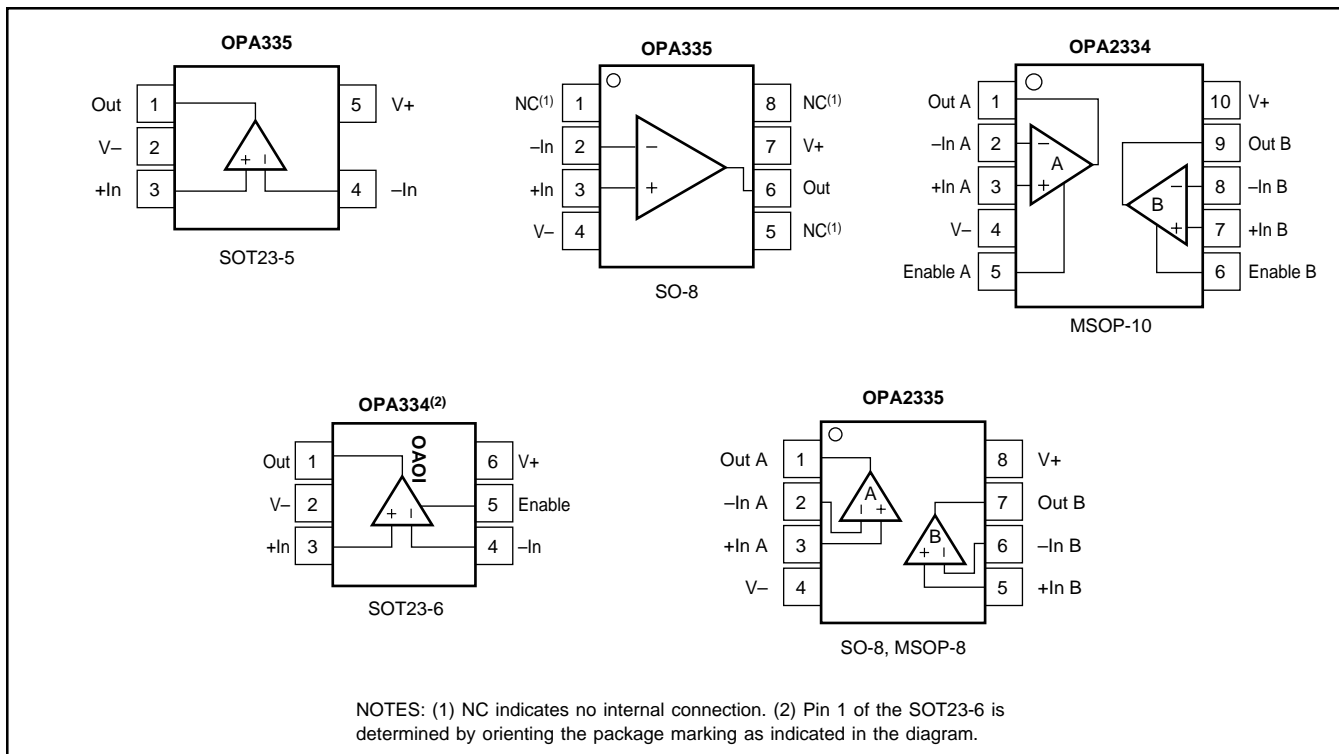
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR ⁽¹⁾	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Shutdown Version						
OPA334	SOT23-6	DBV	-40°C to +125°C	OA0I	OPA334AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA334AIDBVR	Tape and Reel, 3000
OPA2334	MSOP-10	DGS	-40°C to +125°C	BHE	OPA2334AIDGST	Tape and Reel, 250
"	"	"	"	"	OPA2334AIDGSR	Tape and Reel, 2500
Non-Shutdown Version						
OPA335	SOT23-5	DBV	-40°C to +125°C	OAPI	OPA335AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA335AIDBVR	Tape and Reel, 3000
OPA335	SO-8	D	-40°C to +125°C	OPA335	OPA335AID	Rails, 100
"	"	"	"	"	OPA335AIDR	Tape and Reel, 2500
OPA2335	SO-8	D	-40°C to +125°C	OPA2335	OPA2335AID	Rails, 100
"	"	"	"	"	OPA2335AIDR	Tape and Reel, 2500
OPA2335	MSOP-8	DGK	-40°C to +125°C	BHF	OPA2335AIDGKT	Tape and Reel, 250
"	"	"	"	"	OPA2335AIDGKR	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATIONS



ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

At $T_A = +25^{\circ}\text{C}$, $V_S = +5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

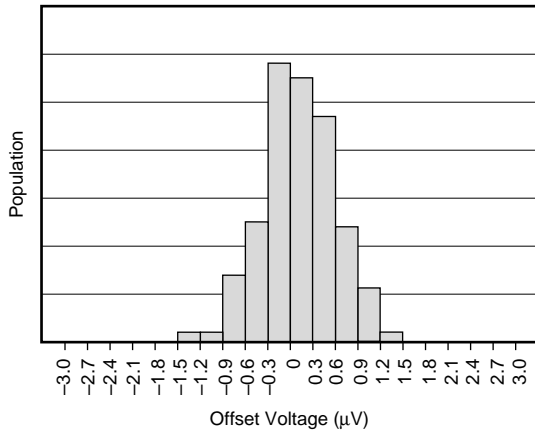
PARAMETER	CONDITION	OPA334AI, OPA335AI OPA2334AI, OPA2335AI			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature vs Power Supply Long-Term Stability ⁽¹⁾ Channel Separation, dc	V_{OS} dV_{OS}/dT PSRR $V_{CM} = V_S/2$ $V_S = +2.7\text{V}$ to $+5.5\text{V}$, $V_{CM} = 0$, Over Temperature		1 ± 0.02 ± 1 See Note (1) 0.1	5 ± 0.05 ± 2	μV $\mu\text{V}/^{\circ}\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{V}$
INPUT BIAS CURRENT Input Bias Current Over Temperature Input Offset Current	I_B $V_{CM} = V_S/2$ I_{OS}		± 70 1 ± 120	± 200 ± 400	pA nA pA
NOISE Input Voltage Noise, $f = 0.01\text{Hz}$ to 10Hz Input Current Noise Density, $f = 10\text{Hz}$	e_n i_n		1.4 20		μV_{PP} $\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Ratio	V_{CM} CMRR $(V^-) - 0.1\text{V} < V_{CM} < (V^+) - 1.5\text{V}$, Over Temperature	$(V^-) - 0.1$ 110	130	$(V^+) - 1.5$	V dB
INPUT CAPACITANCE Differential Common-Mode			1 5		pF pF
OPEN-LOOP GAIN Open-Loop Voltage Gain, Over Temperature Over Temperature	$50\text{mV} < V_O < (V^+) - 50\text{mV}$, $R_L = 100\text{k}\Omega$, $V_{CM} = V_S/2$ $100\text{mV} < V_O < (V^+) - 100\text{mV}$, $R_L = 10\text{k}\Omega$, $V_{CM} = V_S/2$	110 110	130 130		dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate	GBW SR $G = +1$		2 1.6		MHz $\text{V}/\mu\text{s}$
OUTPUT Voltage Output Swing from Rail Voltage Output Swing from Rail Short-Circuit Current Capacitive Load Drive	$R_L = 10\text{k}\Omega$, Over Temperature $R_L = 100\text{k}\Omega$, Over Temperature I_{SC} C_{LOAD}		15 1 ± 50	100 50	mV mV mA
SHUTDOWN t_{OFF} $t_{ON}^{(2)}$ V_L (shutdown) V_H (amplifier is active) Input Bias Current of Enable Pin I_{QSD}		0 0.75 (V+)	1 150 50	+0.8 5.5 2	μs μs V V pA μA
POWER SUPPLY Operating Voltage Range Quiescent Current: OPA334, OPA335 Over Temperature OPA2334, OPA2335 (total—two amplifiers) Over Temperature	I_Q $I_Q = 0$ $I_Q = 0$	2.7	285 570	5.5 350 450 700 900	V μA μA μA μA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance SOT23-5, SOT23-6 Surface-Mount MSOP-8, MSOP-10, SO-8 Surface-Mount	θ_{JA}	-40 -40 -65		+125 +150 +150	$^{\circ}\text{C}$ $^{\circ}\text{C}$ $^{\circ}\text{C}$ $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$

NOTES: (1) 500-hour life test at 150°C demonstrated randomly distributed variation approximately equal to measurement repeatability of $1\mu\text{V}$. (2) Device requires one complete cycle to return to V_{OS} accuracy.

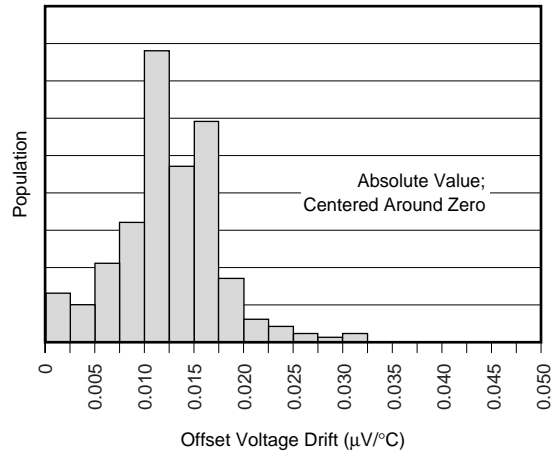
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

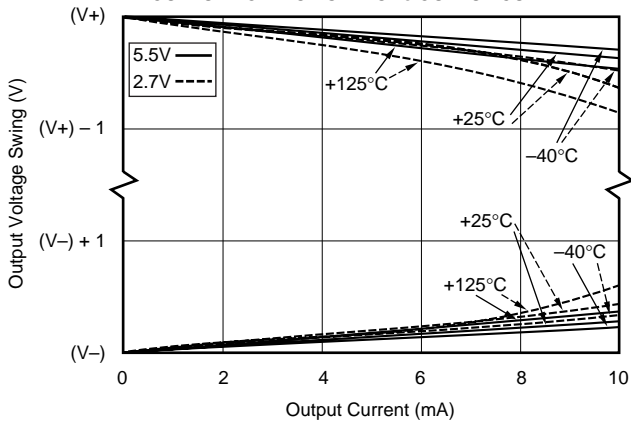
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



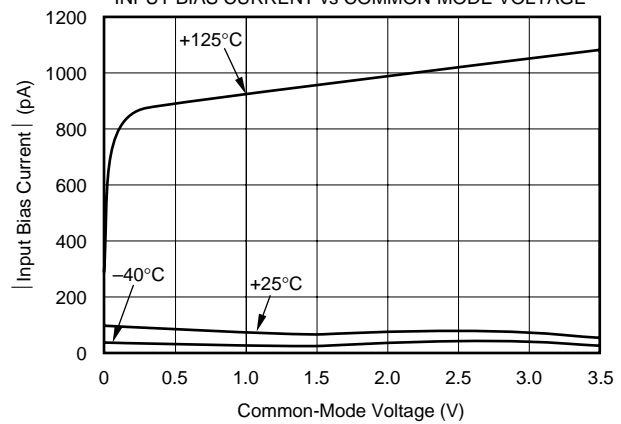
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



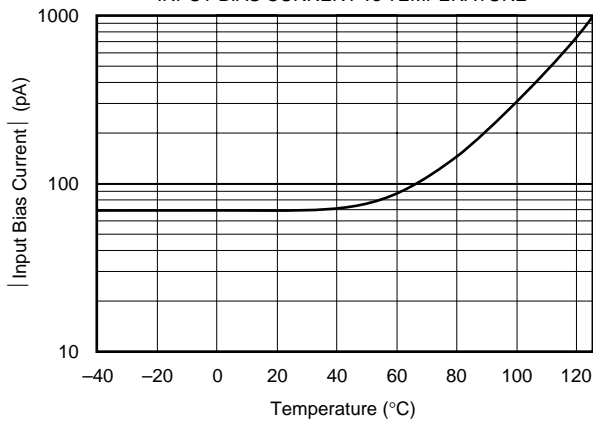
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



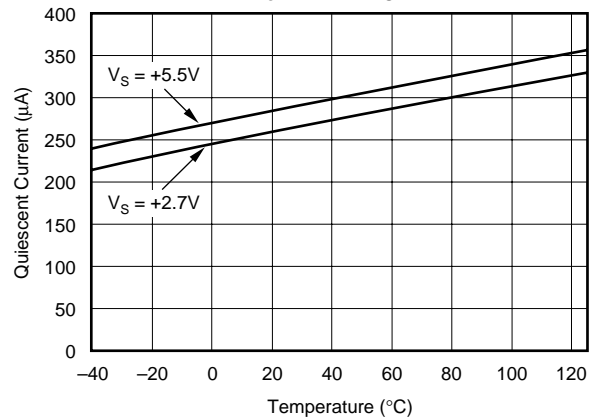
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE

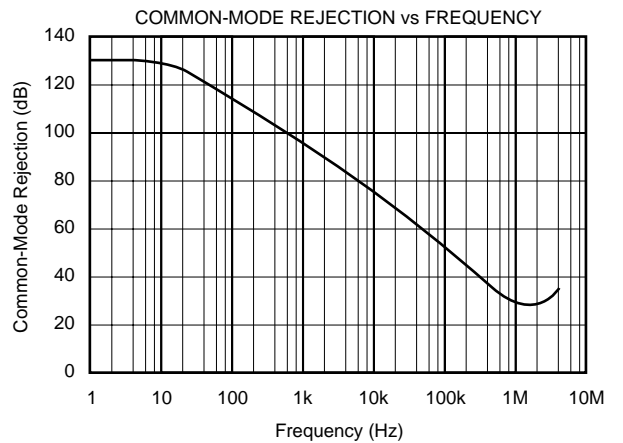
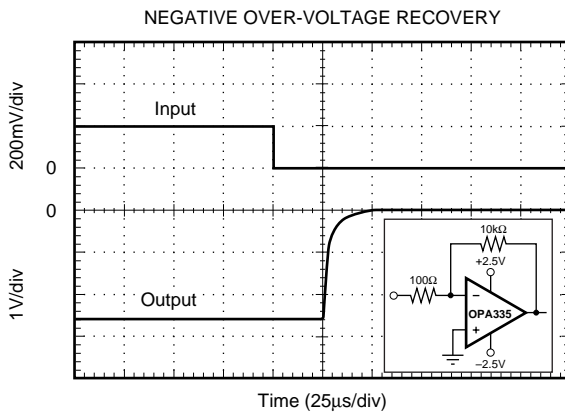
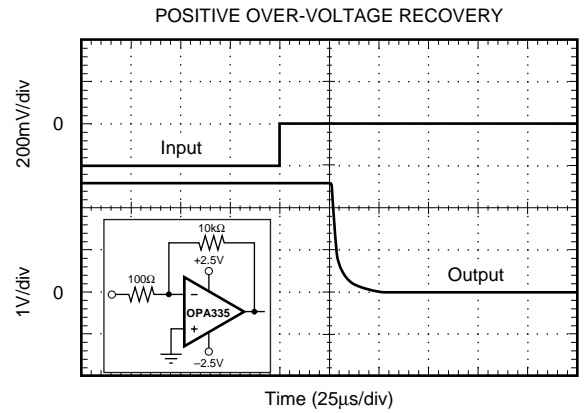
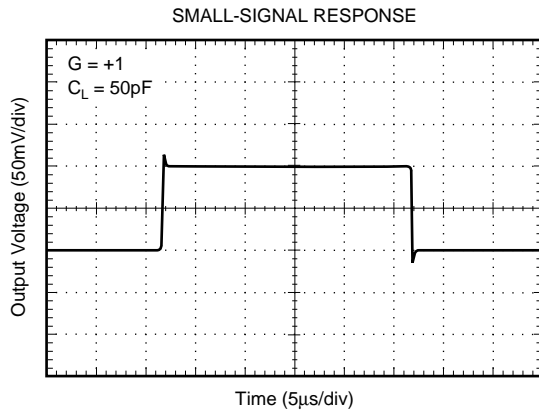
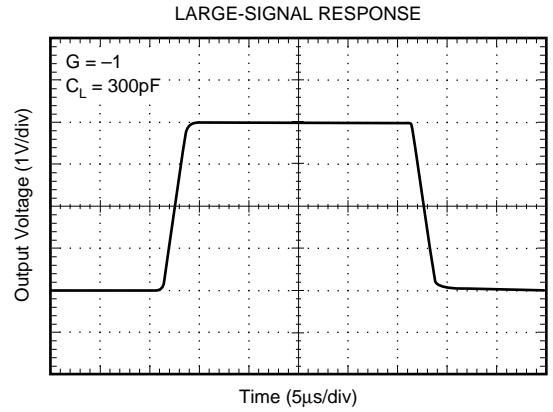
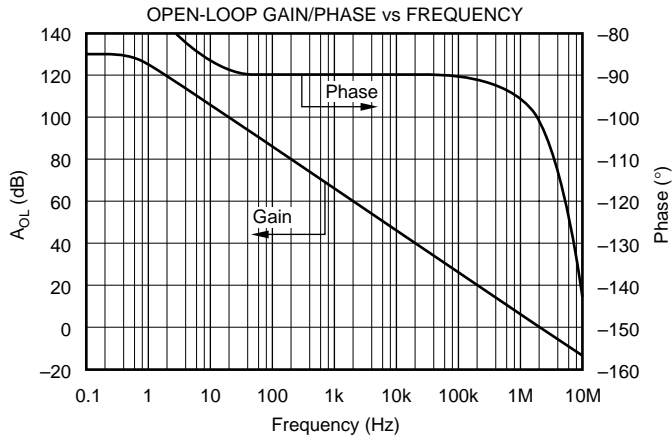


QUIESCENT CURRENT (per channel) vs TEMPERATURE



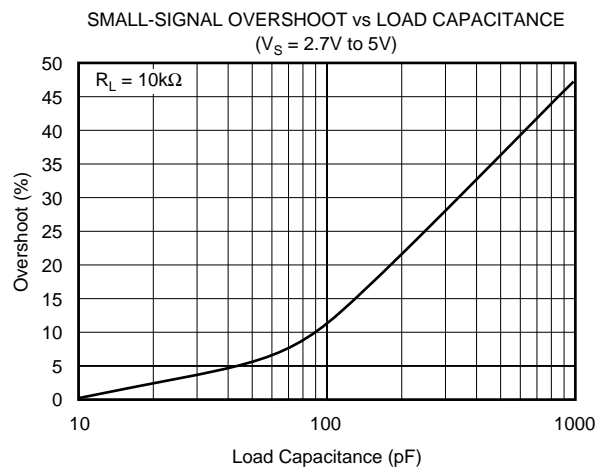
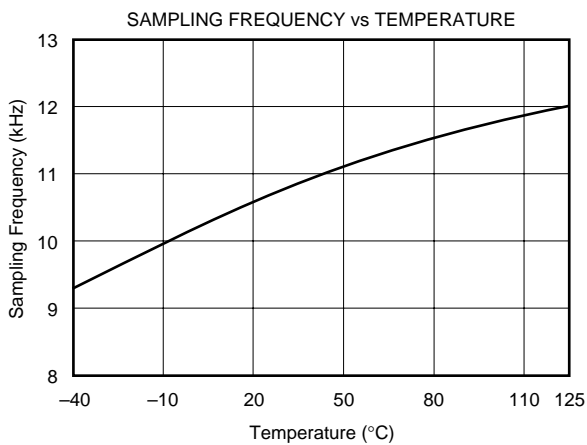
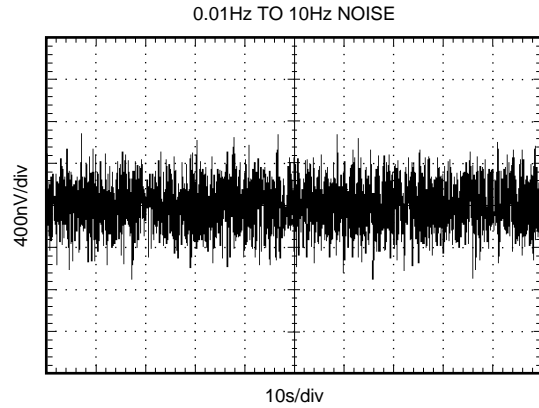
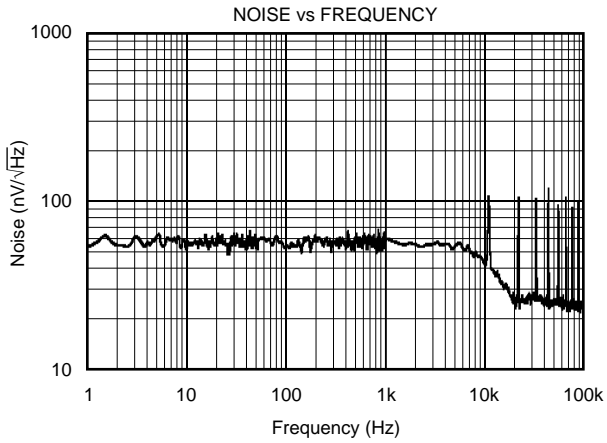
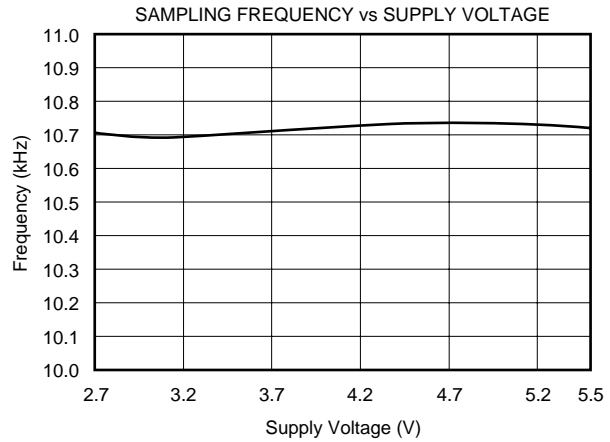
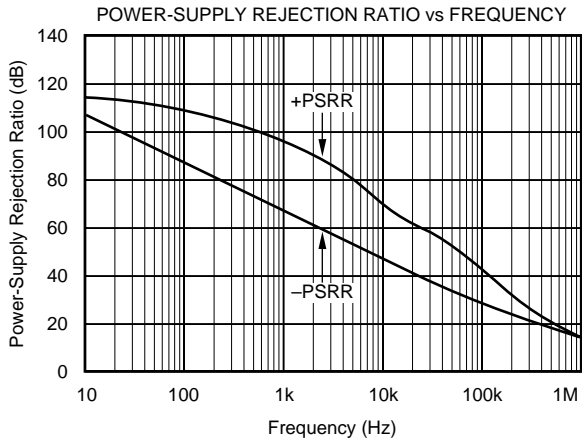
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.



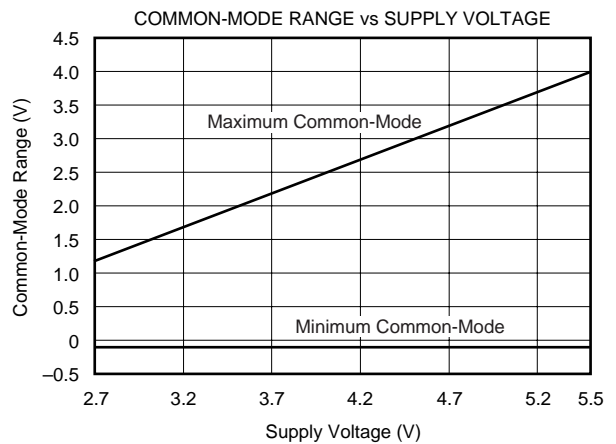
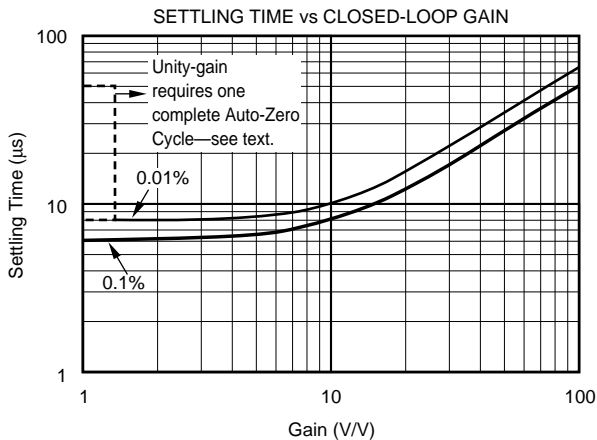
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.



APPLICATIONS INFORMATION

The OPA334 and OPA335 series op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature.

Good layout practice mandates use of a $0.1\mu\text{F}$ capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

- Use low thermoelectric-coefficient connections (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat-sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of $0.1\mu\text{V}/^\circ\text{C}$ or higher, depending on materials used.

OPERATING VOLTAGE

The OPA334 and OPA335 series op amps operate over a power-supply range of $+2.7\text{V}$ to $+5.5\text{V}$ ($\pm 1.35\text{V}$ to $\pm 2.75\text{V}$). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

OPA334 ENABLE FUNCTION

The enable/shutdown digital input is referenced to the $V-$ supply voltage of the amp. A logic high enables the op amp. A valid logic high is defined as $> 75\%$ of the total supply voltage. The valid logic high signal can be up to 5.5V above the negative supply, independent of the positive supply voltage. A valid logic low is defined as $< 0.8\text{V}$ above the $V-$ supply pin. If dual or split power supplies are used, be sure that logic input signals are properly referred to the negative supply voltage. The Enable pin must be connected to a valid high or low voltage, or driven, not left open circuit.

The logic input is a high-impedance CMOS input, with separate logic inputs provided on the dual version. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life.

The enable time is $150\mu\text{s}$, which includes one full auto-zero cycle required by the amplifier to return to V_{OS} accuracy. Prior to this time, the amplifier functions properly, but with unspecified offset voltage.

Disable time is $1\mu\text{s}$. When disabled, the output assumes a high-impedance state. This allows the OPA334 to be operated as a gated amplifier, or to have the output multiplexed onto a common analog output bus.

INPUT VOLTAGE

The input common-mode range extends from $(V-) - 0.1\text{V}$ to $(V+) - 1.5\text{V}$. For normal operation, the inputs must be limited to this range. The common-mode rejection ratio is only valid within the valid input common-mode range. A lower supply voltage results in lower input common-mode range; therefore, attention to these values must be given when selecting the input bias voltage. For example, when operating on a single 3V power supply, common-mode range is from 0.1V below ground to half the power-supply voltage.

Normally, input bias current is approximately 70pA; however, input voltages exceeding the power supplies can cause excessive current to flow in or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 1.

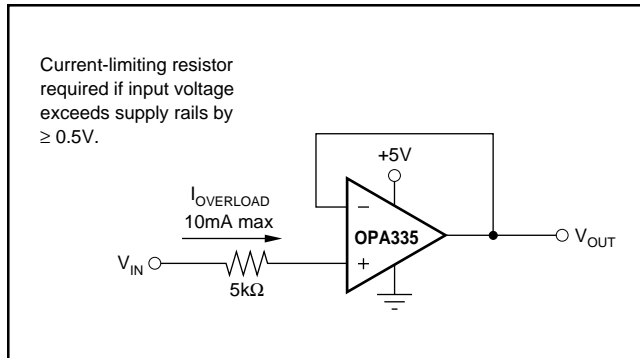


FIGURE 1. Input Current Protection.

INTERNAL OFFSET CORRECTION

The OPA334 and OPA335 series op amps use an auto-zero topology with a time-continuous 2MHz op amp in the signal path. This amplifier is zero-corrected every 100μs using a proprietary technique. Upon power-up, the amplifier requires one full auto-zero cycle of approximately 100μs to achieve specified V_{OS} accuracy. Prior to this time, the amplifier functions properly but with unspecified offset voltage.

This design has remarkably little aliasing and noise. Zero correction occurs at a 10kHz rate, but there is virtually no fundamental noise energy present at that frequency. For all practical purposes, any glitches have energy at 20MHz or higher and are easily filtered, if required. Most applications are not sensitive to such high-frequency noise, and no filtering is required.

Unity-gain operation demands that the auto-zero circuitry correct for common-mode rejection errors of the main amplifier. Because these errors can be larger than 0.01% of a full-scale input step change, one calibration cycle (100μs) can be required to achieve full accuracy. This behavior is shown in the typical characteristic section, see *Settling Time vs Closed-Loop Gain*.

ACHIEVING OUTPUT SWING TO THE OP AMP'S NEGATIVE RAIL

Some applications require output voltage swing from 0V to a positive full-scale voltage (such as +2.5V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0V, near the lower output

swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA334 or OPA335 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires use of another resistor and an additional, more negative, power supply than the op amp's negative supply. A pull-down resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 2.

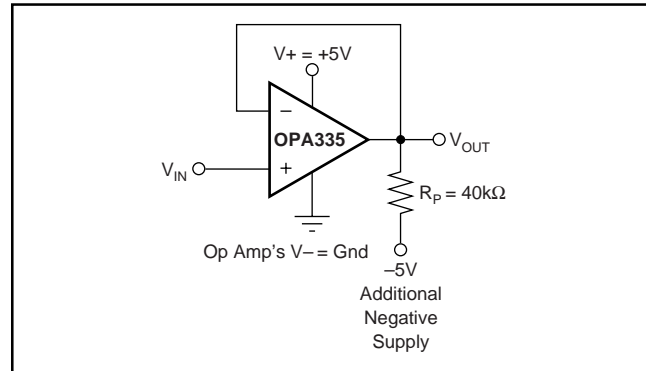


FIGURE 2. Op Amp with Pull-Down Resistor to Achieve $V_{OUT} = \text{Ground}$.

The OPA334 and OPA335 have an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below using the above technique. This technique only works with some types of output stages. The OPA334 and OPA335 have been characterized to perform well with this technique. Accuracy is excellent down to 0V and as low as -2mV. Limiting and non-linearity occurs below -2mV, but excellent accuracy returns as the output is again driven above -2mV. Lowering the resistance of the pull-down resistor will allow the op amp to swing even further below the negative rail. Resistances as low as 10kΩ can be used to achieve excellent accuracy down to -10mV.

LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI (electromagnetic-interference) susceptibility.

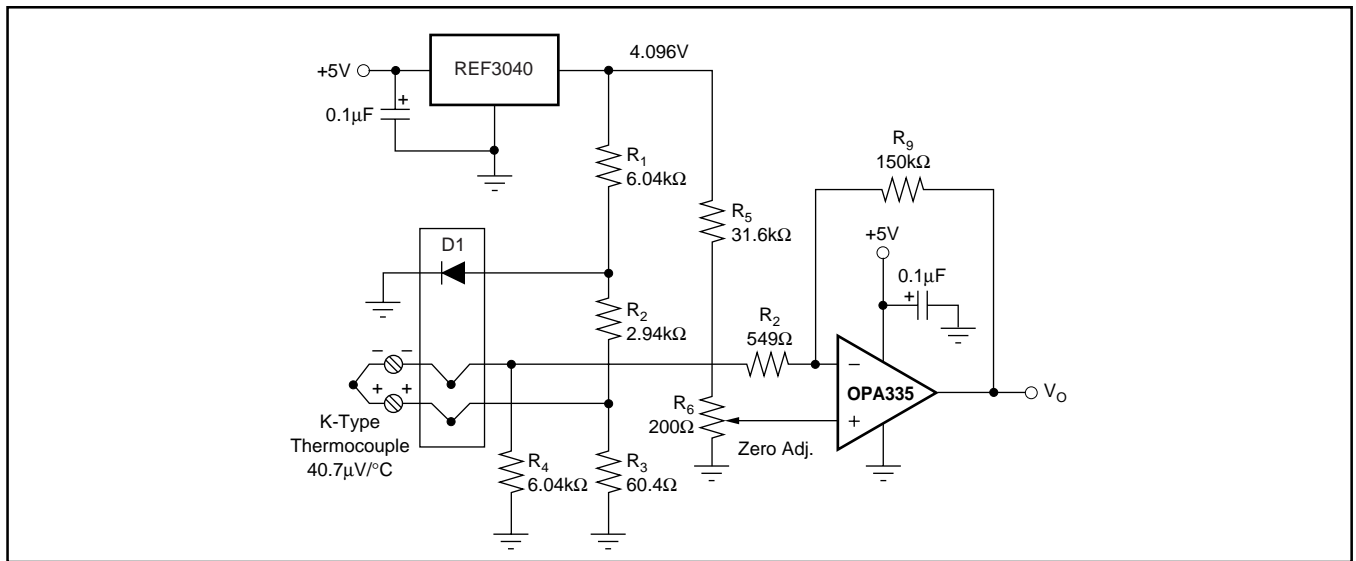


FIGURE 3. Temperature Measurement Circuit.

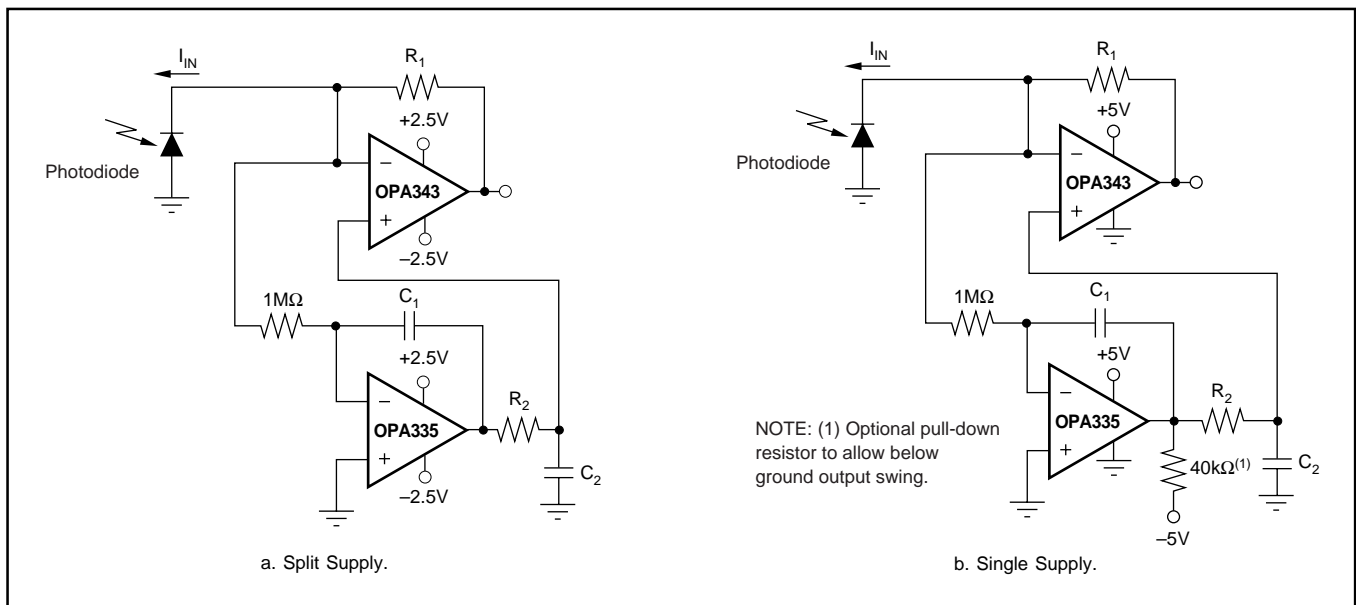


FIGURE 4. Auto-Zeroed Transimpedance Amplifier.

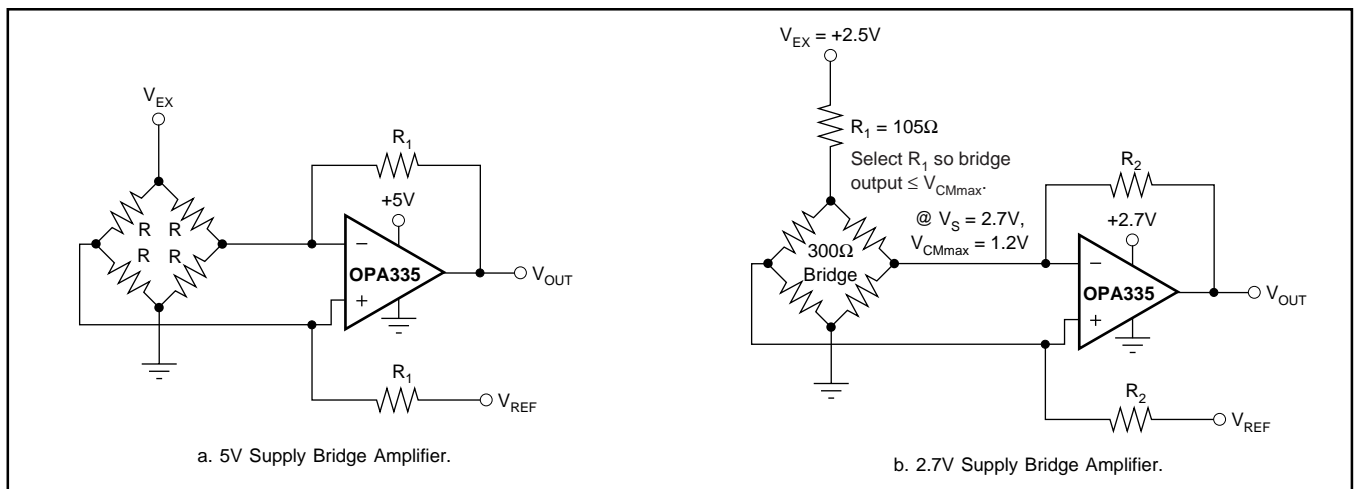


FIGURE 5. Single Op Amp Bridge Amplifier Circuits.

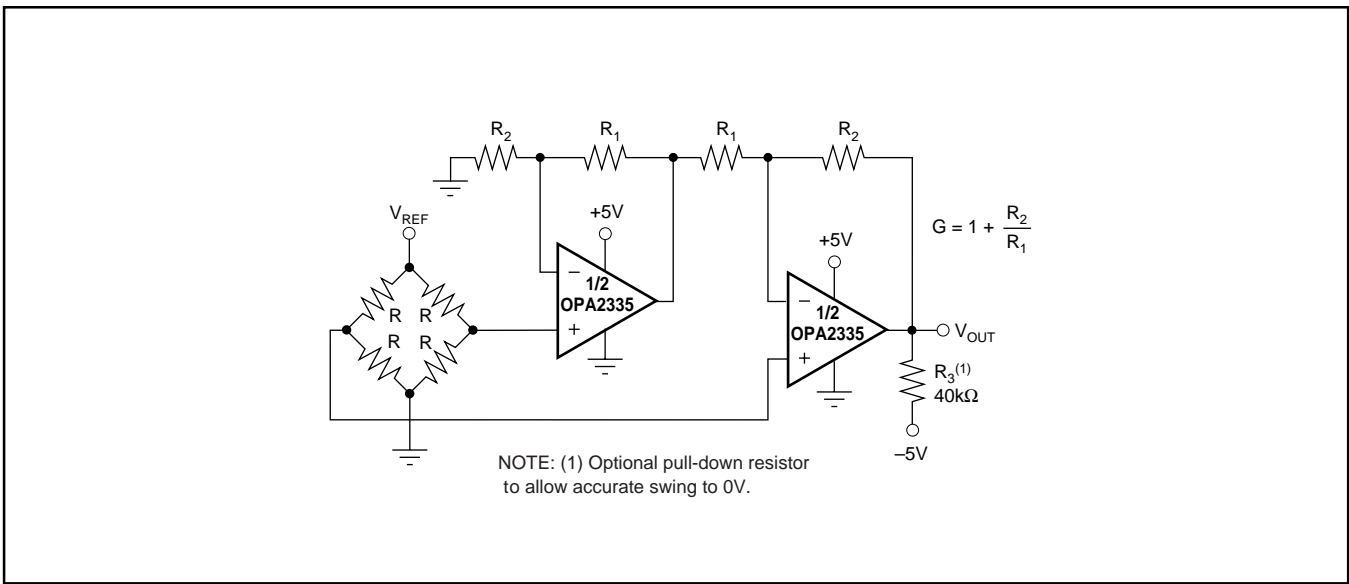


FIGURE 6. Dual Op Amp IA Bridge Amplifier.

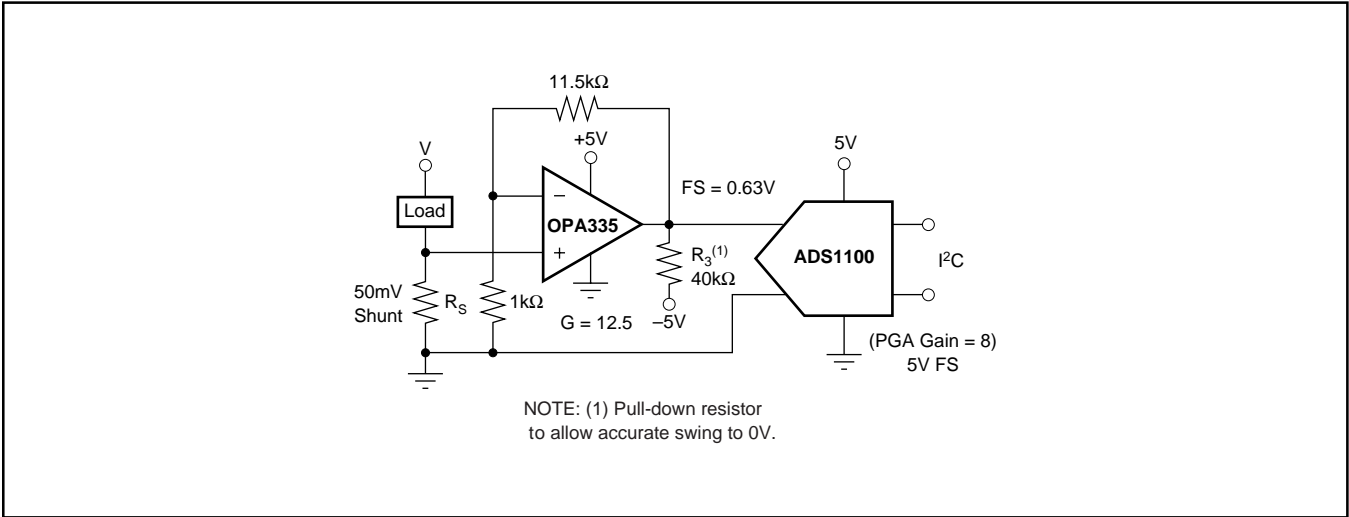


FIGURE 7. Low-Side Current Measurement.

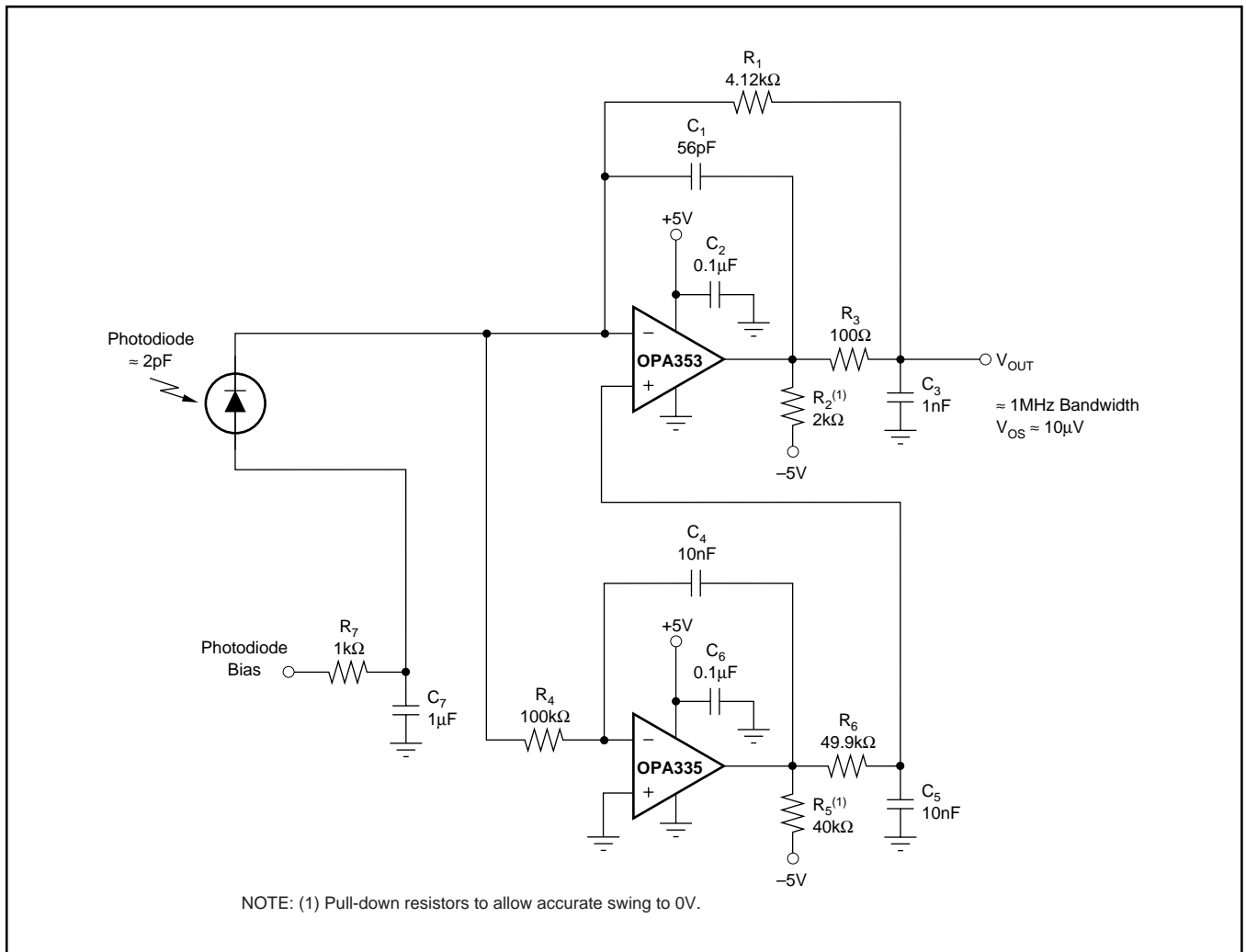
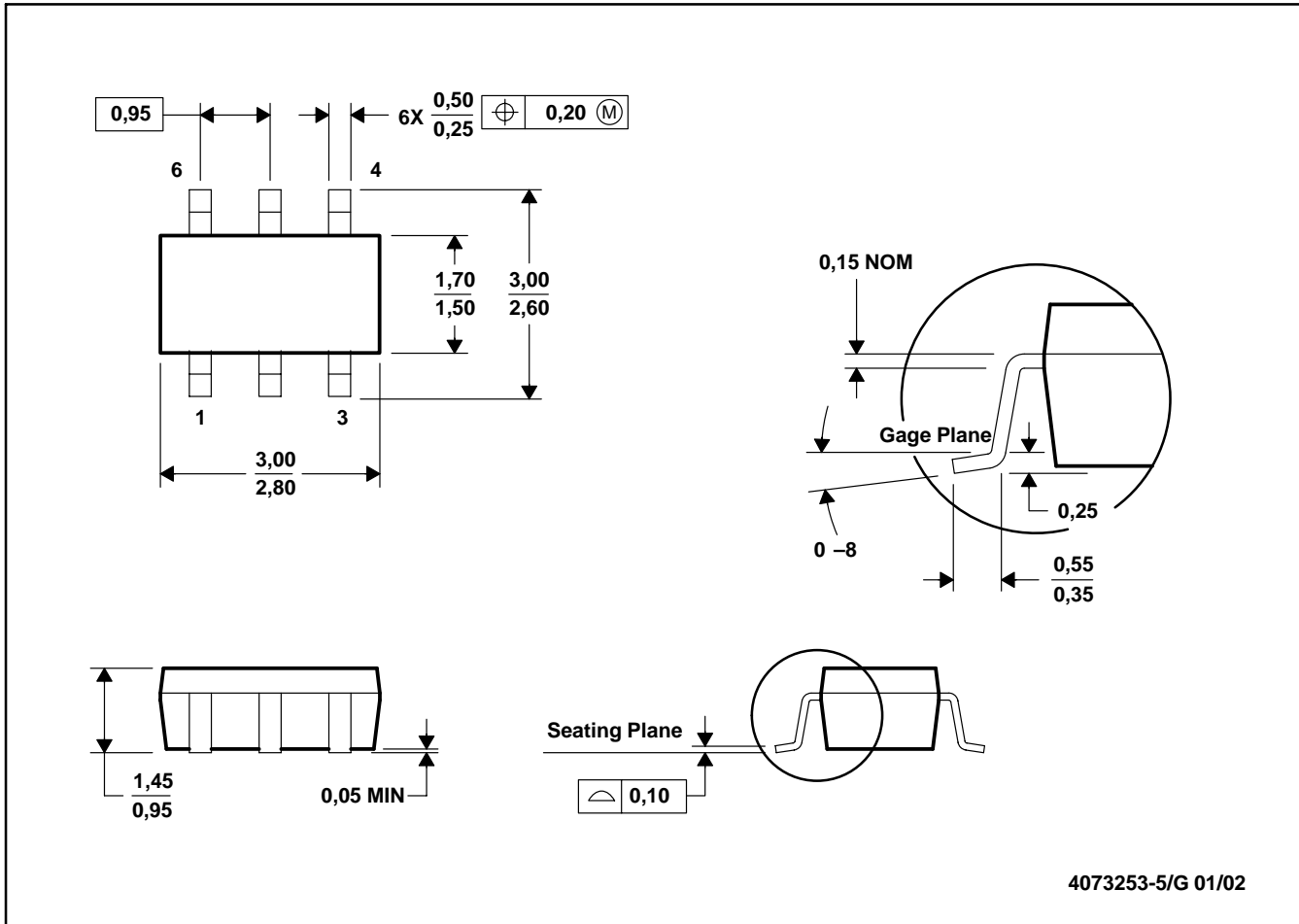
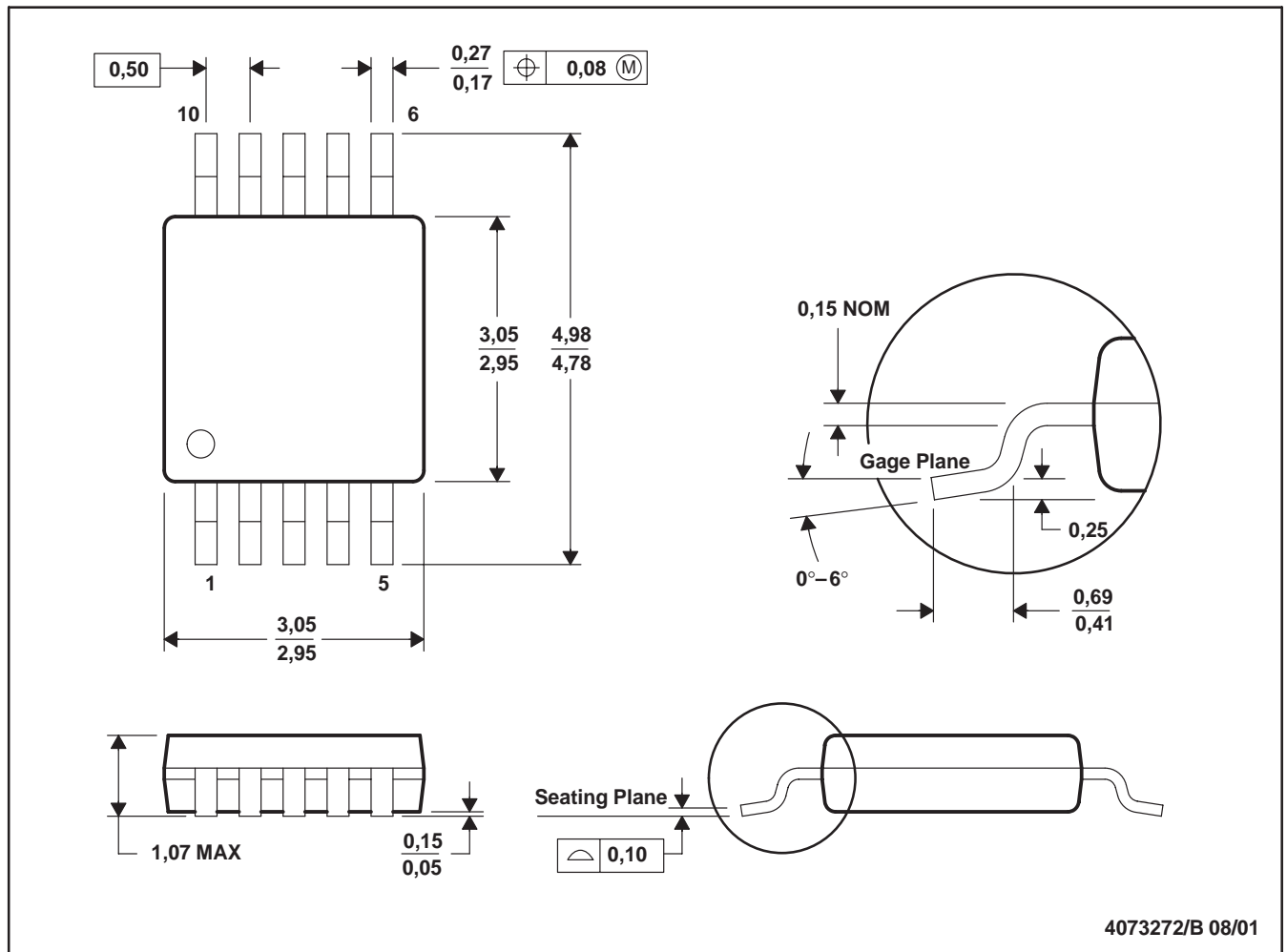


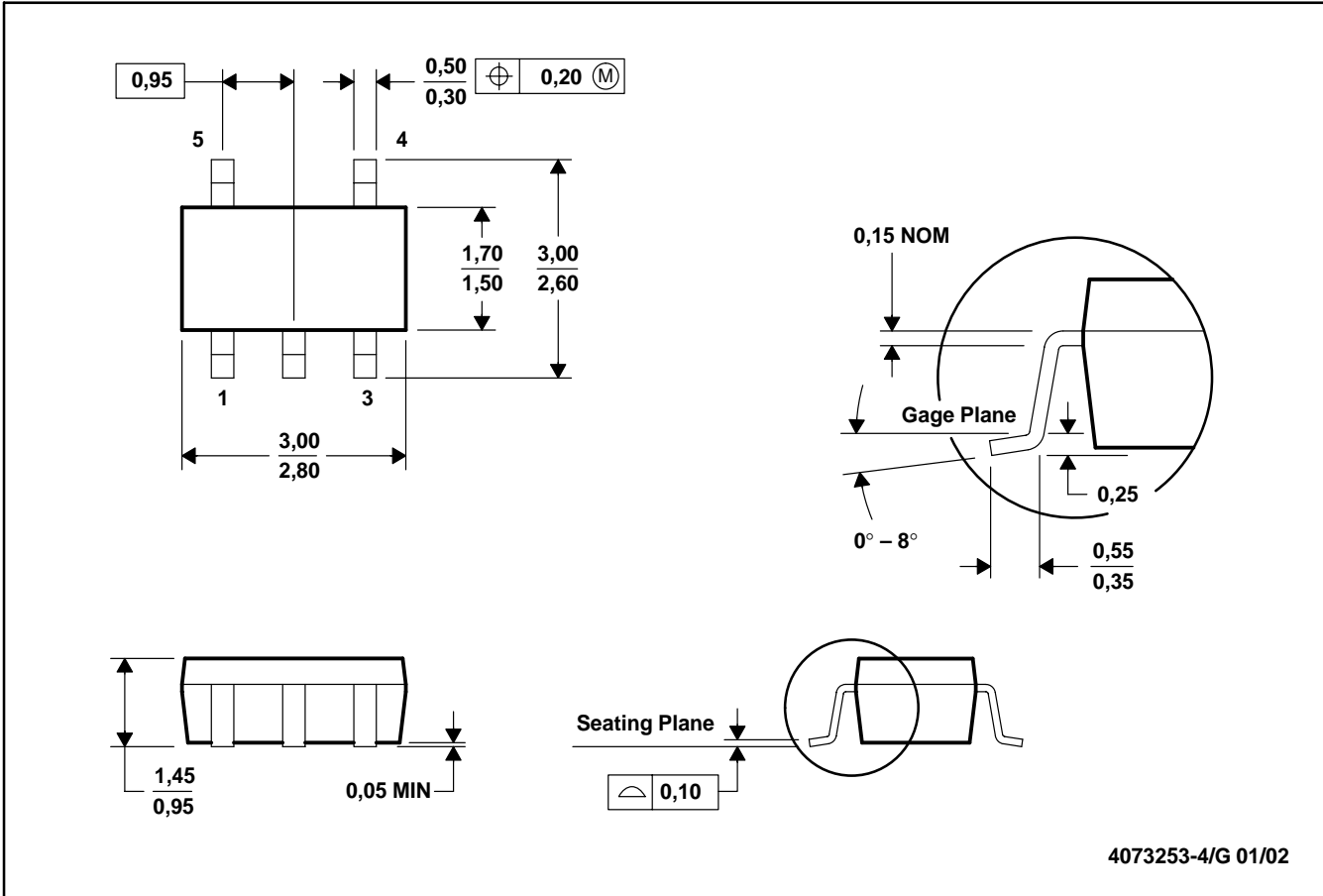
FIGURE 8. High Dynamic Range Transimpedance Amplifier.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 A. Falls within JEDEC MO-187

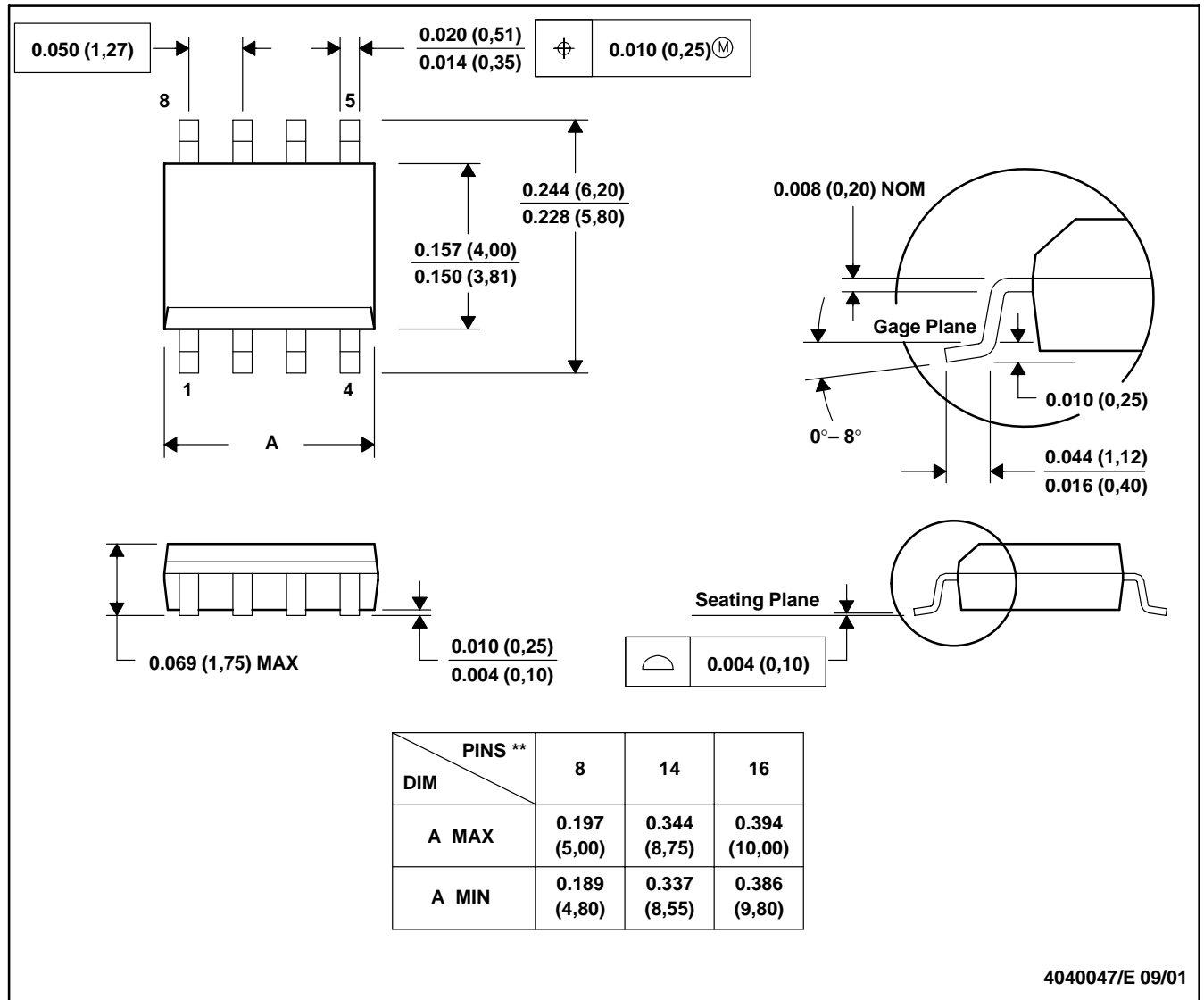


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC MO-178

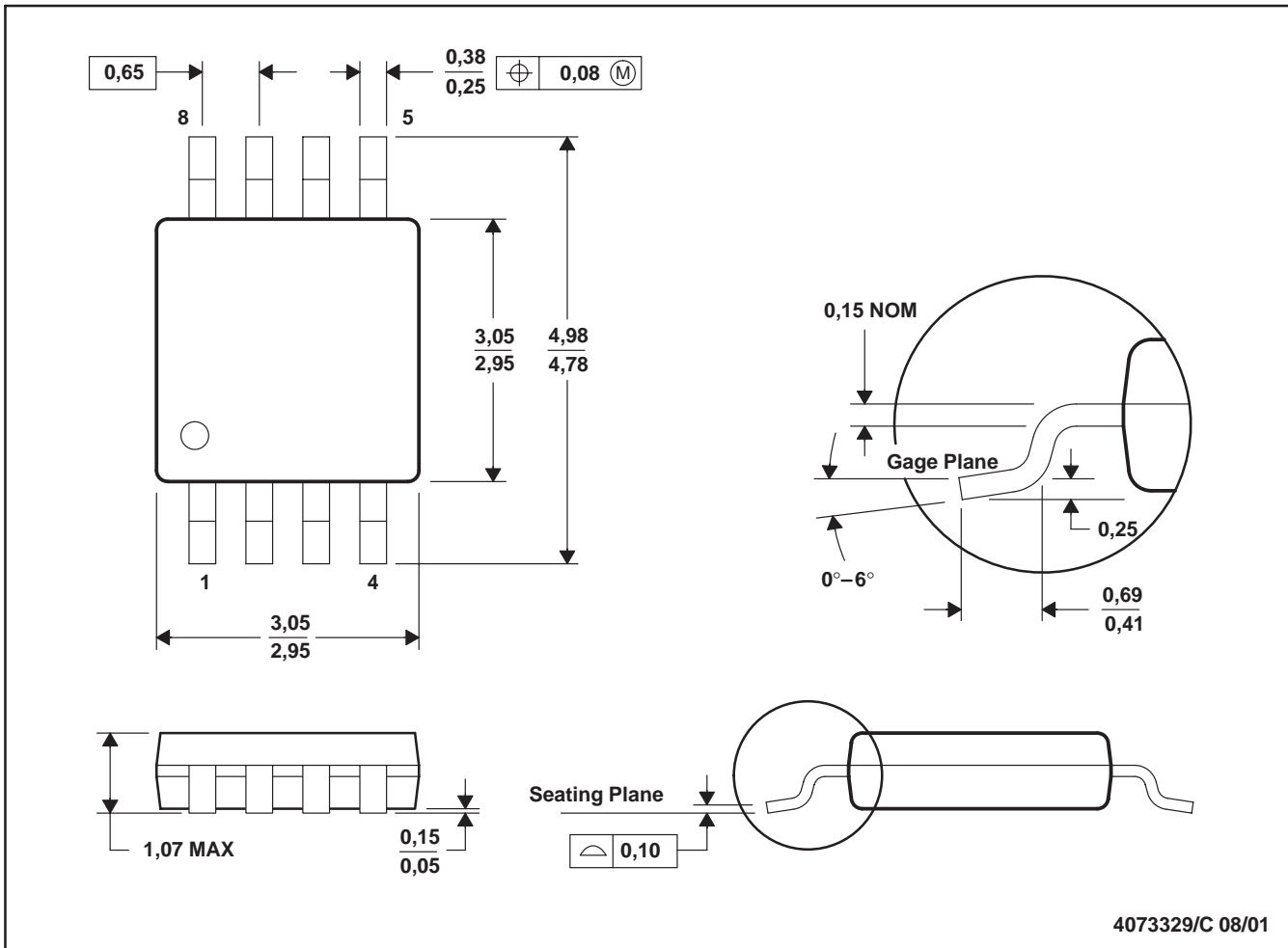
D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2334AIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHE	Samples
OPA2334AIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHE	Samples
OPA2334AIDGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHE	Samples
OPA2335AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 2335	Samples
OPA2335AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 2335	Samples
OPA2335AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		BHF	Samples
OPA2335AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		BHF	Samples
OPA2335AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		BHF	Samples
OPA2335AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		BHF	Samples
OPA2335AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 2335	Samples
OPA2335AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 2335	Samples
OPA334AIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAOI	Samples
OPA334AIDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAOI	Samples
OPA334AIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAOI	Samples
OPA334AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAOI	Samples
OPA335AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 335	Samples
OPA335AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAPI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA335AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAPI	Samples
OPA335AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAPI	Samples
OPA335AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAPI	Samples
OPA335AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 335	Samples
OPA335AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 335	Samples
OPA335AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 335	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2335 :

- Military: [OPA2335M](#)

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2334AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2334AIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2335AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2335AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2335AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA334AIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA334AIDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA335AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA335AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA335AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2334AIDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
OPA2334AIDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
OPA2335AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2335AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2335AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA334AIDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
OPA334AIDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
OPA335AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA335AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA335AIDR	SOIC	D	8	2500	367.0	367.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

MECHANICAL DATA

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

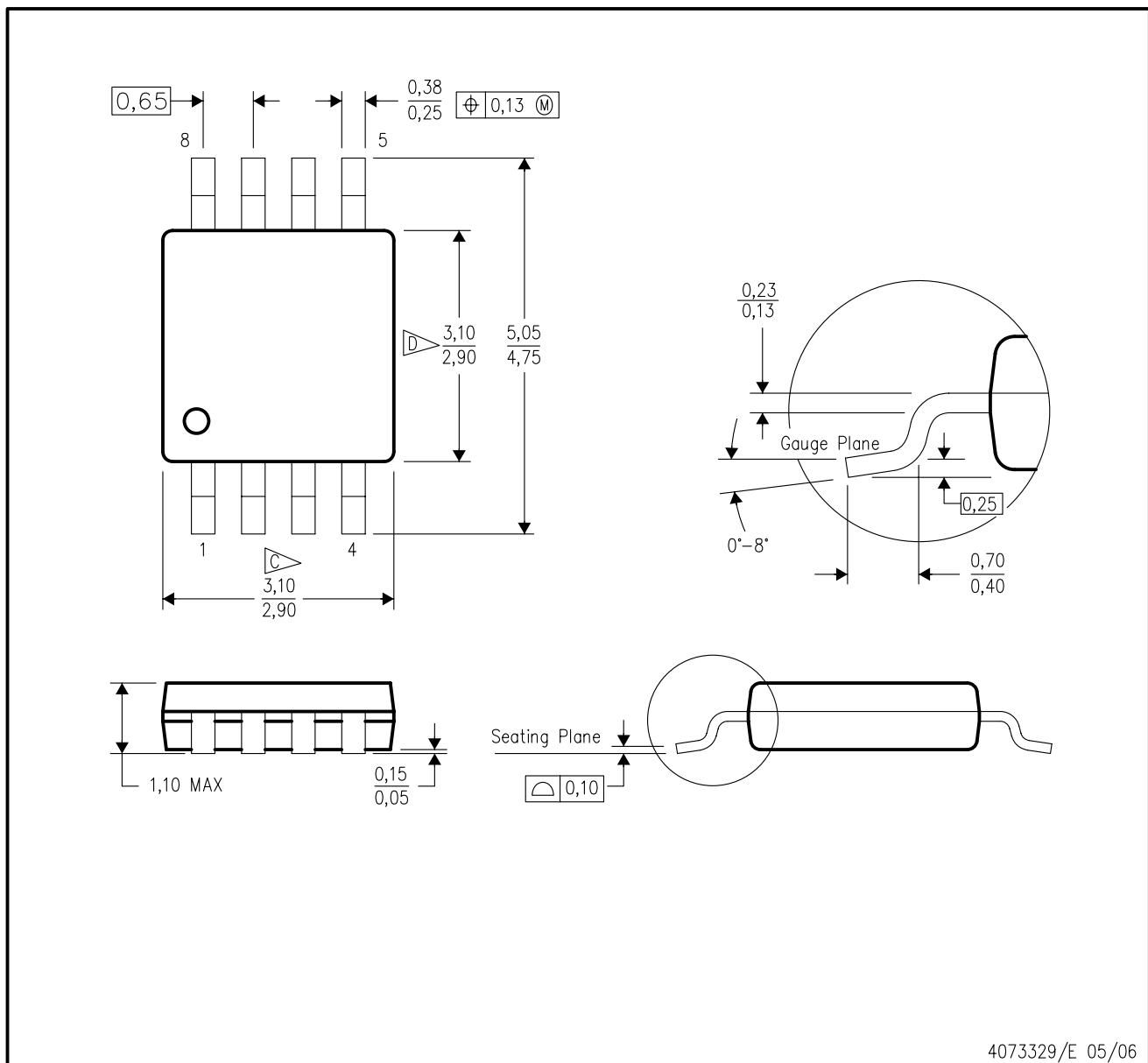
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGS (S-PDSO-G10)

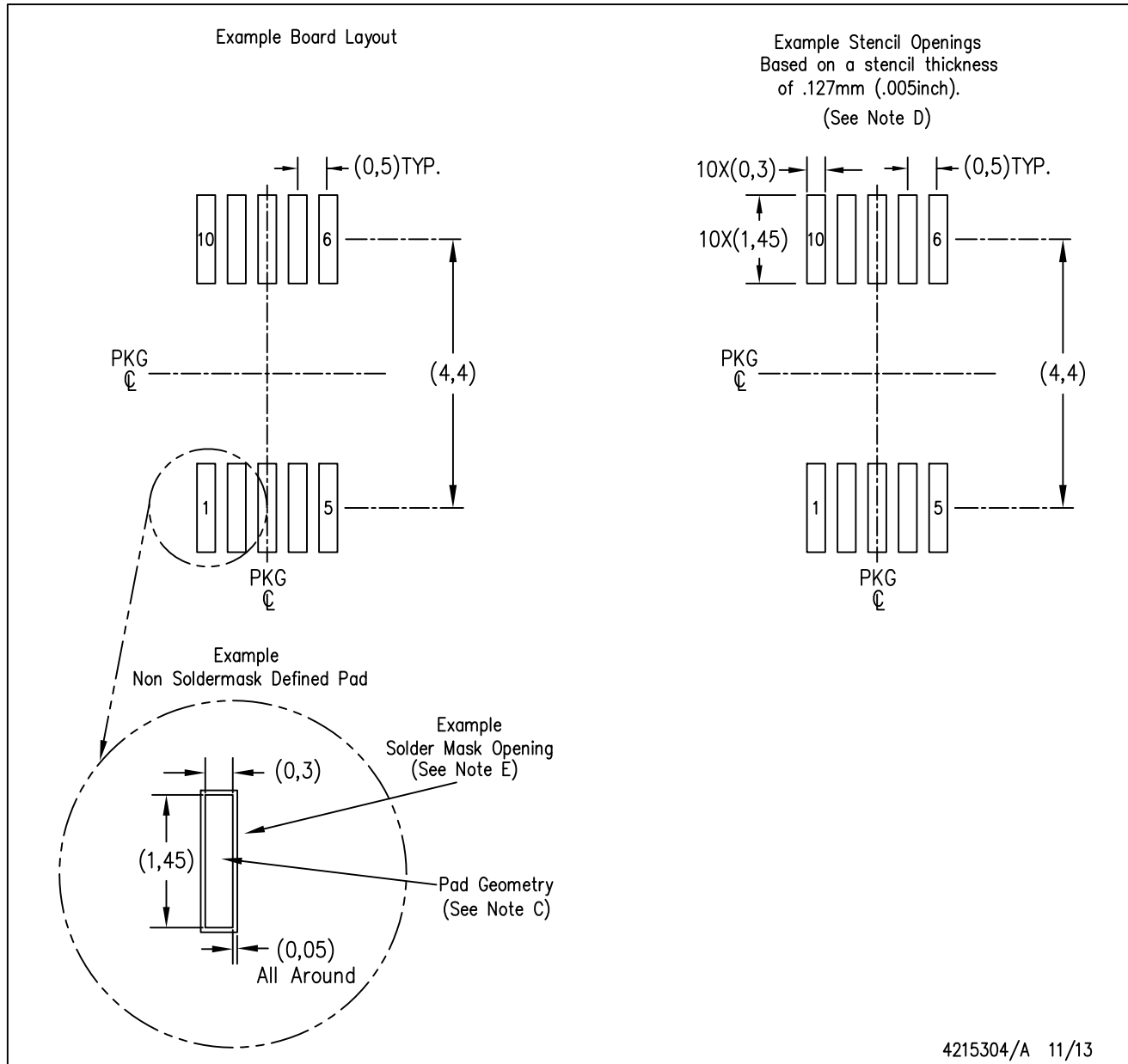
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation BA.

DGS (S-PDSO-G10)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com

AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit www.ameya360.com

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype [ameyasales1](#) [ameyasales2](#)

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com