

### FEATURES

All switches off with power supply off  
 Analog output of on channel clamped within power supplies  
 if an overvoltage occurs  
 Latch-up proof construction  
 Fast switching times  
      $t_{ON}$  250 ns maximum  
      $t_{OFF}$  150 ns maximum  
 Fault and overvoltage protection:  $-40\text{ V}$  to  $+55\text{ V}$   
 Break-before-make construction  
 TTL- and CMOS-compatible inputs

### APPLICATIONS

Data acquisition systems  
 Industrial and process control systems  
 Avionics test equipment  
 Signal routing between systems  
 High reliability control systems

### GENERAL DESCRIPTION

The [ADG438F](#) and [ADG439F](#) are CMOS analog multiplexers, with the [ADG438F](#) comprising eight single channels and the [ADG439F](#) comprising four differential channels. These multiplexers provide fault protection. Using a series n-channel, p-channel, and n-channel MOSFET structure, both device and signal source protection is provided in the event of an overvoltage or power loss. The multiplexer can withstand continuous overvoltage inputs from  $-40\text{ V}$  to  $+55\text{ V}$ . During fault conditions with power supplies off, the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current flows. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources which drive the multiplexer.

The [ADG438F](#) switches one of eight inputs to a common output as determined by the 3-bit binary address lines, A0, A1, and A2. The [ADG439F](#) switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines, A0 and A1. An EN input on each device is used to enable or disable the device. When disabled, all channels are switched off.

### FUNCTIONAL BLOCK DIAGRAM

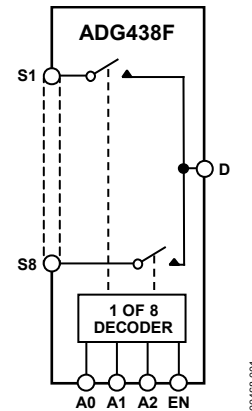


Figure 1.

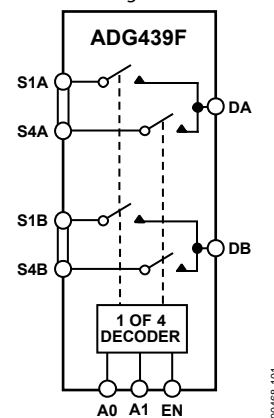


Figure 2.

### PRODUCT HIGHLIGHTS

1. Fault Protection. The [ADG438F](#) and [ADG439F](#) can withstand continuous voltage inputs up to  $-40\text{ V}$  or  $+55\text{ V}$ . When a fault occurs due to the power supplies being turned off, all the channels are turned off and only a leakage current of a few nanoamperes flows.
2. On channel saturates while fault exists.
3. Low  $R_{ON}$ .
4. Fast Switching Times.
5. Break-Before-Make Switching. Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
6. Trench Isolation Eliminates Latch-Up. A dielectric trench separates the p-channel and n-channel MOSFETs thereby preventing latch-up.
7. Improved Off Isolation. Trench isolation enhances the channel-to-channel isolation of the [ADG438F/ADG439F](#).

#### Rev. E

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## REVISION HISTORY

### 7/11—Rev. D to Rev. E

Updated Format.....	Universal
Changes to Product Highlights Section and General Description .....	1
Changes to Specification Section and Table 1 .....	3
Changes to Table 2.....	5
Added Table 3 and Table 4; Renumbered Sequentially .....	6
Changes to Figure 5 to Figure 10.....	7
Changes to Figure 11 to Figure 13.....	8
Added Figure 14 to Figure 16.....	8
Changes to Figure 18 to Figure 20, Figure 23, and Figure 24 .....	9
Changes to Terminology Section.....	12
Changes to Theory of Operation Section, Figure 29, and Figure 30 .....	13
Updated Outline Dimensions .....	14
Changes to Ordering Guide .....	15

### 2/00—Rev. C to Rev. D

# SPECIFICATIONS

## DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ , GND = 0 V, unless otherwise noted.

Table 1.

Parameter	B Version				Unit	Test Conditions/Comments
	+25°C	−40°C to +85°C	−40°C to +105°C	−40°C to +125°C		
ANALOG SWITCH						
Analog Signal Range	$V_{SS} + 1.4$ $V_{DD} - 1.4$ $V_{SS} + 2.2$ $V_{DD} - 2.2$				V typ V typ V typ V typ	Output open circuit  Output loaded, 1 mA
$R_{ON}$	270				$\Omega$ typ	$-10\text{ V} \leq V_S \leq +10\text{ V}$ , $I_S = 1\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	9	390	420	450	$\Omega$ max	See Figure 17
$R_{ON}$ Drift	10	10	10	10	% typ	$-10\text{ V} \leq V_S \leq +10\text{ V}$ , $I_S = 1\text{ mA}$
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.6				% max	$V_S = 0\text{ V}$ , $I_S = 1\text{ mA}$
	3	3	3	3	% max	$V_S = \pm 10\text{ V}$ , $I_S = 1\text{ mA}$
LEAKAGE CURRENTS						
Source Off Leakage, $I_S$ (Off)	$\pm 0.01$				nA typ	$V_D = \pm 10\text{ V}$ , $V_S = \mp 10\text{ V}$
	$\pm 0.5$	$\pm 1.5$	$\pm 1.5$	$\pm 4$	nA max	See Figure 18
Drain Off Leakage, $I_D$ (Off)	$\pm 0.01$				nA typ	$V_D = \pm 10\text{ V}$ , $V_S = \mp 10\text{ V}$
ADG438F ADG439F	$\pm 0.5$	$\pm 5$	$\pm 5$	$\pm 20$	nA max	See Figure 19
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.01$				nA typ	$V_S = V_D = \pm 10\text{ V}$
ADG438F/ADG439F	$\pm 0.5$	$\pm 5$	$\pm 5$	$\pm 20$	nA max	See Figure 20
FAULT						
Source Leakage Current, $I_S$ (Fault)	$\pm 0.02$				nA typ	$V_S = +55\text{ V}$ or $-40\text{ V}$ , $V_D = 0\text{ V}$ ; see Figure 21
(With Overvoltage)	$\pm 0.05$	$\pm 0.1$	$\pm 0.2$	$\pm 0.2$	$\mu\text{A}$ max	
Drain Leakage Current, $I_D$ (Fault)	$\pm 0.05$				nA typ	$V_S = \pm 25\text{ V}$ , $V_D = \mp 10\text{ V}$ ; see Figure 19
(With Overvoltage)	$\pm 0.05$	$\pm 0.1$	$\pm 0.2$	$\pm 0.2$	$\mu\text{A}$ max	
Source Leakage Current, $I_S$ (Fault) (Power Supplies Off)	$\pm 30$				nA typ	$V_S = \pm 25\text{ V}$ , $V_D = V_{EN}$ , A0, A1, A2 = 0 V
	$\pm 0.1$	$\pm 0.2$	$\pm 0.3$	1	$\mu\text{A}$ max	See Figure 22
DIGITAL INPUTS						
Input High Voltage, $V_{INH}$		2.4	2.4	2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	0.8	0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$		$\pm 1$	$\pm 1$	$\pm 1$	$\mu\text{A}$ max	$V_{IN} = 0\text{ V}$ or $V_{DD}$
Digital Input Capacitance, $C_{IN}$	5				pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>						
$t_{TRANSITION}$	175				ns typ	$R_L = 1\text{ M}\Omega$ , $C_L = 35\text{ pF}$
	220	300	300	330	ns max	$V_{S1} = \pm 10\text{ V}$ , $V_{S8} = \mp 10\text{ V}$ ; see Figure 25
$t_{OPEN}$	90					
	60	40	40	40	ns min	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$ , $V_S = 5\text{ V}$ ; see Figure 26
$t_{ON(EN)}$	180				ns typ	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$
	230	300	300	345	ns max	$V_S = 5\text{ V}$ ; see Figure 27
$t_{OFF(EN)}$	100				ns typ	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$
	130	150	150	173	ns max	$V_S = 5\text{ V}$ ; see Figure 27

# ADG438F/ADG439F

Parameter	B Version				Unit	Test Conditions/Comments
	+25°C	–40°C to +85°C	–40°C to +105°C	–40°C to +125°C		
Settling Time, $t_{SETT}$						
0.1%		1	1	1	μs typ	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$
0.01%		2.5	2.5	2.5	μs typ	$V_S = 5\text{ V}$
Charge Injection	15				pC typ	$V_S = 0\text{ V}$ , $R_S = 0\text{ }\Omega$ , $C_L = 1\text{ nF}$ ; see Figure 28
Off Isolation	93				dB typ	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , $f = 100\text{ kHz}$ , $V_S = 7\text{ V rms}$ ; see Figure 23
Channel-to-Channel Crosstalk	93				dB typ	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , $f = 100\text{ kHz}$ , $V_S = 7\text{ rms}$ ; see Figure 24
$C_S$ (Off)	3				pF typ	
$C_D$ (Off)						
ADG438F	22				pF typ	
ADG439F	12				pF typ	
POWER REQUIREMENTS						
$I_{DD}$	0.05				mA typ	$V_{IN} = 0\text{ V or }5\text{ V}$
	0.1	0.2	0.2	0.2	mA max	
$I_{SS}$	0.1				μA typ	
		1	1	1	μA max	

<sup>1</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$  unless otherwise noted.

**Table 2.**

Parameter	Rating
$V_{DD}$ to $V_{SS}$	48 V
$V_{DD}$ to GND	–0.3 V to +48 V
$V_{SS}$ to GND	+0.3 V to –48 V
Digital Input, EN, Ax	–0.3 V to $V_{DD} + 0.3$ V or 20 mA, whichever occurs first
$V_S$ , Analog Input Overvoltage with Power On ( $V_{DD} = +15$ V, $V_{SS} = -15$ V)	$V_{SS} - 25$ V to $V_{DD} + 40$ V
$V_S$ , Analog Input Overvoltage with Power Off ( $V_{DD} = 0$ V, $V_{SS} = 0$ V)	–40 V to +55 V
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	40 mA
Operating Temperature Range Industrial (B Version)	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Plastic DIP Package	
$\theta_{JA}$ , Thermal Impedance	117°C/W
SOIC Package	
$\theta_{JA}$ , Thermal Impedance	
Narrow Body	125°C/W
Wide Body	90°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



#### **ESD (electrostatic discharge) sensitive device.**

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADG438F/ADG439F

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

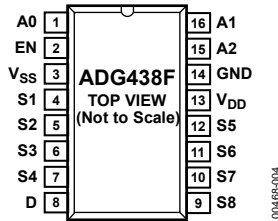


Figure 3. ADG438F Pin Configuration

Table 3. ADG438F Pin Function Description

Pin No.	Mnemonic	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled, and all switches are off. When high, Ax logic inputs determine on switches.
3	V <sub>SS</sub>	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	S1	Source Terminal 1. This pin can be an input or an output.
5	S2	Source Terminal 2. This pin can be an input or an output.
6	S3	Source Terminal 3. This pin can be an input or an output.
7	S4	Source Terminal 4. This pin can be an input or an output.
8	D	Drain Terminal. This pin can be an input or an output.
9	S8	Source Terminal 8. This pin can be an input or an output.
10	S7	Source Terminal 7. This pin can be an input or an output.
11	S6	Source Terminal 6. This pin can be an input or an output.
12	S5	Source Terminal 5. This pin can be an input or an output.
13	V <sub>DD</sub>	Most Positive Power Supply Potential.
14	GND	Ground (0 V) Reference.
15	A2	Logic Control Input.
16	A1	Logic Control Input.

Table 5. ADG438F Truth Table<sup>1</sup>

A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

<sup>1</sup> X = don't care.

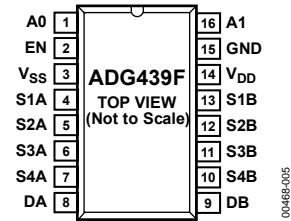


Figure 4. ADG439F Pin Configuration

Table 4. ADG439F Pin Function Description

Pin No.	Mnemonic	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled, and all switches are off. When high, Ax logic inputs determine on switches.
3	V <sub>SS</sub>	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	S1A	Source Terminal 1A. This pin can be an input or an output.
5	S2A	Source Terminal 2A. This pin can be an input or an output.
6	S3A	Source Terminal 3A. This pin can be an input or an output.
7	S4A	Source Terminal 4A. This pin can be an input or an output.
8	DA	Drain Terminal A. This pin can be an input or an output.
9	DB	Drain Terminal B. This pin can be an input or an output.
10	S4B	Source Terminal 4B. This pin can be an input or an output.
11	S3B	Source Terminal 3B. This pin can be an input or an output.
12	S2B	Source Terminal 2B. This pin can be an input or an output.
13	S1B	Source Terminal 1B. This pin can be an input or an output.
14	V <sub>DD</sub>	Most Positive Power Supply Potential.
15	GND	Ground (0 V) Reference.
16	A1	Logic Control Input.

Table 6. ADG439F Truth Table<sup>1</sup>

A1	A0	EN	On Switch Pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

<sup>1</sup> X = don't care.

## TYPICAL PERFORMANCE CHARACTERISTICS

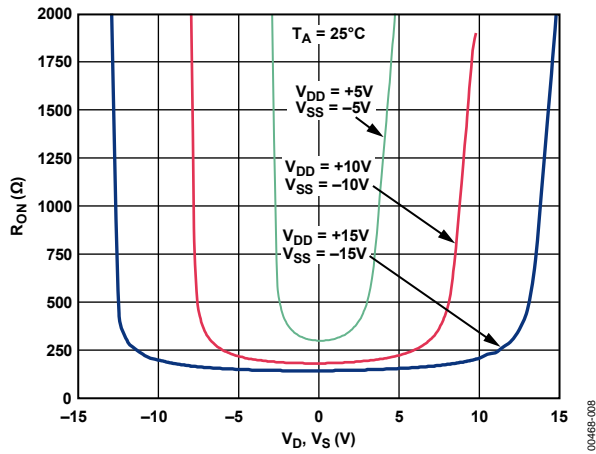


Figure 5. On Resistance as a Function of  $V_D$  ( $V_S$ )

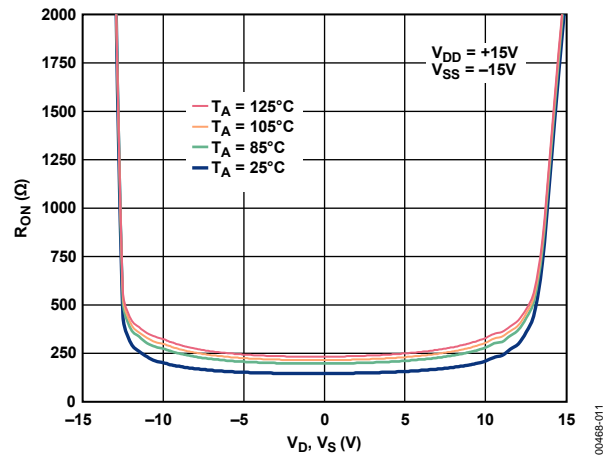


Figure 8. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures

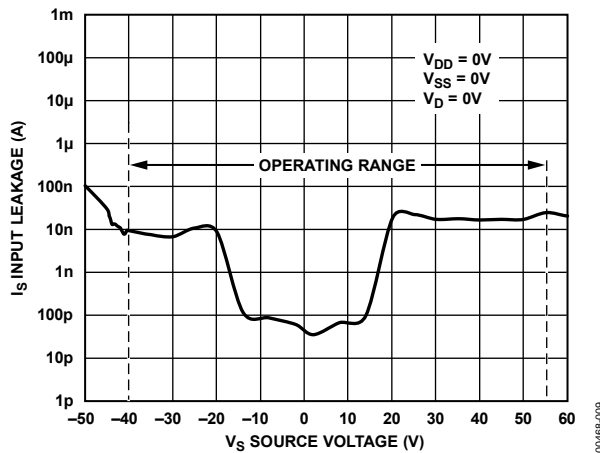


Figure 6. Source Input Leakage Current as a Function of  $V_S$  (Power Supplies Off) During Overvoltage Conditions

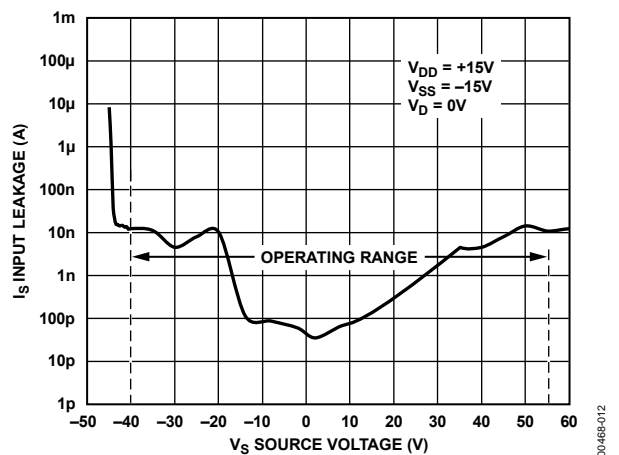


Figure 9. Source Input Leakage Current as a Function of  $V_S$  (Power Supplies On) During Overvoltage Conditions

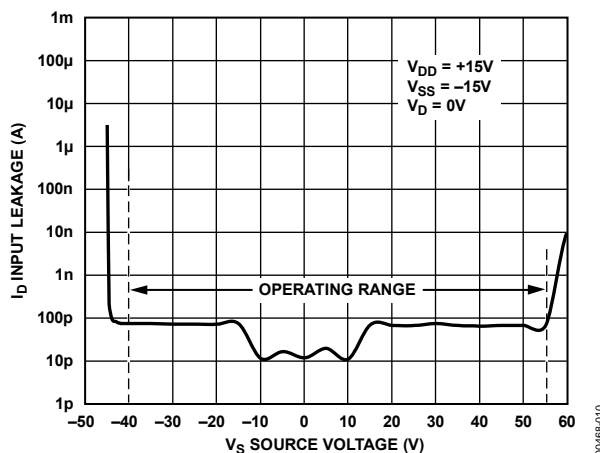


Figure 7. Drain Output Leakage Current as a Function of  $V_S$  (Power Supplies On) During Overvoltage Conditions

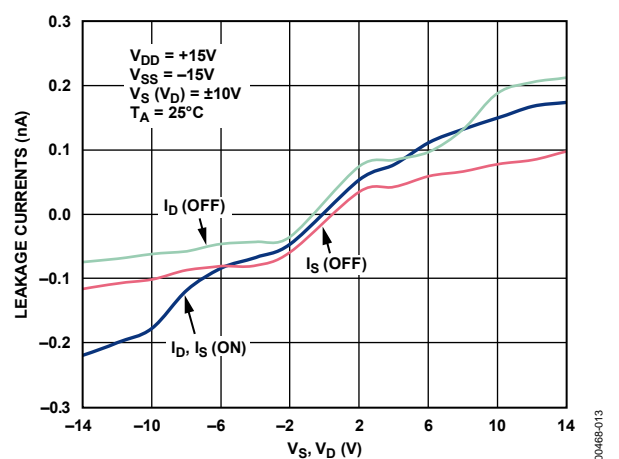


Figure 10. Leakage Currents as a Function of  $V_D$  ( $V_S$ )

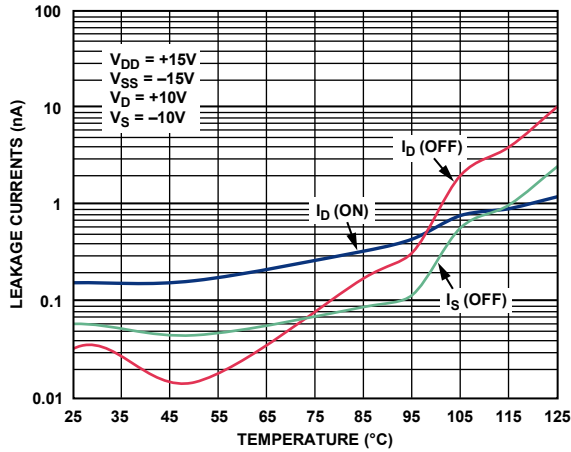


Figure 11. Leakage Currents as a Function of Temperature

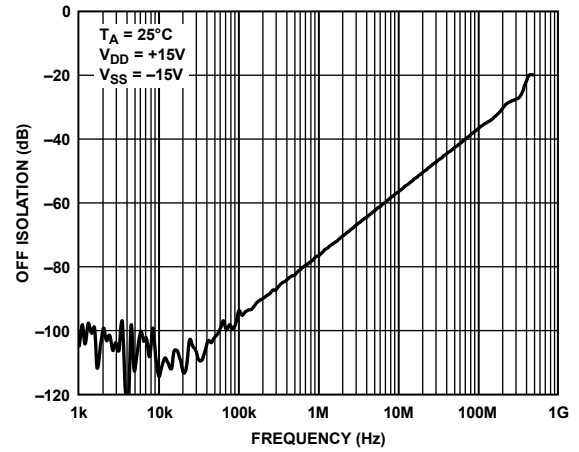


Figure 14. Off Isolation vs. Frequency,  $\pm 15$  V Dual Supply

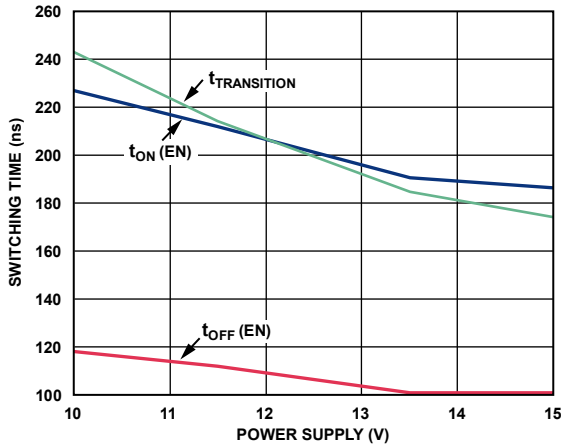


Figure 12. Switching Time vs. Dual Power Supply

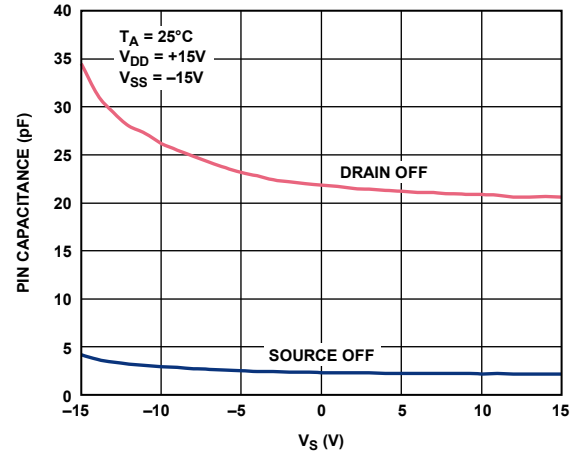


Figure 15. Capacitance vs. Source Voltage

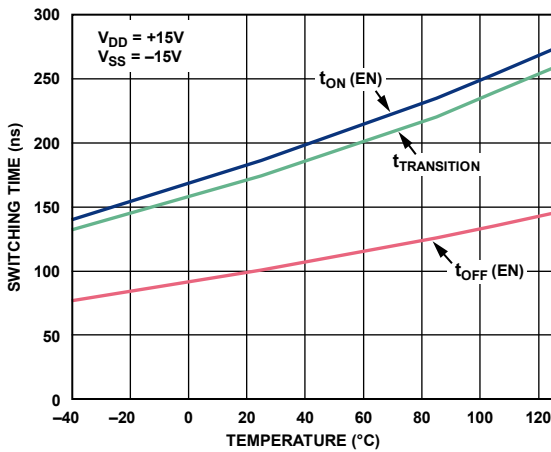


Figure 13. Switching Time vs. Temperature

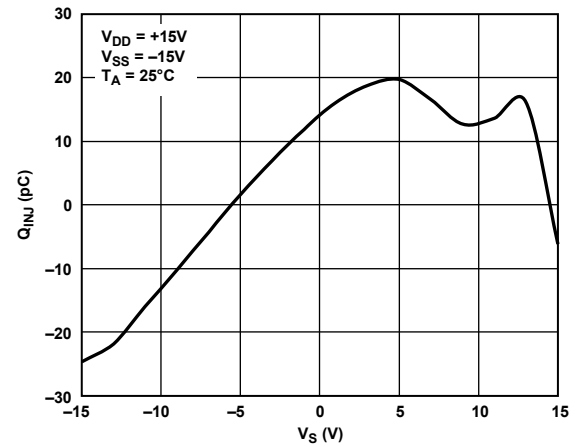


Figure 16. Charge Injection vs. Source Voltage



TEST CIRCUITS

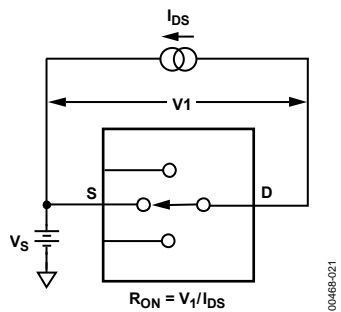


Figure 17. On Resistance

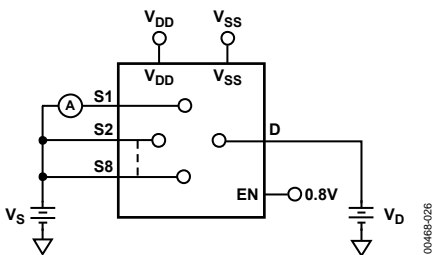


Figure 21. Input Leakage Current (with Overvoltage)

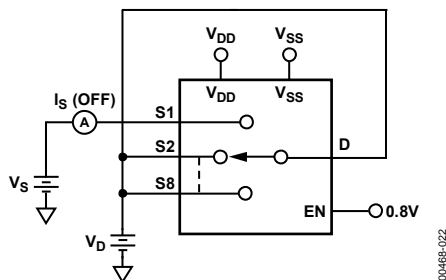
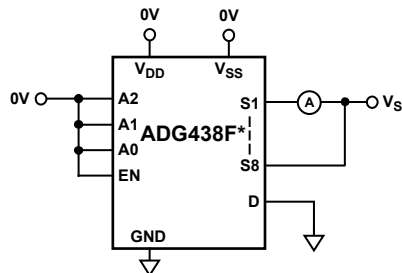


Figure 18.  $I_S$  (Off)



\*SIMILAR CONNECTION FOR ADG439F.  
Figure 22. Input Leakage Current (with Power Supplies Off)

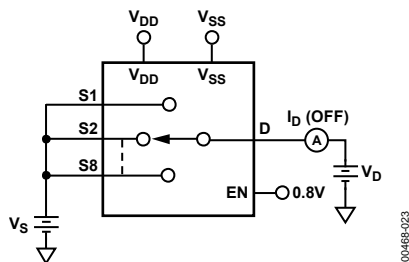
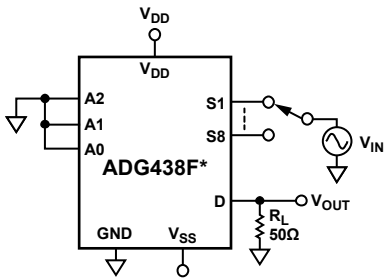


Figure 19.  $I_D$  (Off)



\*SIMILAR CONNECTION FOR ADG439F.  
Figure 23. Off Isolation

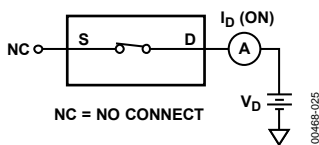
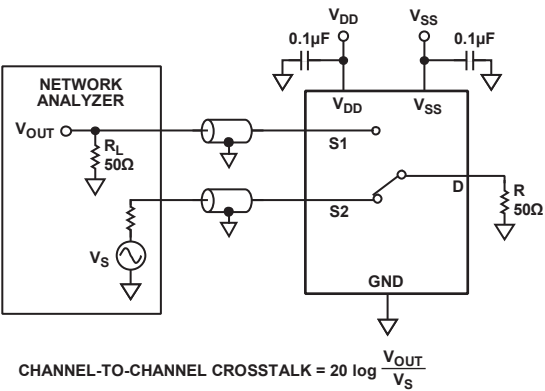
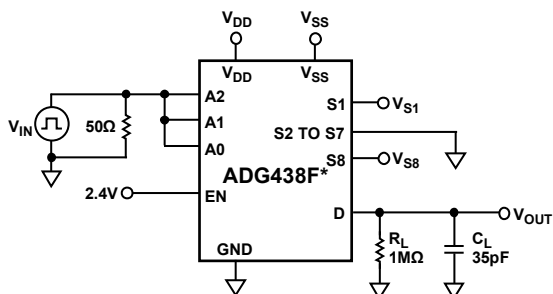


Figure 20.  $I_D$  (On)

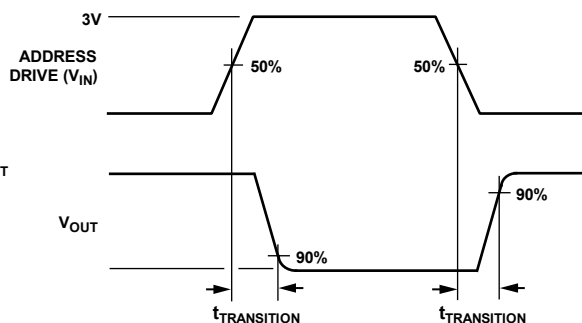


CHANNEL-TO-CHANNEL CROSSTALK =  $20 \log \frac{V_{OUT}}{V_S}$   
Figure 24. Channel-to-Channel Crosstalk

# ADG438F/ADG439F

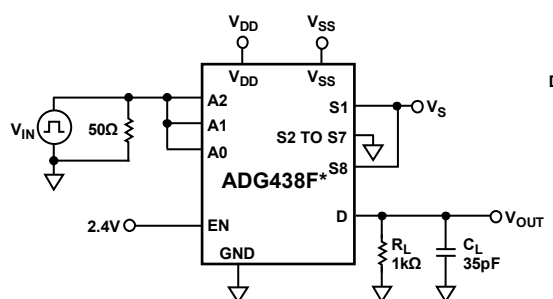


\*SIMILAR CONNECTION FOR ADG439F.

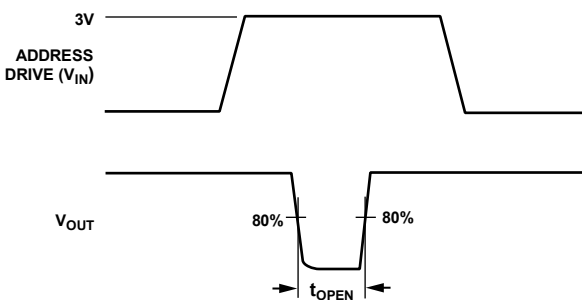


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Figure 25. Switching Time of Multiplexer,  $t_{\text{TRANSITION}}$

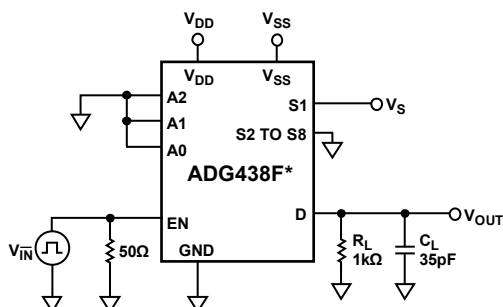


\*SIMILAR CONNECTION FOR ADG439F.

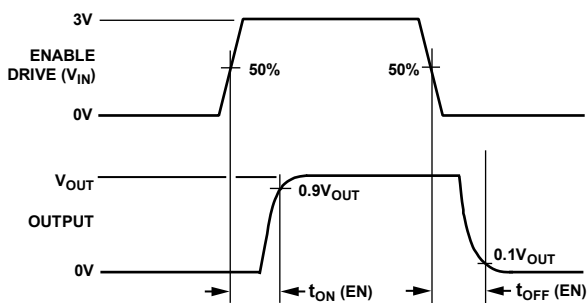


00468-029

Figure 26. Break-Before-Make Delay,  $t_{\text{OPEN}}$

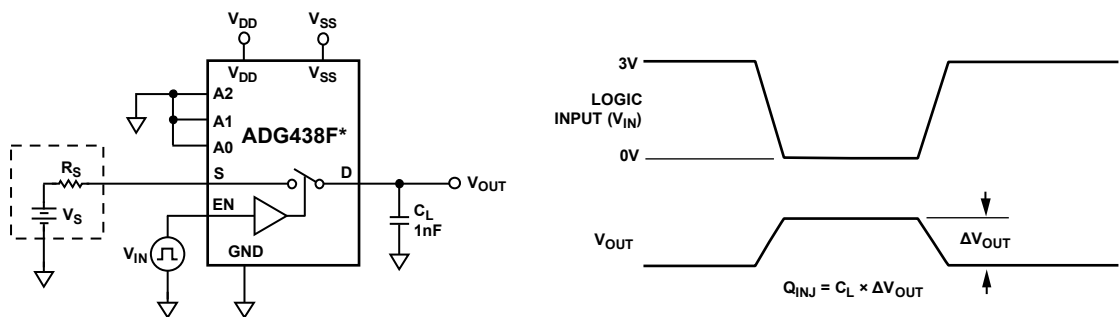


\*SIMILAR CONNECTION FOR ADG439F.



00468-030

Figure 27. Enable Delay,  $t_{\text{ON}}(\text{EN})$ ,  $t_{\text{OFF}}(\text{EN})$



\*SIMILAR CONNECTION FOR ADG439F.

Figure 28. Charge Injection

00468-033

## TERMINOLOGY

**V<sub>DD</sub>**

Most positive power supply potential.

**V<sub>SS</sub>**

Most negative power supply potential.

**GND**

Ground (0 V) reference.

**R<sub>ON</sub>**

Ohmic resistance between D and S.

**ΔR<sub>ON</sub>**

ΔR<sub>ON</sub> represents the difference between the R<sub>ON</sub> of any two channels as a percentage of the maximum R<sub>ON</sub> of those two channels.

**R<sub>FLAT (ON)</sub>**

Flatness is defined as the difference between the maximum and minimum value of the on resistance measured over the specified analog signal range and is represented by R<sub>FLAT (ON)</sub>.

Flatness is calculated by

$$((R_{MAX} - R_{MIN}) / R_{MAX} \times 100)$$

**R<sub>ON</sub> Drift**

Change in R<sub>ON</sub> when temperature changes by one degree Celsius.

**I<sub>S</sub> (Off)**

Source leakage current when the switch is off.

**I<sub>D</sub> (Off)**

Drain leakage current when the switch is off.

**I<sub>D</sub>, I<sub>S</sub> (On)**

Channel leakage current when the switch is on.

**V<sub>D</sub> (V<sub>S</sub>)**

Analog voltage on Terminal D and Terminal S.

**I<sub>S</sub> (Fault—Power Supplies On)**

Source leakage current when exposed to an overvoltage condition.

**I<sub>D</sub> (Fault—Power Supplies On)**

Drain leakage current when exposed to an overvoltage condition.

**I<sub>S</sub> (Fault—Power Supplies Off)**

Source leakage current with power supplies off.

**C<sub>S</sub> (Off)**

Channel input capacitance for off condition.

**C<sub>D</sub> (Off)**

Channel output capacitance for off condition.

**C<sub>D</sub>, C<sub>S</sub> (On)**

On switch capacitance.

**C<sub>IN</sub>**

Digital input capacitance.

**t<sub>ON</sub> (EN)**

Delay time between the 50% and 90% points of the digital input and switch on condition.

**t<sub>OFF</sub> (EN)**

Delay time between the 50% and 90% points of the digital input and switch off condition.

**t<sub>TRANSITION</sub>**

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

**t<sub>OPEN</sub>**

Off time measured between 80% points of both switches when switching from one address state to another.

**V<sub>INL</sub>**

Maximum input voltage for Logic 0.

**V<sub>INH</sub>**

Minimum input voltage for Logic 1.

**I<sub>INL</sub> (I<sub>INH</sub>)**

Input current of the digital input.

**Off Isolation**

A measure of unwanted signal coupling through an off channel.

**Charge Injection**

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

**I<sub>DD</sub>**

Positive supply current.

**I<sub>SS</sub>**

Negative supply current.

## THEORY OF OPERATION

The [ADG438F/ADG439F](#) multiplexers are capable of withstanding overvoltages from  $-40\text{ V}$  to  $+55\text{ V}$ , irrespective of whether the power supplies are present or not. Each channel of the multiplexer consists of an n-channel MOSFET, a p-channel MOSFET, and an n-channel MOSFET, connected in series. When the analog input exceeds the power supplies, one of the MOSFETs saturates, limiting the current. The current during a fault condition is determined by the load on the output. Figure 31 illustrates the channel architecture that enables these multiplexers to withstand continuous overvoltages.

When an analog input of  $V_{SS} + 2.2\text{ V}$  to  $V_{DD} - 2.2\text{ V}$  (output loaded,  $1\text{ mA}$ ) is applied to the [ADG438F/ADG439F](#), the multiplexer behaves as a standard multiplexer, with specifications similar to a standard multiplexer, for example, the on-resistance is  $270\ \Omega$  typically. However, when an overvoltage is applied to the device, one of the three MOSFETs saturates.

Figure 29 to Figure 32 show the conditions of the three MOSFETs for the various overvoltage situations. When the analog input applied to an on channel approaches the positive power supply line, the n-channel MOSFET saturates because the voltage on the analog input exceeds the difference between  $V_{DD}$  and the n-channel threshold voltage ( $V_{TN}$ ). When a voltage more negative than  $V_{SS}$  is applied to the multiplexer, the p-channel MOSFET saturates because the analog input is more negative than the difference between  $V_{SS}$  and the p-channel threshold voltage ( $V_{TP}$ ). Because  $V_{TN}$  is nominally  $1.4\text{ V}$  and  $V_{TP} = -1.4\text{ V}$ , the analog input range to the multiplexer is limited to  $V_{SS} + 1.4\text{ V}$  to  $V_{DD} - 1.4\text{ V}$  (output open circuit) when a  $\pm 15\text{ V}$  power supply is used.

When the power supplies are present but the channel is off, again either the p-channel MOSFET or one of the n-channel MOSFETs remains off when an overvoltage occurs.

Finally, when the power supplies are off, the gate of each MOSFET is at ground. A negative overvoltage switches on the first n-channel MOSFET, but the bias produced by the overvoltage causes the p-channel MOSFET to remain turned off. With a positive overvoltage, the first MOSFET in the series remains off because the gate to source voltage applied to this MOSFET is negative.

During fault conditions (power supplies off), the leakage current into and out of the [ADG438F/ADG439F](#) is limited to a few microamps. This limit protects the multiplexer and succeeding circuitry from over stresses as well as protects the signal sources that drive the multiplexer. Also, the other channels of the multiplexer are undisturbed by the overvoltage and continue to operate normally.

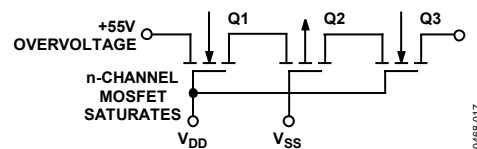


Figure 29. +55 V Overvoltage Input to the On Channel

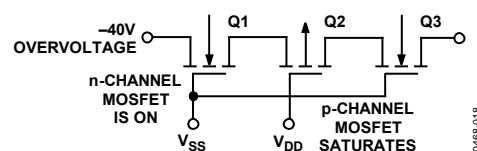


Figure 30. -40 V Overvoltage on an Off Channel with Multiplexer Power On

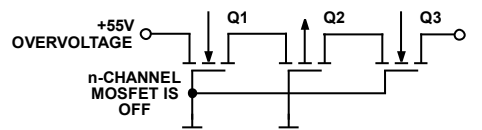


Figure 31. +55 V Overvoltage with Power Off

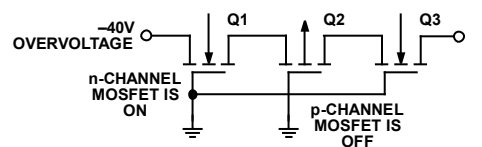
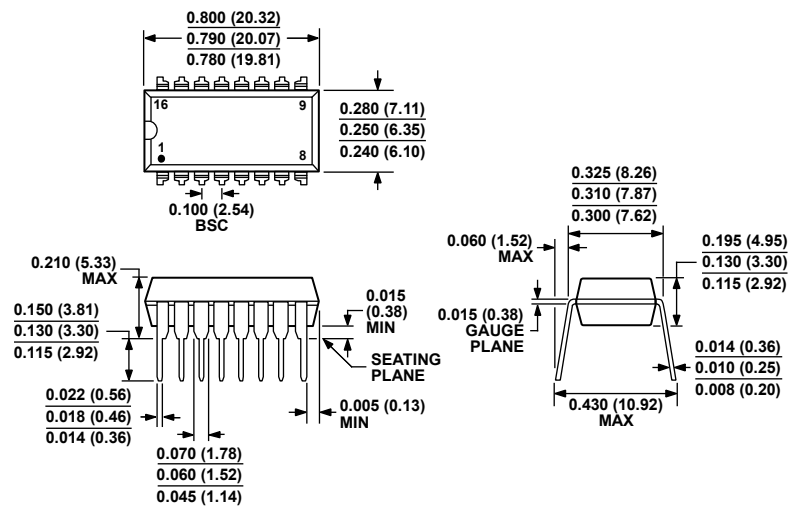


Figure 32. -40 V Overvoltage with Power Off

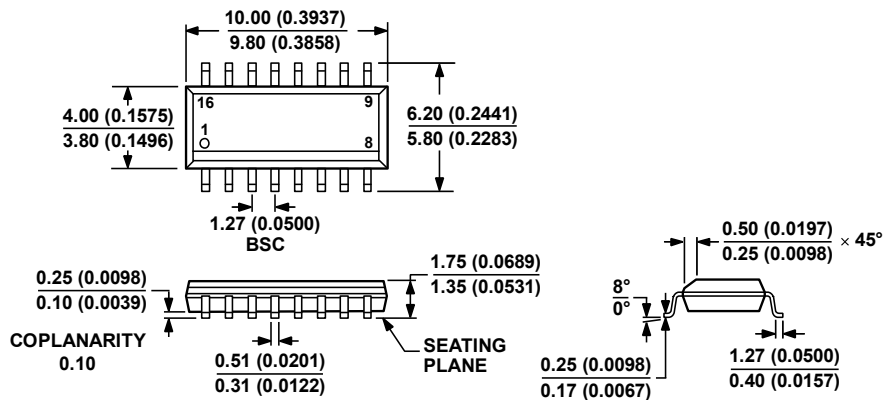
## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-AB  
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 33. 16-Lead Plastic Dual In-Line Package [PDIP]  
Narrow Body  
(N-16)

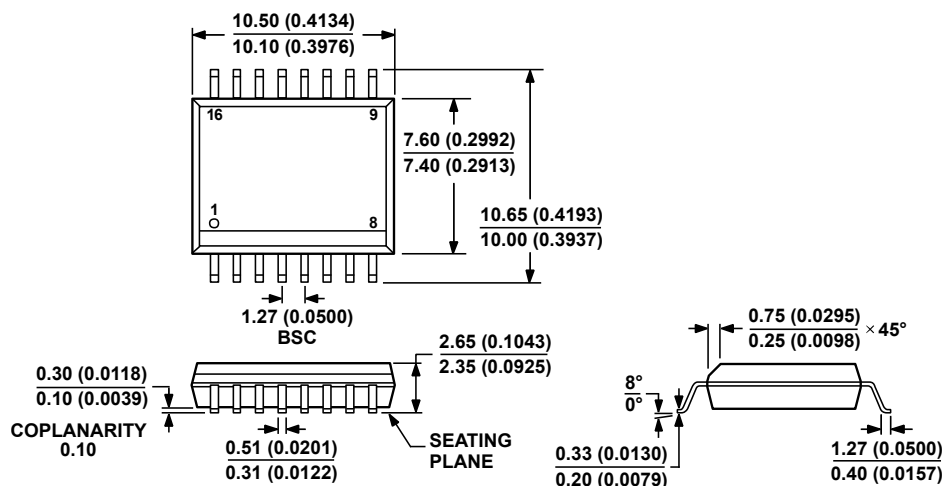
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AC  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 34. 16-Lead Standard Small Outline Package [SOIC\_N]  
Narrow Body  
(R-16)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 35. 16-Lead Standard Small Outline Package [SOIC\_W]

Wide Body  
(RW-16)

Dimensions shown in millimeters and (inches)

03-27-2007-B

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADG438FBN	−40°C to +125°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG438FBNZ	−40°C to +125°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG438FBR	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG438FBR-REEL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG438FBRZ	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG438FBRZ-REEL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG439FBN	−40°C to +125°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG439FBNZ	−40°C to +125°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG439FBR	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG439FBR-REEL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG439FBRW	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADG439FBRWZ	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADG439FBRWZ-REEL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADG439FBRZ	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG439FBRZ-REEL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16

<sup>1</sup> Z = RoHS Compliant Part.

## NOTES



# AMEYA360

Components Supply Platform

Authorized Distribution Brand :



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