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STK581U3C2D-E

Advance Information

Inverter IPM for 3-phase Motor Drive

Overview

This “Inverter IPM” is highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single SIP module (Single-In line Package). Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.

Function

- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control input and status output are at low voltage levels directly compatible with microcontrollers
- Built-in cross conduction prevention
- Externally accessible embedded thermistor for substrate temperature measurement
- The level of the over-current protection current is adjustable with the external resistor, “RSD”

Certification

- UL1557 (File Number : E339285).

Specifications

Absolute Maximum Ratings at $T_c = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}	P to N, surge < 500V *1	450	V
Collector-emitter voltage	V_{CE}	P to U,V,W or U,V,W to N	600	V
Output current	I_o	P, N, U,V,W terminal current	± 30	A
		P, N, U,V,W terminal current at $T_c = 100^\circ\text{C}$	± 15	A
Output peak current	I_{op}	P, N, U,V,W terminal current for a Pulse width of 1ms.	± 45	A
Pre-driver voltage	$VD1,2,3,4$	VB1 to U, VB2 to V, VB3 to W, V_{DD} to V_{SS} *2	20	V
Input signal voltage	V_{IN}	HIN1, 2, 3, LIN1, 2, 3	-0.3 to V_{DD}	V
FAULT terminal voltage	V_{FAULT}	FAULT terminal	-0.3 to V_{DD}	V
Maximum power dissipation	P_d	IGBT per channel	49	W
Junction temperature	T_j	IGBT,FRD	150	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +125	$^\circ\text{C}$
Operating case temperature	T_c	H-IC case temperature	-40 to +100	$^\circ\text{C}$
Tightening torque		Case mounting screws *3	1.17	Nm
Withstand voltage	V_{is}	50Hz sine wave AC 1 minute *4	2000	VRMS

Reference voltage is “ V_{SS} ” terminal voltage unless otherwise specified.

*1 : Surge voltage developed by the switching operation due to the wiring inductance between “P” and “N” terminal.

*2 : Terminal voltage : $VD1=VB1-U$, $VD2=VB2-V$, $VD3=VB3-W$, $VD4=V_{DD}-V_{SS}$

*3 : Flatness of the heat-sink should be 0.15mm and below.

*4 : Test conditions : AC2500V, 1 second.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

Electrical Characteristics at $T_c = 25^\circ\text{C}$, $V_{D1}, V_{D2}, V_{D3}, V_{D4} = 15\text{V}$

Parameter	Symbol	Conditions		Test circuit	min	typ	max	Unit
Power output section								
Collector-emitter cut-off current	I _{CE}	V _{CE} = 600V		Fig.1	-	-	0.1	mA
Bootstrap diode reverse current	I _{R(BD)}	V _{R(BD)}			-	-	0.1	mA
Collector to emitter saturation voltage	V _{CE(SAT)}	I _c = 30A T _j = 25°C	Upper side	Fig.2	-	1.8	2.7	V
			Lower side *1		-	2.1	3.0	
		I _c = 15A T _j = 100°C	Upper side		-	1.5	-	
			Lower side *1		-	1.7	-	
Diode forward voltage	V _F	I _F = 30A T _j = 25°C	Upper side	Fig.3	-	2.0	2.9	V
			Lower side *1		-	2.3	3.2	
		I _F = 15A T _j = 100°C	Upper side		-	1.5	-	
			Lower side *1		-	1.7	-	
Junction to case thermal resistance	θ _{j-c(T)}	IGBT			-	-	2.5	°C/W
	θ _{j-c(D)}	FRD			-	-	3	
Control (Pre-driver) section								
Pre-driver power dissipation	I _D	V _{D1} , 2, 3 = 15V		Fig.4	-	0.08	0.4	mA
		V _{D4} = 15V			-	1.6	4	
High level Input voltage	V _{in H}	H _{IN1} , H _{IN2} , H _{IN3} , L _{IN1} , L _{IN2} , L _{IN3} to V _{SS}			2.5	-	-	V
Low level Input voltage	V _{in L}				-	-	0.8	V
Input threshold voltage hysteresis*1	V _{in th(hys)}				0.5	0.8	-	V
Logic 1 input leakage current	I _{IN+}	V _{IN} = +3.3V			-	100	143	μA
Logic 0 input leakage current	I _{IN-}	V _{IN} = 0V			-	-	2	μA
FAULT terminal input electric current	I _{oSD}	FAULT : ON / V _{FAULT} = 0.1V			-	2	-	mA
FAULT clear time	FLTCLR	Fault output latch time.			18	-	80	ms
V _{CC} and V _S undervoltage positive going threshold.	V _{CCUV+} V _{SUV+}				10.5	11.1	11.7	V
V _{CC} and V _S undervoltage negative going threshold.	V _{CCUV-} V _{SUV-}				10.3	10.9	11.5	V
V _{CC} and V _S undervoltage hysteresis	V _{CCUVH} V _{SUVH-}				0.14	0.2	-	V
Over current protection level	ISD	PW = 100μs, RSD = 0Ω		Fig.5	38.5	-	48.2	A
Output level for current monitor	ISO	I _o = 10A			0.32	0.34	0.36	V

Reference voltage is “ V_{SS} ” terminal voltage unless otherwise specified.

*1 : The lower side's $V_{CE(SAT)}$ and V_F include a loss by the shunt resistance

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Electrical Characteristics at $T_c = 25^\circ\text{C}$, $V_{D1}, V_{D2}, V_{D3}, V_{D4} = 15\text{V}$, $V_{CC}=300\text{V}$, $L=3.5\text{mH}$

Parameter	Symbol	Conditions	Test circuit	min	typ	max	Unit
Switching Character							
Switching time	tON	Io = 30A	Fig.6	0.3	0.6	1.3	μs
	tOFF			-	0.9	1.6	
Turn-on switching loss	Eon	Io = 30A		-	800	-	μJ
Turn-off switching loss	Eoff			-	550	-	μJ
Total switching loss	Etot			-	1350	-	μJ
Turn-on switching loss	Eon	Io = 15A, Tc = 100°C		-	530	-	μJ
Turn-off switching loss	Eoff			-	450	-	μJ
Total switching loss	Etot			-	980	-	μJ
Diode reverse recovery energy	Erec			IF = 15A, P = 400V, Tc = 100°C	-	39	-
Diode reverse recovery time	trr	-			75	-	Ns
Reverse bias safe operating area	RBSOA	Io = 45A, VCE = 450V		Full square			
Short circuit safe operating area	SCSOA	VCE = 400V, Tc = 100°C		4	-	-	μs
Allowable offset voltage slew rate	dv/dt	Between U, V, W to N		-50	-	50	V/ns

Reference voltage is “VSS” terminal voltage unless otherwise specified.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Notes :

- When the internal protection circuit operates, a Fault signal is turned ON (When the Fault terminal is low level, Fault signal is ON state : output form is open DRAIN) but the Fault signal does not latch. After protection operation ends, it returns automatically within about 18ms to 80ms and resumes operation beginning condition. So, after Fault signal detection, set all input signals to OFF (Low) at once. However, the operation of pre-drive power supply low voltage protection (UVLO : with hysteresis about 0.2V) is as follows.

Upper side :

The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn ‘low’.

Lower side :

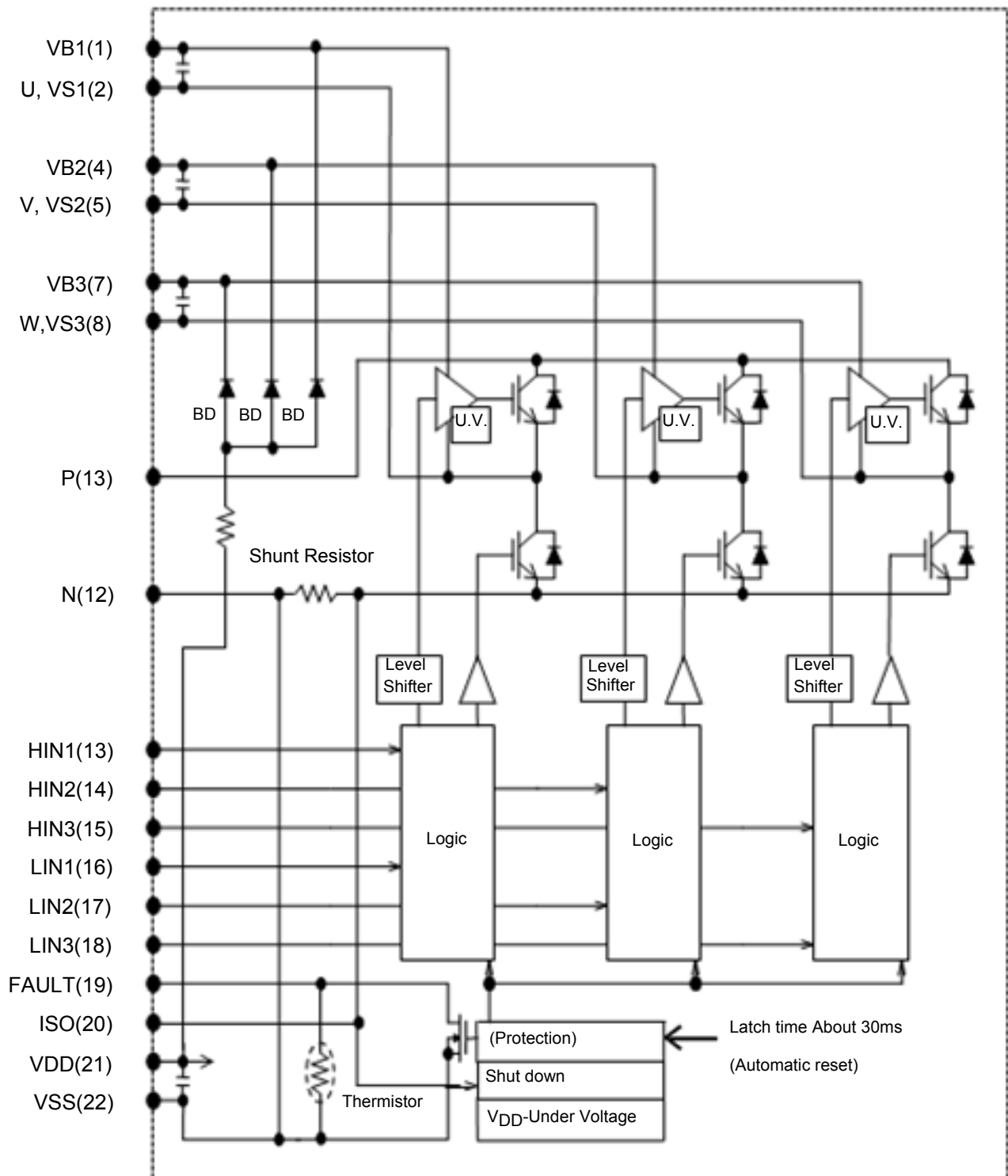
The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.

- When assembling the IPM on the heat sink with M3 type screw, tightening torque range is 0.79 Nm to 1.17 Nm.
- The pre-drive low voltage protection is the feature to protect devices when the pre-driver supply voltage falls due to an operating malfunction.

Module Pin-Out Description

Pin	Name	Description
1	VB1	High Side Floating Supply Voltage 1
2	U, VS1	Output 1 - High Side Floating Supply Offset Voltage
3	–	Without Pin
4	VB2	High Side Floating Supply voltage 2
5	V, VS2	Output 2 - High Side Floating Supply Offset Voltage
6	–	Without Pin
7	VB3	High Side Floating Supply voltage 1
8	W, VS3	Output 1 - High Side Floating Supply Offset Voltage
9	–	Without Pin
10	P	Positive Bus Input Voltage
11	–	Without Pin
12	N	Positive Bus Input Voltage
13	–	Without Pin
14	HIN1	Logic Input High Side Gate Driver - Phase U
15	HIN2	Logic Input High Side Gate Driver - Phase V
16	HIN3	Logic Input High Side Gate Driver - Phase W
17	LIN1	Logic Input Low Side Gate Driver - Phase U
18	LIN2	Logic Input Low Side Gate Driver - Phase V
19	LIN3	Logic Input Low Side Gate Driver - Phase W
20	ISO	Current monitor output
21	VDD	+15V Main Supply
22	VSS	Negative Main Supply

Equivalent Block Diagram



Test Circuit

(The tested phase : U+ shows the upper side of the U phase and U- shows the lower side of the U phase.)

■ ICE / IR(BD)

	U+	V+	W+	U-	V-	W-
M	10	10	10	2	5	8
N	2	5	8	12	12	12

	U(BD)	V(BD)	W(BD)
M	1	4	7
N	22	22	22

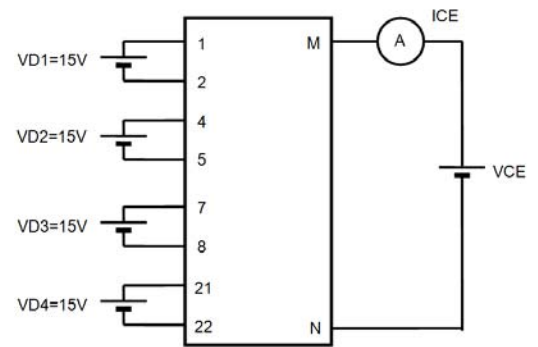


Fig. 1

■ VCE(SAT) (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	10	10	10	2	6	8
N	2	5	8	12	12	12
m	13	14	15	16	17	18

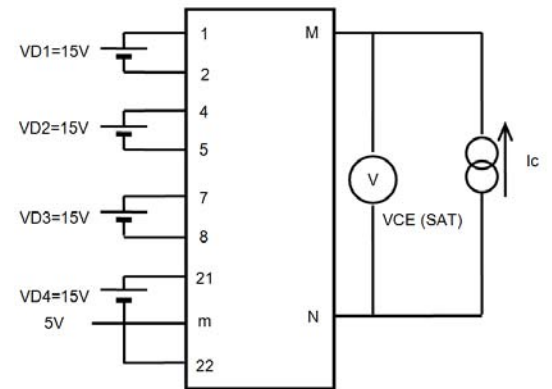


Fig. 2

■ VF (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	10	10	10	2	5	8
N	2	5	8	12	12	12

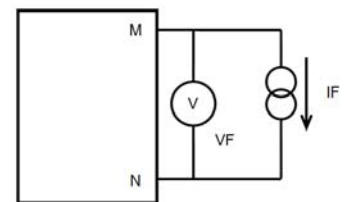


Fig. 3

■ ID

	VD1	VD2	VD3	VD4
M	1	4	7	21
N	2	5	8	22

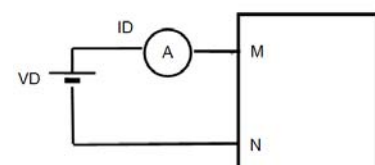


Fig. 4

■ ISD

Input signal

(0 to 5V)

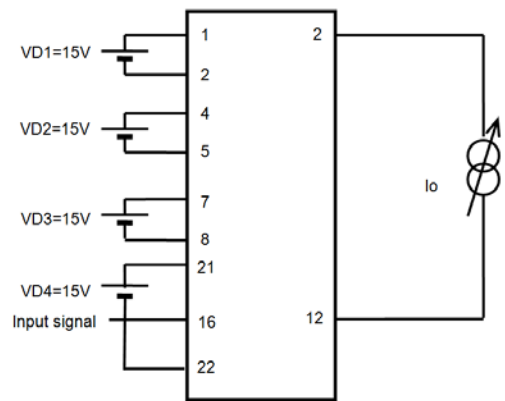
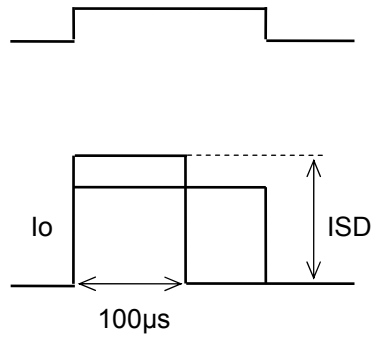


Fig. 5

■ Switching time (The circuit is a representative example of the lower side U phase.)

Input signal
(0 to 5V)

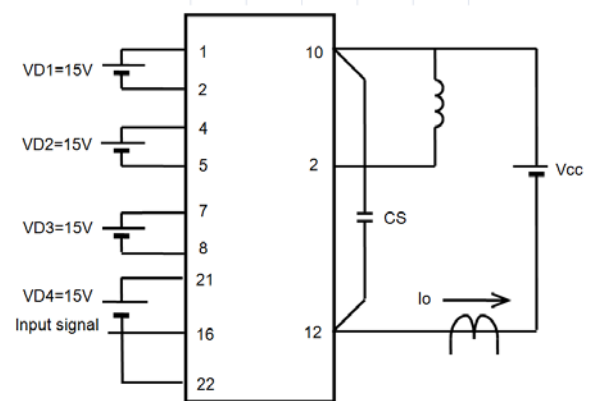
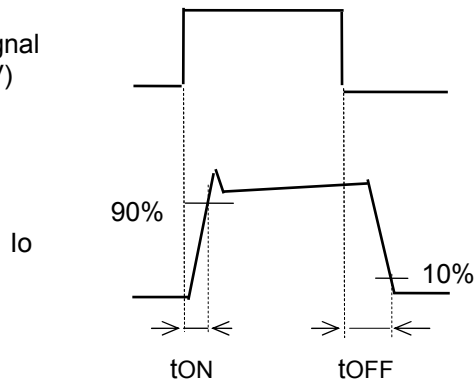


Fig. 6

Logic Timing Chart

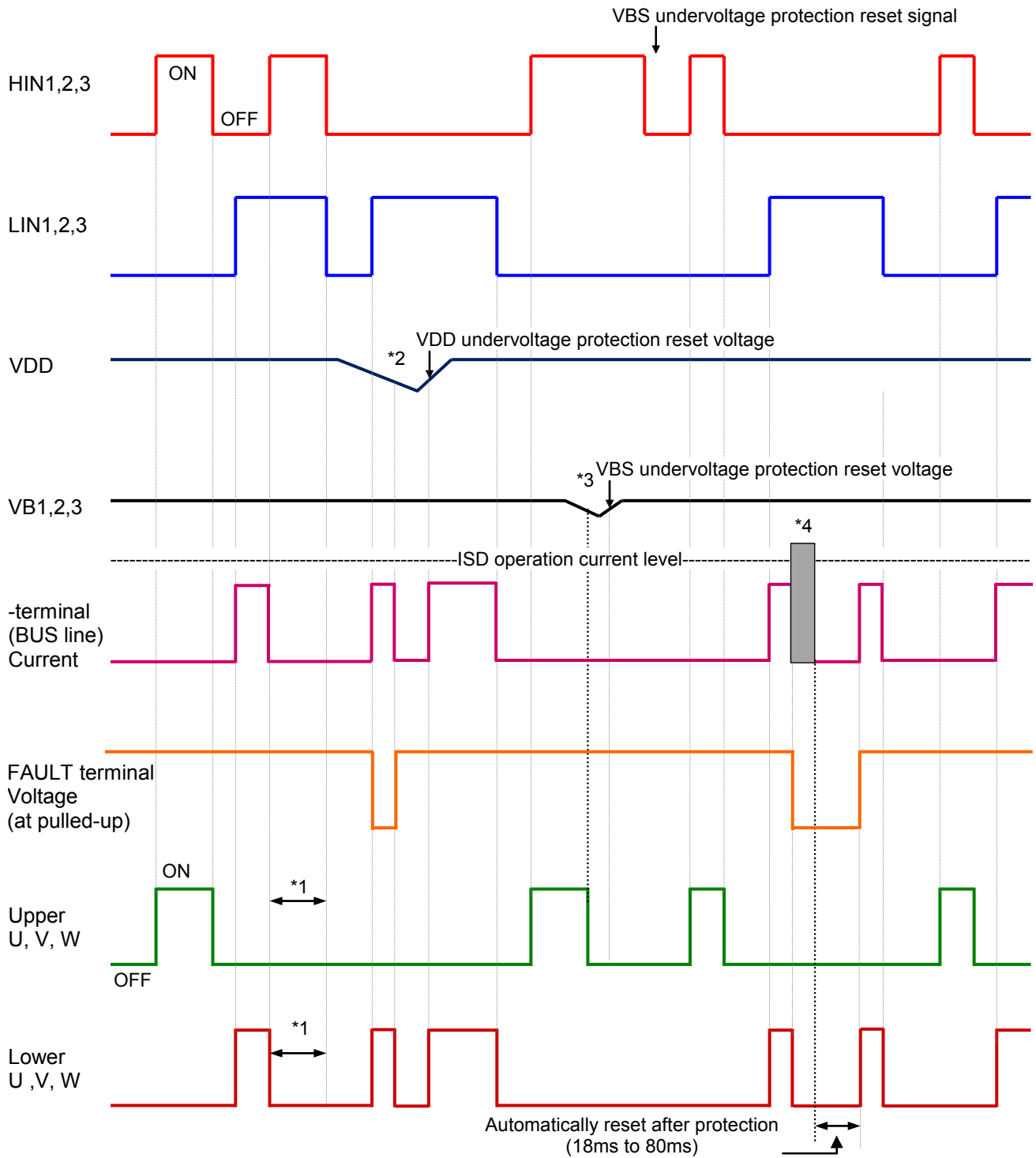


Fig. 7

Notes

- *1 : Diagram shows the prevention of shoot-through via control logic. More dead time to account for switching delay needs to be added externally.
- *2 : When V_{DD} decreases all gate output signals will go low and cut off all of 6 IGBT outputs. When V_{DD} rises the operation will resume immediately.
- *3 : When the upper side gate voltage at VB1, VB2 and VB3 drops only, the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gate voltage rises.
- *4 : In case of over current detection, all IGBT's are turned off and the FAULT output is asserted. Normal operation resumes in 18 to 80ms after the over current condition is removed.

Logic level table

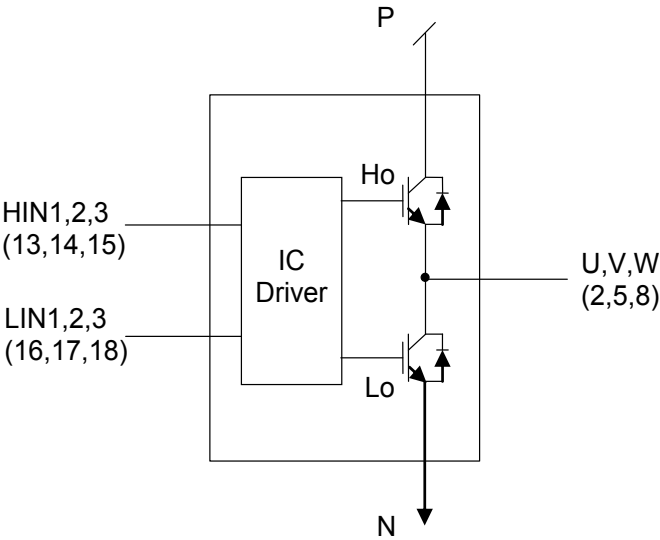


Fig. 8

INPUT			OUTPUT			
HIN	LIN	OCP	Ho	Lo	U, V, W	FAULT
H	L	OFF	H	L	P	OFF
L	H	OFF	L	H	N	OFF
L	L	OFF	L	L	High Impedance	OFF
H	H	OFF	L	L	High Impedance	OFF
X	X	ON	L	L	High Impedance	ON

Sample Application Circuit

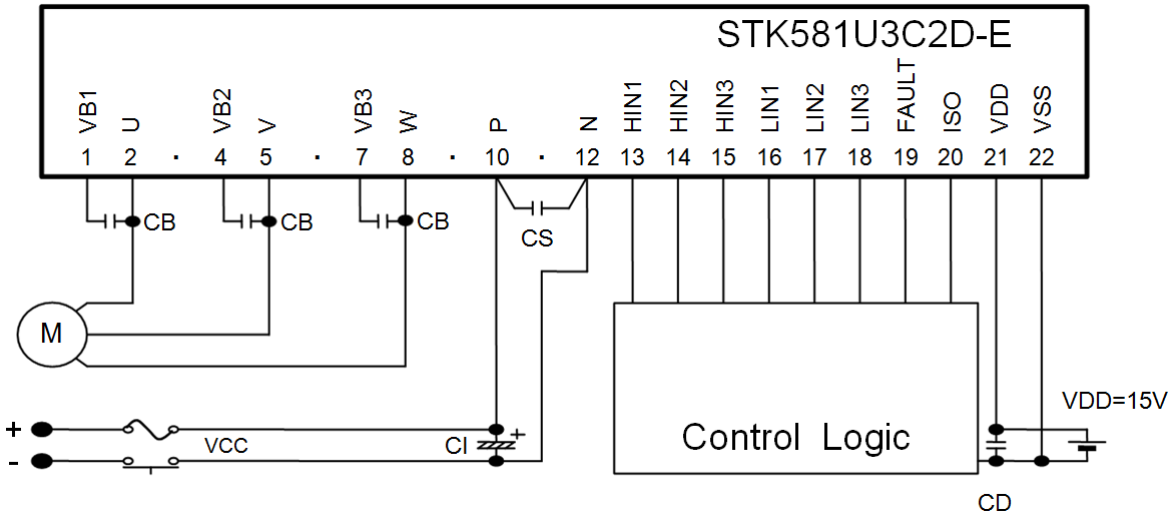


Fig. 9

STK581U3C2D-E

Recommended Operating Conditions at T_c = 25°C

Item	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V _{CC}	P to N	0	280	450	V
Pre-driver supply voltage	VD1, 2, 3	VB1 to U, VB2 to V, VB3 to W	12.5	15	17.5	V
	VD4	V _{DD} to V _{SS} *1	13.5	15	16.5	
ON-state input voltage	V _{IN} (ON)	HIN1, HIN2, HIN3,	3.0	-	5.0	V
OFF-state input voltage	V _{IN} (OFF)	LIN1, LIN2, LIN3	0	-	0.3	
PWM frequency	f _{PWM}		1	-	20	kHz
Dead time	DT	Turn-off to turn-on	2	-	-	μs
Allowable input pulse width	PWIN	ON and OFF	1	-	-	μs
Tightening torque		'M4' type screw	0.79	-	1.17	Nm

*1 Pre-drive power supply (VD4=15±1.5V) must have the capacity of I_o=20mA(DC), 0.5A(Peak).

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Usage Precautions

1. This IPM includes bootstrap diode and resistors. Therefore, by adding a capacitor “CB”, a high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47μF, however this value needs to be verified prior to production. If selecting the capacitance more than 47μF (±20%), connect a resistor (about 20Ω) in series between each 3-phase upper side power supply terminals (VB1, 2, 3) and each bootstrap capacitor.
When not using the bootstrap circuit, each upper side pre-drive power supply requires an external independent power supply.
2. It is essential that wiring length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of “CS” is in the range of 0.1 to 10μF.
3. “ISO” (pin20) is terminal for current monitor. When the pull-down resistor is used, please select it more than 5.6kΩ
4. “FAULT” (pin19) is open DRAIN output terminal (Active Low). Pull up resistor is recommended more than 5.6kΩ.
5. Inside the IPM, a thermistor used as the temperature monitor for internal substrate is connected between VSS terminal and TH terminal, therefore, an external pull up resistor connected between the TH terminal and an external power supply should be used. The temperature monitor example application is as follows, please refer the Fig.10, and Fig.11 below.
6. Pull down resistor of 33kΩ is provided internally at the signal input terminals. An external resistor of 2.2k to 3.3kΩ should be added to reduce the influence of external wiring noise.
7. The over-current protection feature is not intended to protect in exceptional fault condition. An external fuse is recommended for safety.
8. When input pulse width is less than 1.0μs, an output may not react to the pulse. (Both ON signal and OFF signal)

This data shows the example of the application circuit, does not guarantee a design as the mass production set.

The characteristic of thermistor

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resistance	R ₂₅	T _c = 25°C	99	100	101	kΩ
Resistance	R ₁₀₀	T _c = 100°C	5.12	5.38	5.66	kΩ
B-Constant (25 to 50 °C)	B		4165	4250	4335	K
Temperature Range			-40	-	+125	°C

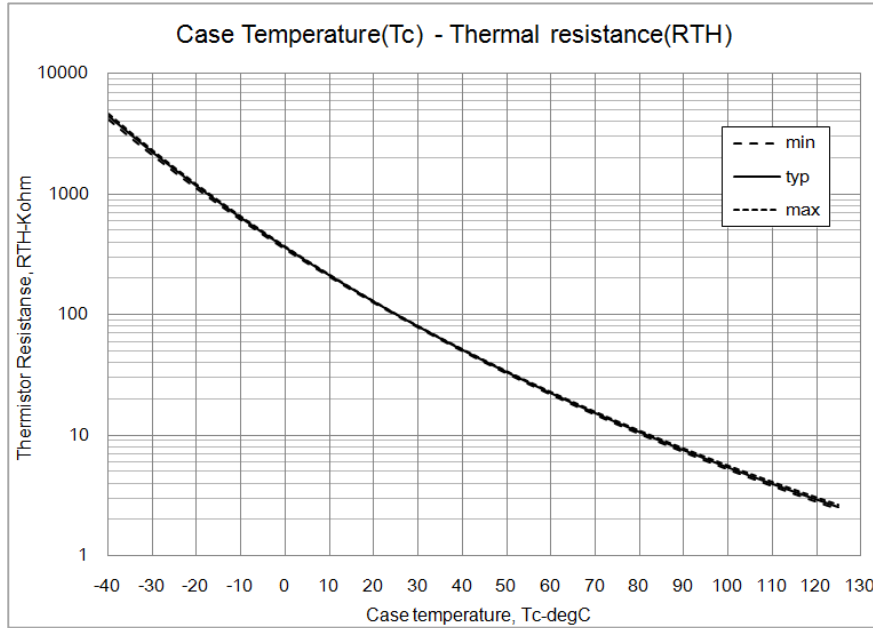


Fig. 10

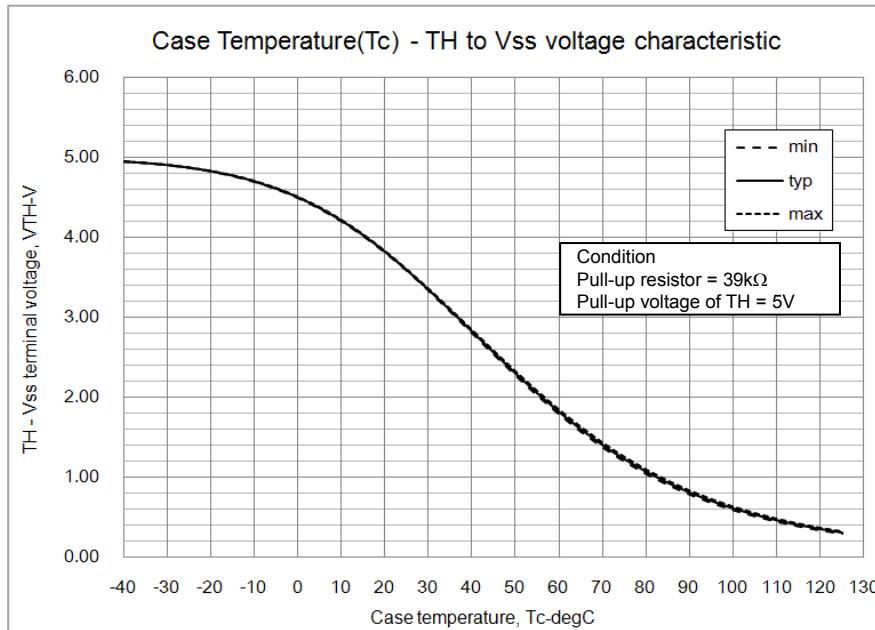


Fig. 11

The characteristic of PWM switching frequency

Maximum sinusoidal phase current as function of switching frequency ($V_{BUS}=300V$, $T_c=100^\circ C$)

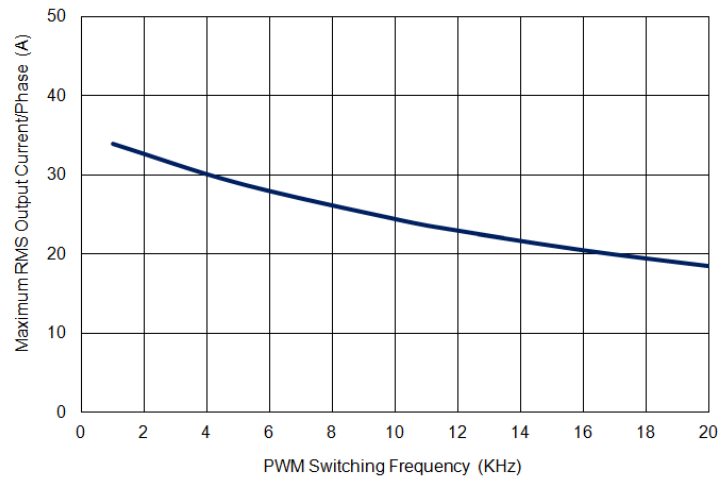


Fig.12

Switching waveform

IGBT Turn-on. Typical turn-on waveform @ $T_c=100^\circ C$, $V_{BUS}=400V$

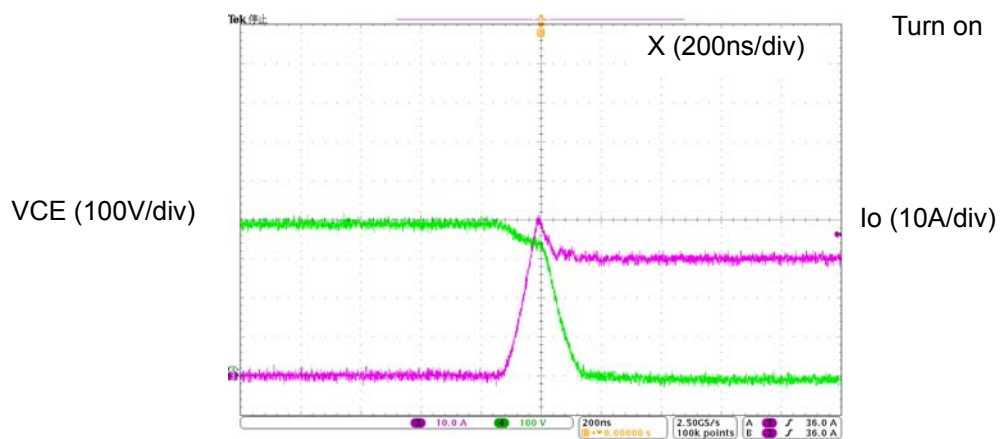


Fig. 13

IGBT Turn-off. Typical turn-off waveform @ $T_c=100^\circ C$, $V_{BUS}=400V$

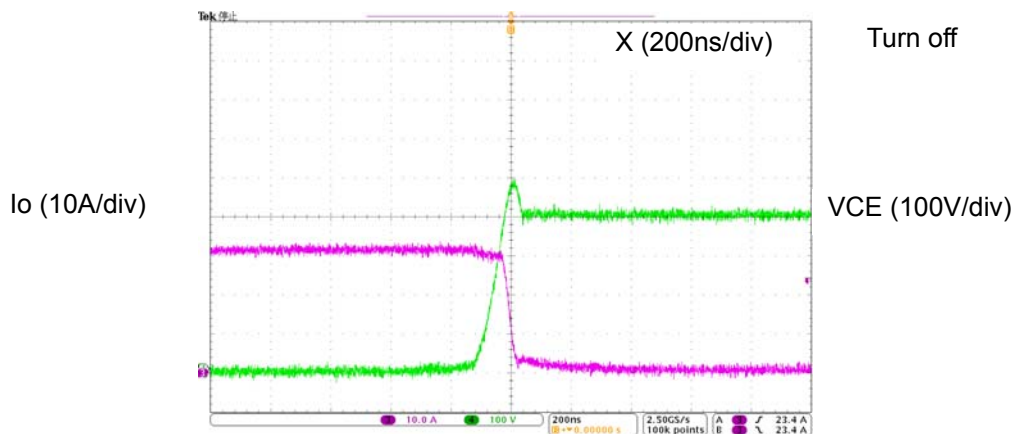


Fig. 14

CB capacitor value calculation for bootstrap circuit

Calculate condition

Item	Symbol	Value	Unit
Upper side power supply.	VBS	15	V
Total gate charge of output power IGBT at 15V.	Qg	266	nC
Upper side power supply low voltage protection.	UVLO	12	V
Upper side power dissipation.	IDmax	400	μA
ON time required for CB voltage to fall from 15V to UVLO	Tonmax	-	s

Capacitance calculation formula

CB must not be discharged below to the upper limit of the UVLO - the maximum allowable on-time (Tonmax) of the upper side is calculated as follows:

$$\begin{aligned} VBS * CB - Qg - IDmax * Tonmax &= UVLO * CB \\ CB &= (Qg + IDmax * Tonmax) / (VBS - UVLO) \end{aligned}$$

The relationship between Tonmax and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47μF, however, the value needs to be verified prior to production.

Tonmax-CB characteristic

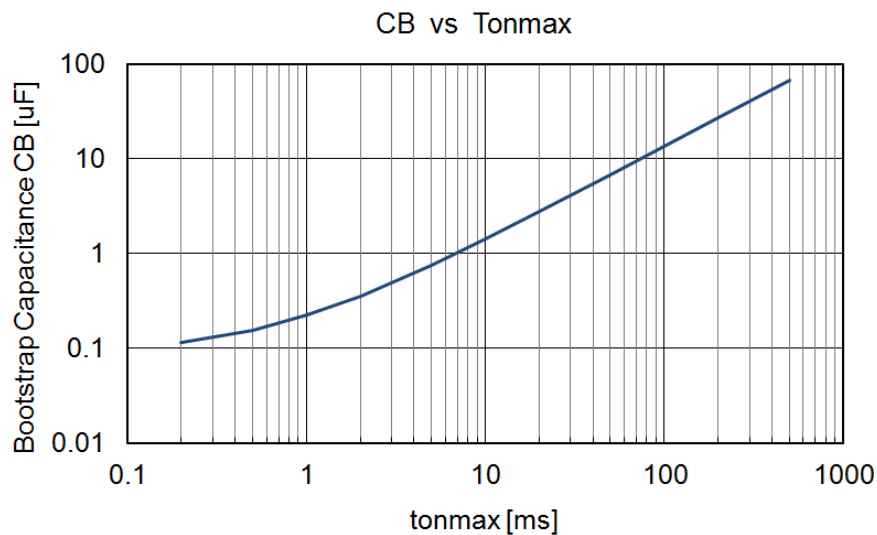


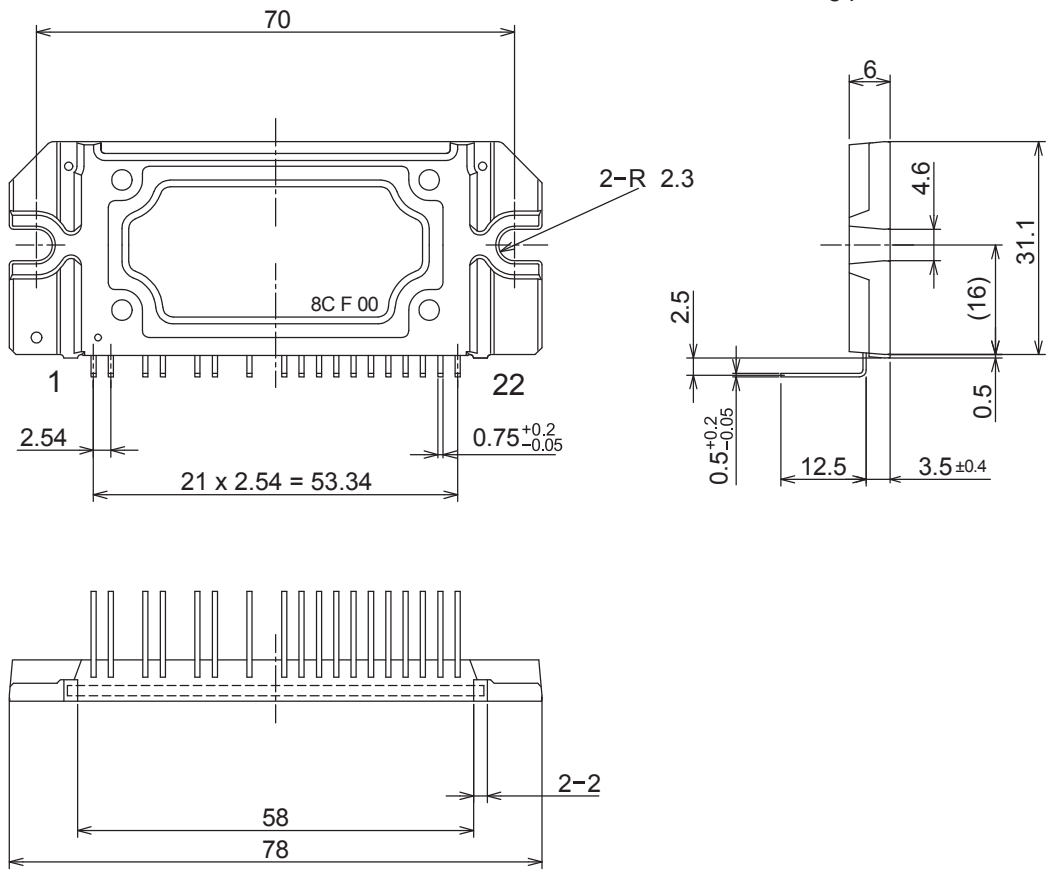
Fig 15

Package Dimensions

unit : mm

SIP22 70x31.1
CASE 127BU
ISSUE 0

Missing pin : 3, 6, 9, 11



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK581U3C2D-E	SIP22 70x31.1 (Pb-Free)	7 / Tube

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