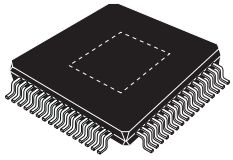
L6460

SPI configurable stepper and DC multi motor driver

Data brief

Features

- Operating voltage supply from 13 V to 40 V
- 4 full bridge driver configurable in multi-motor application to drive:
  - 2 DC and 1 stepper motor
  - 4 DC motor
- Bridge 1 and 2 (R_{DSon} = 0.60 Ω) can be configured to work as:
  - Dual full bridge driver
  - Super DC driver
  - 2 half bridge driver
  - 1 super half bridge
  - 2 power switches
  - 1 super power switch
- Bridge 3 and 4 (R_{DSon} = 0.75 Ω) can be configured to work as:
  - Same as bridges 1 and 2, listed above
  - 2 buck regulators (bridge 3)
  - 1 super buck regulator
  - Battery charger (bridge 4)
- Power supply management
  - One switching buck regulator
  - One switching regulator controller
  - One linear regulator
  - One battery charger
- Fully protected through
  - Thermal warning and shutdown
  - Overcurrent protection
  - Undervoltage lock-out
- 16 bit SPI interface
- Programmable watchdog function
- Integrated power sequencing and supervisory functions with fault signaling through serial interface and external reset pin
- Very low power dissipation in shut-down mode (~35 mW)



TQFP64 exposed pad

- Aux features
  - Multi-channels 9 bit ADC
  - 2 operational amplifiers
  - Digital comparator
  - 2 low voltage power switches
  - 3 general purpose PWM generators
  - 14 GPIOs

Description

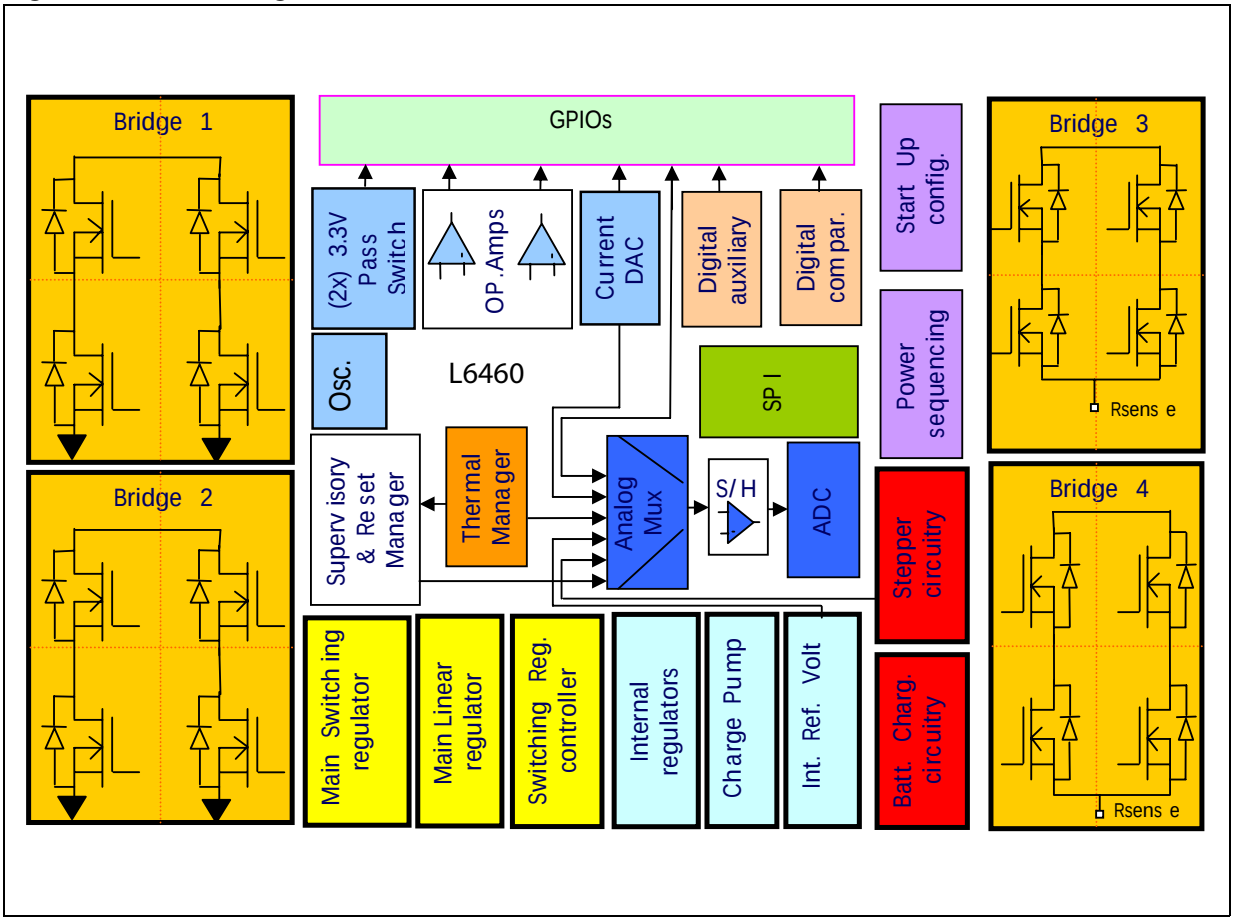
The L6460 is optimized to control and drive multi-motor system providing a unique level of integration in term of control, power and auxiliary features. Thanks to the high configurability L6460 can be customized to drive different motor architectures and to optimize the number of embedded features, such as the voltage regulators, the high precision A/D converter, the OP amp and the voltage comparators. The possibility to drive simultaneously stepper and DC motor makes L6460 the ideal solution for all the application featuring multi motors.

Table 1. Device summary

Order code	Package	Packing
L6460	TQFP64	Tray

1 Block diagram

Figure 1. Block diagram



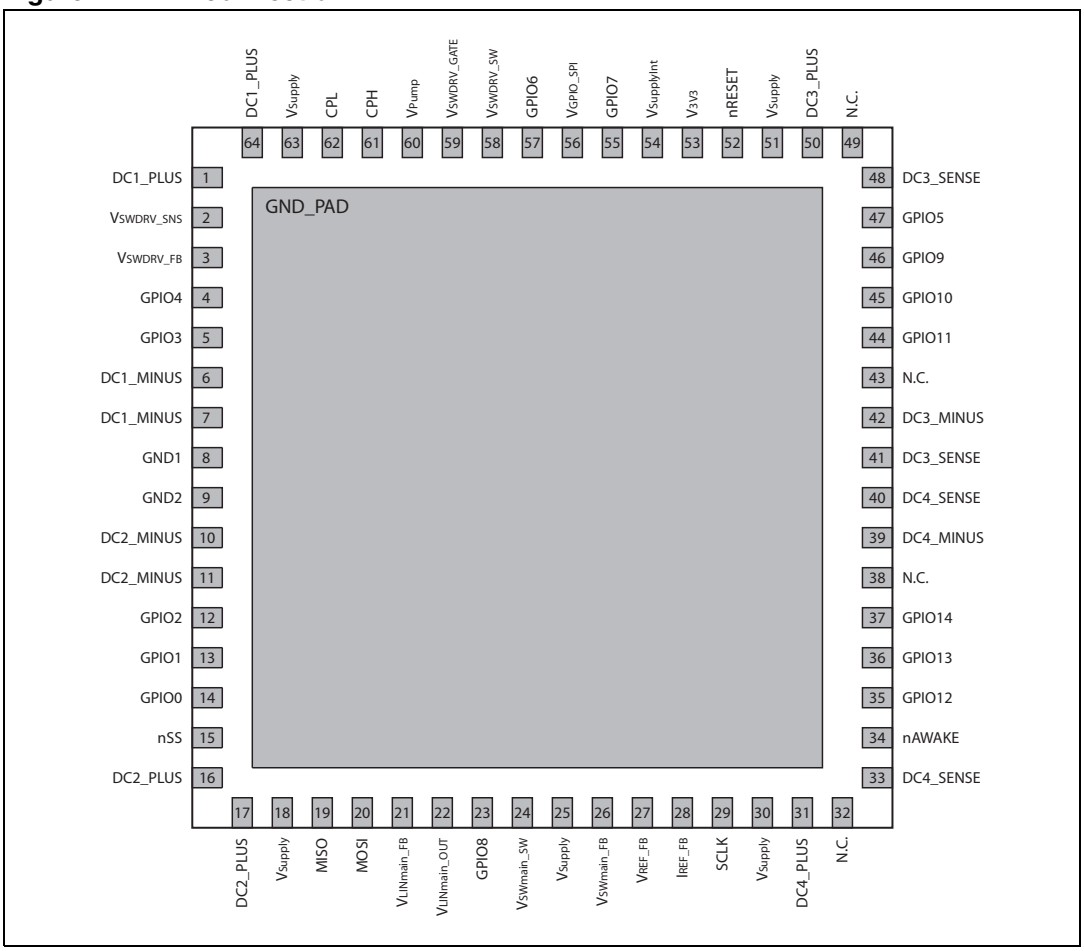
1.1 Functional description

L6460 offers the possibility to control and power multi motor systems, through the management of simultaneous driving of stepper and DC motor. A number of features can be configured through the digital interface (SPI), including 3 voltage regulators, 1 high precision A/D converter, 2 operational amplifiers and 14 configurable GPIOs.

The high flexibility allows the possibility to configure two, one full or half bridge to work as power stage featuring additional voltage buck regulators.

1.2 Pin connection

Figure 2. Pin connection



1.3 Pin list

Table 2. Pins configuration

Pin #	Pin name	Description	Type
1	DC1_PLUS	Bridge 1 phase “plus” output	Output
2	V_{SWDRV_SNS}	Switching regulator controller sense	Analog input
3	V_{SWDRV_FB}	Switching regulator controller feedback	Analog input
4	GPIO4	General purpose I/O	Analog In/Out - CMOS bi-dir
5	GPIO3	General purpose I/O	Analog In/Out - CMOS bi-dir
6	DC1_MINUS	Bridge 1 phase “minus” output	Output
7	DC1_MINUS	Bridge 1 phase “minus” output	Output
8	GND1	Ground pin for bridge1 (1)(2)(3)	Power/digital
9	GND2	Ground pin for bridge2 (1)(2)(3)	Power/digital

Table 2. Pins configuration (continued)

Pin #	Pin name	Description	Type
10	DC2_MINUS	Bridge 2 phase “minus” output	Output
11	DC2_MINUS	Bridge 2 phase “minus” output	Output
12	GPIO2	General purpose I/O	Analog In/Out - CMOS bi-dir
13	GPIO1	General purpose I/O	Analog In/Out - CMOS bi-dir
14	GPIO0	General purpose I/O	Analog Input - CMOS input
15	nSS	SPI chip select pin	CMOS input
16	DC2_PLUS	Bridge 2 phase “plus” output	Output
17	DC2_PLUS	Bridge 2 phase “plus” output	Output
18	V_{Supply}	Main voltage supply	Power input
19	MISO	SPI serial data output	CMOS output
20	MOSI	SPI serial data input	CMOS input
21	$V_{LINmain\_FB}$	Linear main regulator feedback	Analog input
22	$V_{LINmain\_OUT}$	Linear main regulator output	Power output
23	GPIO 8	General purpose I/O	Analog In/Out - CMOS bi-dir
24	V_{SWmain_SW}	Main switching regulator switching output	Power output
25	V_{Supply}	Main voltage supply	Power Input
26	V_{SWmain_FB}	Main switching regulator feedback pin	Analog input
27	V_{REF_FB}	Regulator voltage feedback	Analog input
28	I_{REF_FB}	Regulator current feedback	Analog input
29	SCLK	SPI input clock pin	CMOS input
30	V_{Supply}	Main voltage supply	Power input
31	DC4_PLUS	Bridge 4 phase “plus” output	Output
32	N.C.	Not connected	
33	DC4_SENSE	Bridge 4 sense output(4)	Output
34	nAWAKE	Device wake up	CMOS input
35	GPIO12	General purpose I/O	Analog In/Out - CMOS bi-dir
36	GPIO13	General purpose I/O	Analog In/Out - CMOS bi-dir
37	GPIO14	General purpose I/O	Analog In/Out - CMOS bi-dir
38	N.C.	Not connected	
39	DC4_MINUS	Bridge 4 phase “minus” output	Output
40	DC4_SENSE	Bridge 4 sense output(4)	Output
41	DC3_SENSE	Bridge 3 sense output(4)	Output
42	DC3_MINUS	Bridge 3 phase “minus” output	Output
43	N.C.	Not connected	
44	GPIO11	General purpose I/O	Analog In/Out - CMOS bi-dir

Table 2. Pins configuration (continued)

Pin #	Pin name	Description	Type
45	GPIO10	General purpose I/O	Analog In/Out - CMOS bi-dir
46	GPIO9	General purpose I/O	Analog In/Out - CMOS bi-dir
47	GPIO5	General purpose I/O	Analog In/Out - CMOS bi-dir
48	DC3_SENSE	Bridge 3 sense output(4)	Output
49	N.C.	Not connected	
50	DC3_PLUS	Bridge 3 phase “plus” output	Output
51	V_{Supply}	Main voltage supply	Power input
52	nRESET	Open drain system reset pin	CMOS Input/output
53	V_{3v3}	Internal 3.3 volt regulator	Power Input/output
54	$V_{SupplyInt}$	Internal voltage supply	Power Input
55	GPIO7	General purpose I/O	Analog In/Out - CMOS bi-dir
56	V_{GPIO_SPI}	Low voltage pins power supply	Power input
57	GPIO6	General purpose I/O	Analog In/Out - CMOS bi-dir
58	V_{SWDRV_SW}	Switching regulator controller source input	Power input
59	V_{SWDRV_GATE}	Switching driver gate drive pin	Analog output
60	V_{Pump}	Charge pump voltage	Power Input/output
61	CPH	Charge pump high switch pin	Power Input/output
62	CPL	Charge pump low switch pin	Power Input/output
63	V_{Supply}	Main voltage supply	Power input
64	DC1_plus	Bridge 1 phase “plus” output	Output
E_Pad	GND_PAD	(1)(2)(3)	

1. These pins must be connected all together to a unique PCB ground.
2. Bridges1 and 2 have 2 ground pads: one is bonded to the relative ground pin (GND1 or GND2) and the other is connected to exposed pad (E_Pad) ground ring. This makes the bond wires testing possible by forcing a current between E-Pad and GND1 or GND2 pins and using the other pin as sense pin to measure the resistance of E-Pad bonding. (N.B: grounds of two bridges are internally connected together).
3. The analog ground is connected to exposed pad E-Pad.
4. The pin must be tied to ground if bridge is not used as a stepper motor.

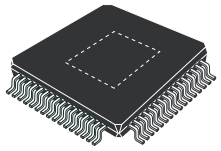
2 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

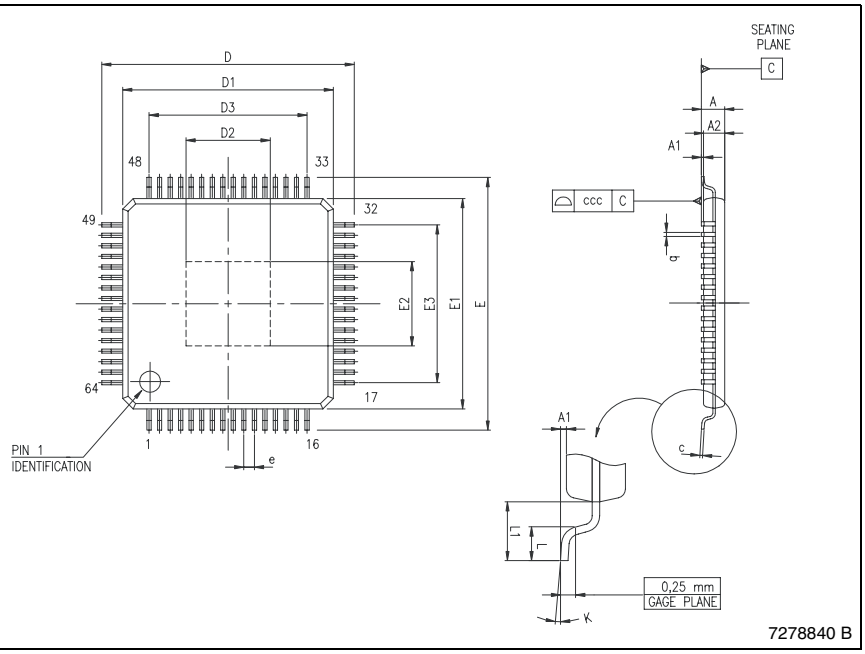
Figure 3. TQFP64 mechanical data an package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.20			0.0472
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.0374	0.0393	0.0413
b	0.17	0.22	0.27	0.0066	0.0086	0.0086
c	0.09		0.20	0.0035		0.0078
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D2	2.00			0.787		
D3		7.50			0.295	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E2	2.00			0.787		
E3		7.50			0.295	
e		0.50			0.0197	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
k	0˚	3.5˚	7˚	0˚	3.5˚	7˚
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



TQFP64 (10x10x1.0mm)
Exposed Pad Down



3 Revision history

Table 3. Document revision history

Date	Revision	Changes
30-Oct-2009	1	Initial release.

AMEYA360
Components Supply Platform

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