TLV733P Capacitor-Free, 300-mA, Low-Dropout Regulator in a 1-mm × 1-mm SON Package

1 Features

- Input Voltage Range: 1.4 V to 5.5 V
- Stable Operation With or Without Capacitors
- Foldback Overcurrent Protection
- Packages:
  - 1.0-mm × 1.0-mm X2SON (4)
  - SOT-23 (5)
- Very Low Dropout: 122 mV at 300 mA (3.3 V_{OUT})
- Accuracy: 1% typical, 1.4% maximum
- Low I_Q: 34 µA
- Available in Fixed-Output Voltages: 1.0 V to 3.3 V
- High PSRR: 50 dB at 1 kHz
- Active Output Discharge

2 Applications

- Tablets
- Smartphones
- Notebook and Desktop Computers
- Portable Industrial and Consumer Products
- WLAN and Other PC Add-On Cards
- Camera Modules

3 Description

The TLV733 series of low-dropout linear regulators (LDOs) are ultra-small, low quiescent current LDOs that can source 300 mA with good line and load transient performance. These devices provide a typical accuracy of 1%.

The TLV733 series is designed with a modern capacitor-free architecture to ensure stability without an input or output capacitor. The removal of the output capacitor allows for a very small solution size, and can eliminate inrush current at startup. However, the TLV733 series is also stable with ceramic output capacitors if an output capacitor is necessary. The TLV733 also provides foldback current control during device power-up and enabling if an output capacitor is used. This functionality is especially important in battery-operated devices.

The TLV733 provides an active pull-down circuit to quickly discharge output loads when disabled.

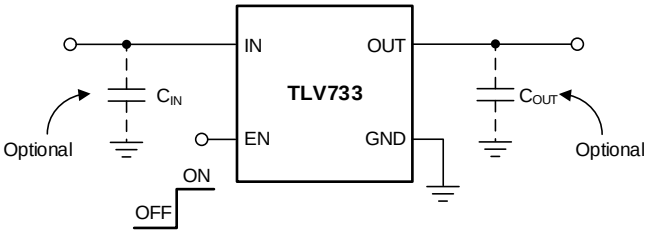
The TLV733 series is available in standard DBV (SOT-23) and DQN (X2SON) packages.

Device Information(1)

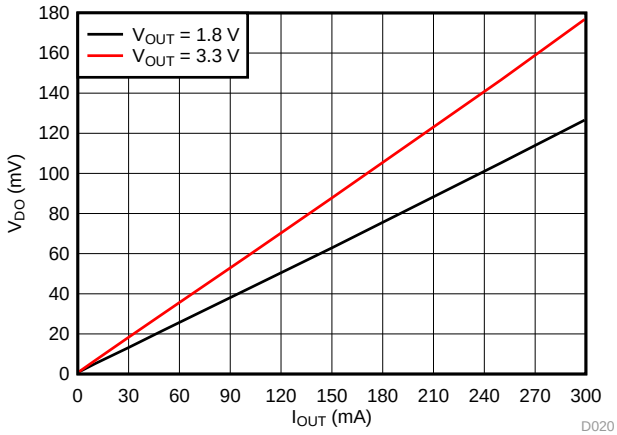
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV733P	SOT-23 (5)	2.90 mm × 1.60 mm
	X2SON (4)	1.00 mm × 1.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Application Circuit



Dropout Voltage vs Output Current



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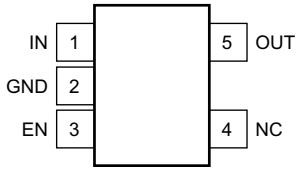
4 Revision History

Changes from Original (October 2014) to Revision A **Page**

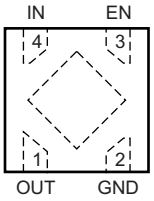
- Changed top page header information for data sheet to reflect device family instead of individual devices ... 1
- Changed Input Voltage Range Features bullet to be first in list ... 1
- Changed *Typical Application Circuit* on front page; corrected error in optional capacitor identification ... 1
- Changed format of I/O column contents and order of packages in *Pin Functions* table ... 3
- Moved storage temperature range specification to *Absolute Maximum Ratings* table ... 4
- Changed *Handling Ratings* table title to *ESD Ratings*, updated table format ... 4
- Added new first row to the V_{DO} parameter in the *Electrical Characteristics* table ... 5
- Changed condition text for Figure 34 ... 16
- Added *Evaluation Module* subsection ... 20
- Deleted *Related Links* section ... 20

5 Pin Configuration and Functions

DBV Package
SOT-23-5
(Top View)



DQN Package
1-mm × 1-mm X2SON-4
(Top View)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO. DQN	NO. DBV		
EN	3	3	I	Enable pin. Drive EN greater than 0.9 V to turn on the regulator. Drive EN less than 0.35 V to put the LDO into shutdown mode.
GND	2	2	—	Ground pin
IN	4	1	I	Input pin. A small capacitor is recommended from this pin to ground. See the *Input and Output Capacitor Selection* section for more details.
NC	N/A	4	—	No internal connection
OUT	1	5	O	Regulated output voltage pin. For best transient response, use a small 1-µF ceramic capacitor from this pin to ground. See the *Input and Output Capacitor Selection* section for more details.
Thermal pad		—	—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted); all voltages are with respect to GND(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6.0	V
	V_{EN}	–0.3	V_{IN} + 0.3 V	V
	V_{OUT}	–0.3	3.6	V
Current	I_{OUT}	Internally limited		A
Output short-circuit duration		Indefinite		
Temperature	Storage temperature range, T_{stg}	–65	150	°C
	Operating junction range, T_J	–55	160	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input range, V_{IN}	1.4		5.5	V
Output range, V_{OUT}	1.0		3.3	V
Output current, I_{OUT}	0		300	mA
Enable range, V_{EN}	0		V_{IN}	V
Junction temperature, T_J	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV733xxP		UNIT
		DQN (X2SON)	DBV (SOT-23)	
		4 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	218.6	228.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	164.8	151.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	164.9	55.8	
ψ_{JT}	Junction-to-top characterization parameter	5.6	31.4	
ψ_{JB}	Junction-to-board characterization parameter	163.9	54.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	131.4	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At operating temperature range (T_J = –40°C to 125°C), V_{IN} = V_{OUT}nom + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF, unless otherwise noted. All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			1.4		5.5	V
	DC output accuracy	T_J = 25°C		–1%		1%	
		–40°C ≤ T_J ≤ 125°C		–1.4%		1.4%	
UVLO	Undervoltage lockout	V_{IN} rising			1.3	1.4	V
		V_{IN} falling			1.25		V
$\Delta V_{O(\Delta VI)}$	Line regulation				1		mV/V
$\Delta V_{O(\Delta IO)}$	Load regulation	DQN package			16		mV
		DBV package			25		mV
V_{DO}	Dropout voltage[1]	V_{OUT} = 0.98 × V_{OUT}nom, I_{OUT} = 300 mA	V_{OUT} = 1.1 V, –40°C ≤ T_J ≤ 85°C			460	mV
			1.2 V ≤ V_{OUT} < 1.5 V, –40°C ≤ T_J ≤ 85°C			420	mV
			1.5 V ≤ V_{OUT} < 1.8 V, –40°C ≤ T_J ≤ 85°C			370	mV
			1.8 V ≤ V_{OUT} < 2.5 V, –40°C ≤ T_J ≤ 85°C			270	mV
			2.5 V ≤ V_{OUT} < 3.3 V, –40°C ≤ T_J ≤ 85°C			260	mV
			V_{OUT} = 3.3 V, –40°C ≤ T_J ≤ 85°C		125	220	mV
			1.2 V ≤ V_{OUT} < 1.5 V, –40°C ≤ T_J ≤ 125°C			450	mV
			1.5 V ≤ V_{OUT} < 1.8 V, –40°C ≤ T_J ≤ 125°C			400	mV
			1.8 V ≤ V_{OUT} < 2.5 V, –40°C ≤ T_J ≤ 125°C			300	mV
			2.5 V ≤ V_{OUT} < 3.3 V, –40°C ≤ T_J ≤ 125°C			290	mV
			V_{OUT} = 3.3 V, –40°C ≤ T_J ≤ 125°C		125	270	mV
I_{GND}	Ground pin current	I_{OUT} = 0 mA			34	60	µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.35 V, 2.0 V ≤ V_{IN} ≤ 5.5 V, T_J = 25°C			0.1	1	µA
PSRR	Power-supply rejection ratio	V_{OUT} = 1.8 V, I_{OUT} = 300 mA	f = 100 Hz		68		dB
			f = 10 kHz		35		dB
			f = 100 kHz		28		dB
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			120		μV_{RMS}
$V_{EN(HI)}$	EN pin high voltage (enabled)			0.9	0.63		V
$V_{EN(LO)}$	EN pin low voltage (disabled)				0.52	0.35	V
I_{EN}	EN pin current	V_{EN} = 5.5 V			0.01		µA
t_{STR}	Startup time	Time from EN assertion to 98% × V_{OUT}nom, V_{OUT} = 1.0 V, I_{OUT} = 0 mA			250		µs
		Time from EN assertion to 98% × V_{OUT}nom, V_{OUT} = 3.3 V, I_{OUT} = 0 mA			800		µs
	Pull-down resistor	V_{IN} = 2.3 V			120		Ω
I_{LIM}	Output current limit			360			mA
I_{OS}	Short-circuit current limit	V_{OUT} shorted to GND, V_{OUT} = 1.0 V			150		mA
		V_{OUT} shorted to GND, V_{OUT} = 3.3 V			170		mA
T_{sd}	Thermal shutdown	Shutdown, temperature increasing			160		°C
		Reset, temperature decreasing			140		°C

(1) Dropout voltage for the TLV73310P is not valid at room temperature. The device engages undervoltage lockout (V_{IN} < $UVLO_{FALL}$) before the dropout condition is met.

6.6 Typical Characteristics

At operating temperature range (T_J = –40°C to 125°C), V_{IN} = V_{OUT}nom + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF, unless otherwise noted.

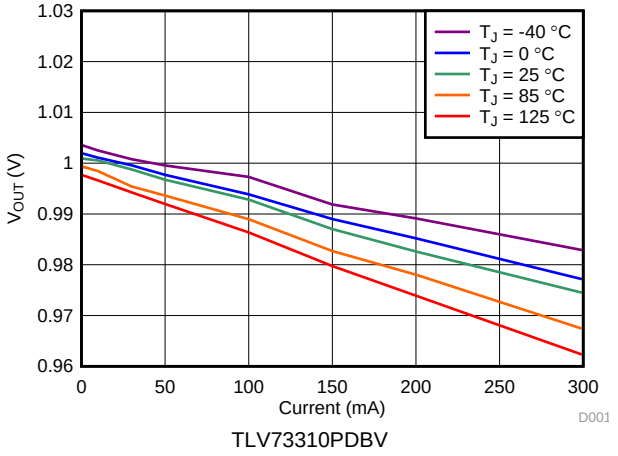


Figure 1. 1.0-V Load Regulation vs I_{OUT} and Temperature

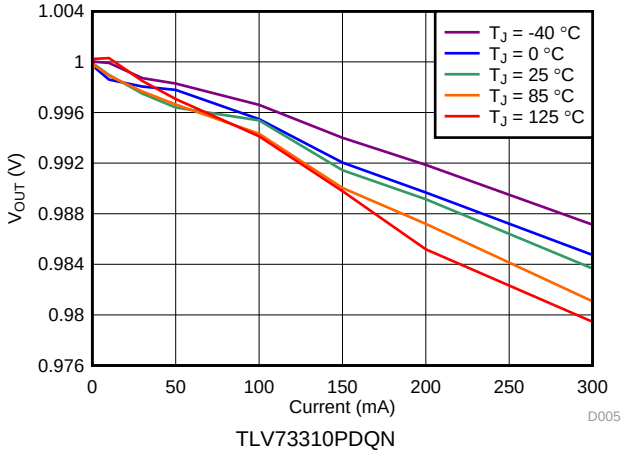


Figure 2. 1.0-V Load Regulation vs I_{OUT} and Temperature

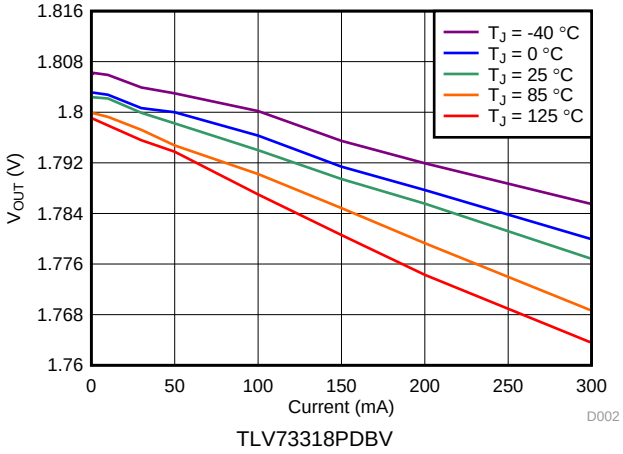


Figure 3. 1.8-V Load Regulation vs I_O and Temperature

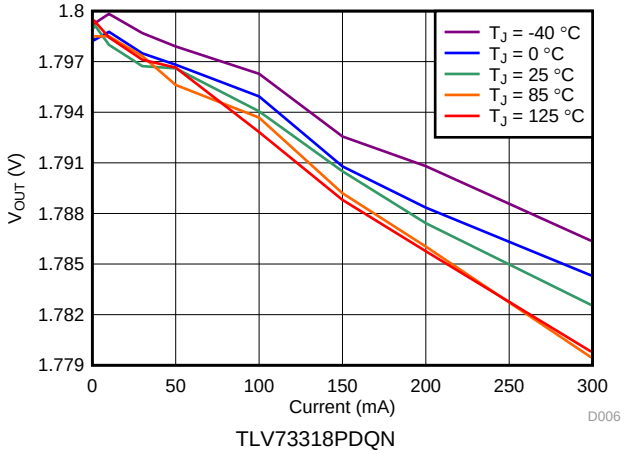


Figure 4. 1.8-V Load Regulation vs I_{OUT} and Temperature

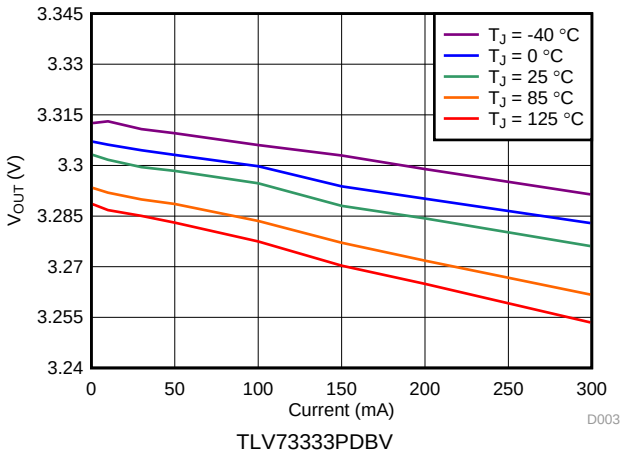


Figure 5. 3.3-V Load Regulation vs I_{OUT} and Temperature

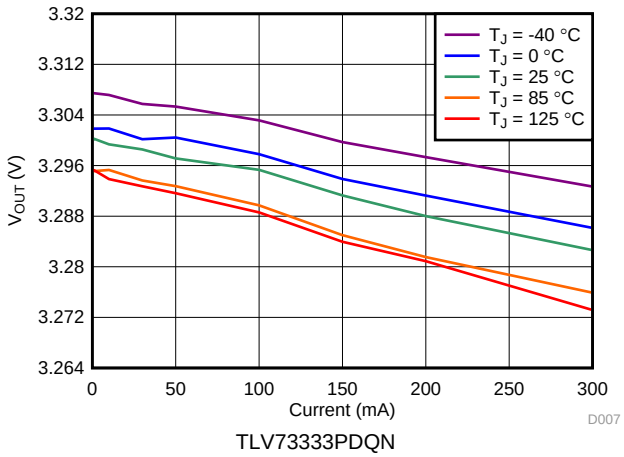


Figure 6. 3.3-V Load Regulation vs I_{OUT} and Temperature

Typical Characteristics (continued)

At operating temperature range (T_J = –40°C to 125°C), V_{IN} = V_{OUT}nom + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF, unless otherwise noted.

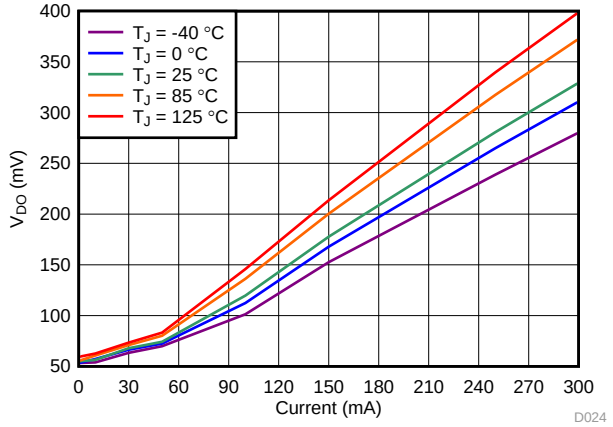


Figure 7. 1.2-V Dropout Voltage vs I_{OUT} and Temperature

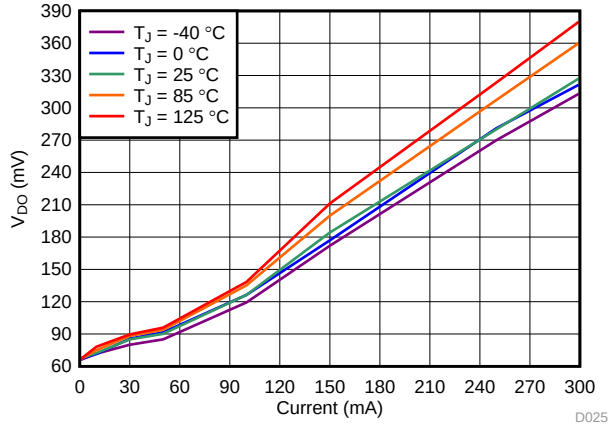


Figure 8. 1.2-V Dropout Voltage vs I_{OUT} and Temperature

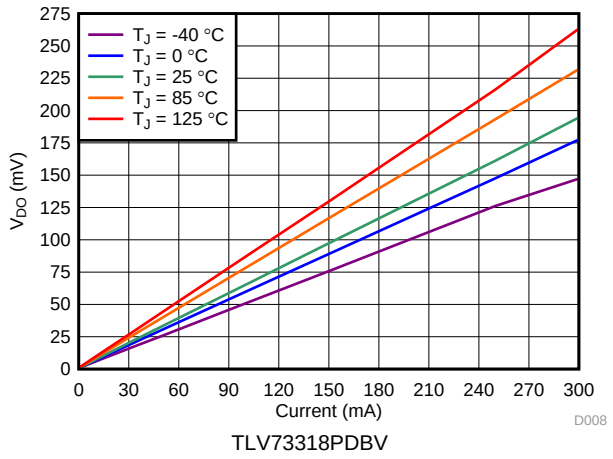


Figure 9. 1.8-V Dropout Voltage vs I_{OUT} and Temperature

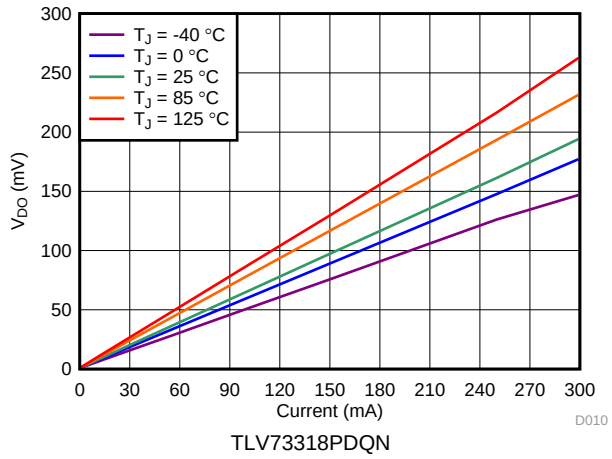


Figure 10. 1.8-V Dropout Voltage vs I_{OUT} and Temperature

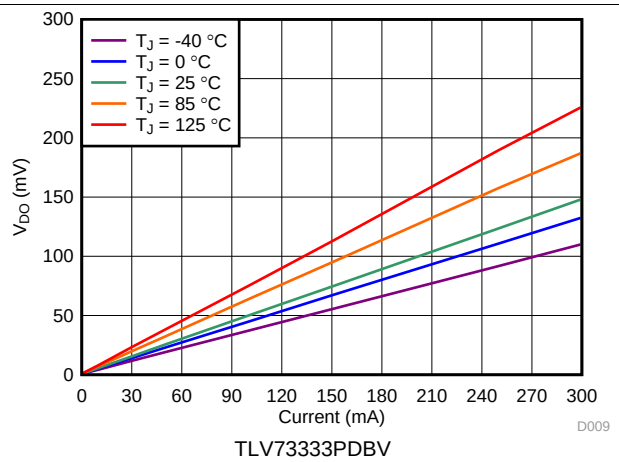


Figure 11. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

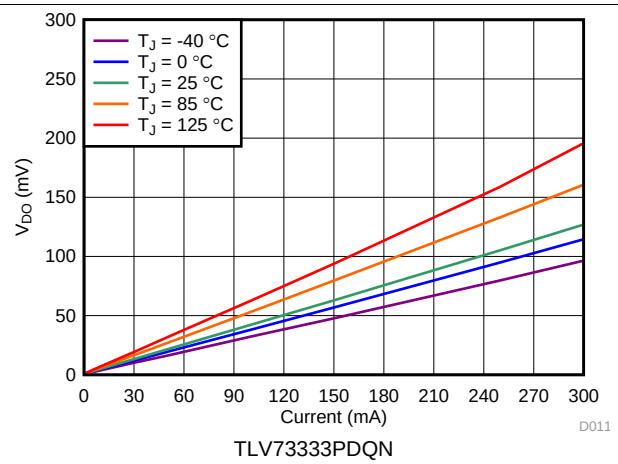


Figure 12. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

Typical Characteristics (continued)

At operating temperature range (T_J = –40°C to 125°C), V_{IN} = V_{OUT}nom + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF, unless otherwise noted.

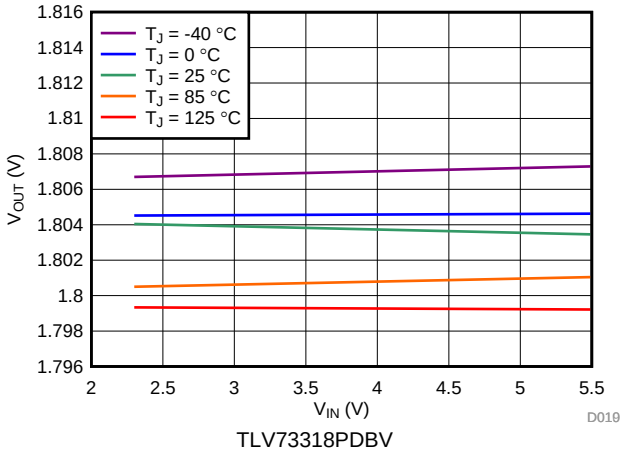


Figure 13. 1.8-V Regulation vs V_{IN} (Line Regulation) and Temperature

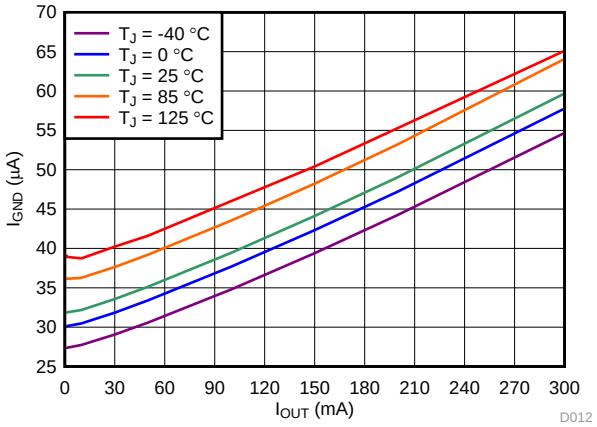


Figure 14. Ground Pin Current vs I_{OUT} and Temperature

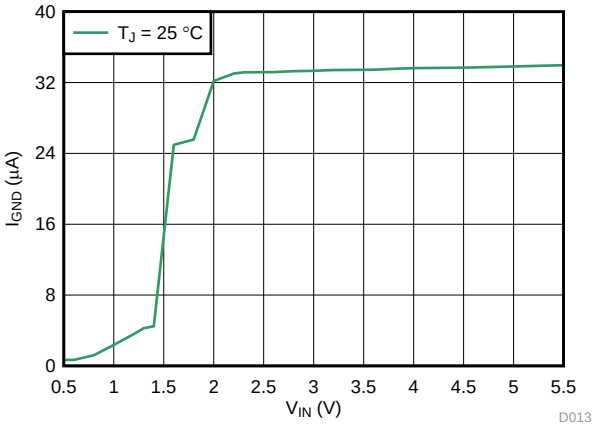


Figure 15. Ground Pin Current vs V_{IN}

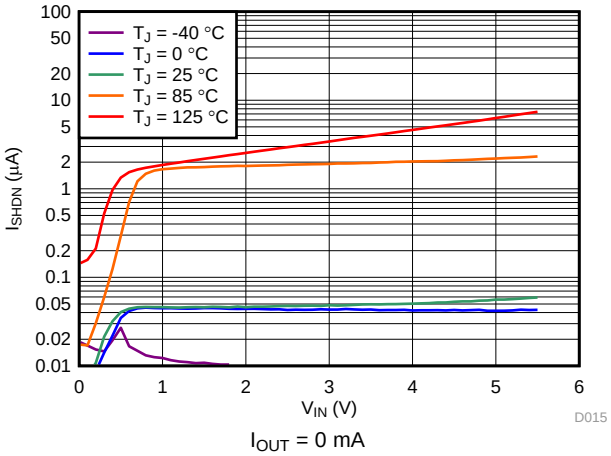


Figure 16. Shutdown Current vs V_{IN} and Temperature

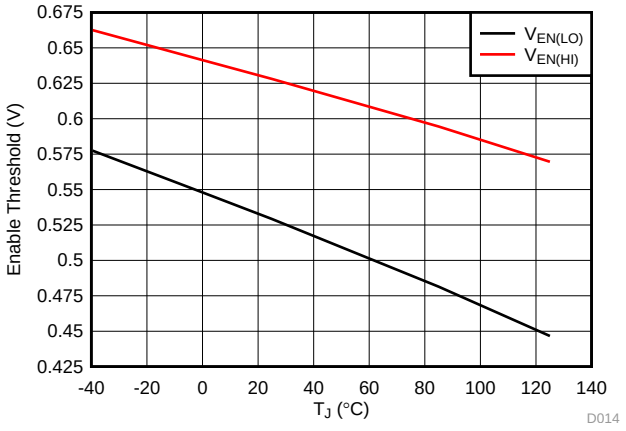


Figure 17. Enable Threshold vs Temperature

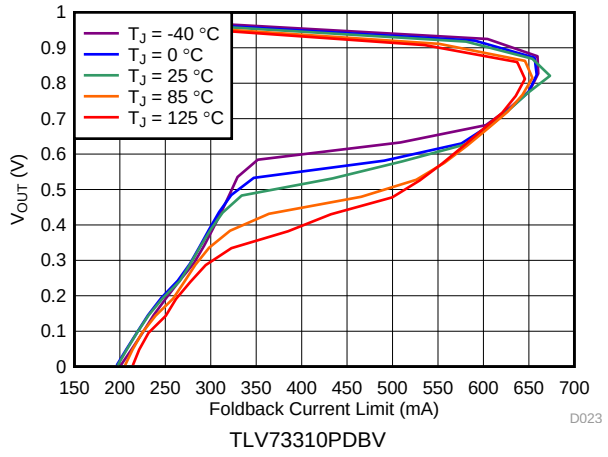
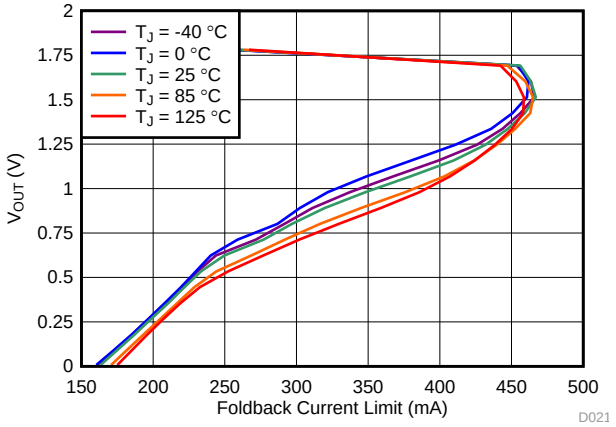


Figure 18. 1.0-V Foldback Current Limit vs I_{OUT} and Temperature

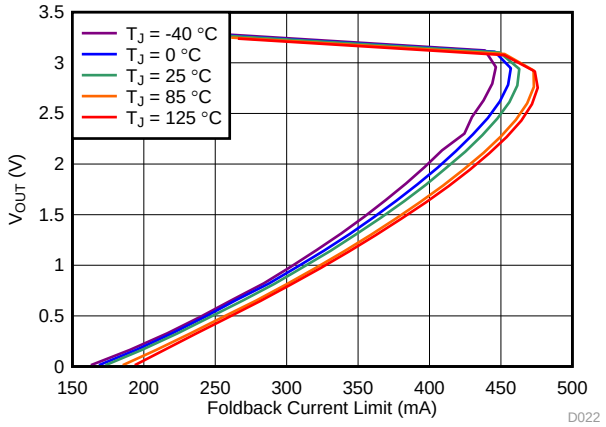
Typical Characteristics (continued)

At operating temperature range (T_J = –40°C to 125°C), V_{IN} = V_{OUT}nom + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF, unless otherwise noted.



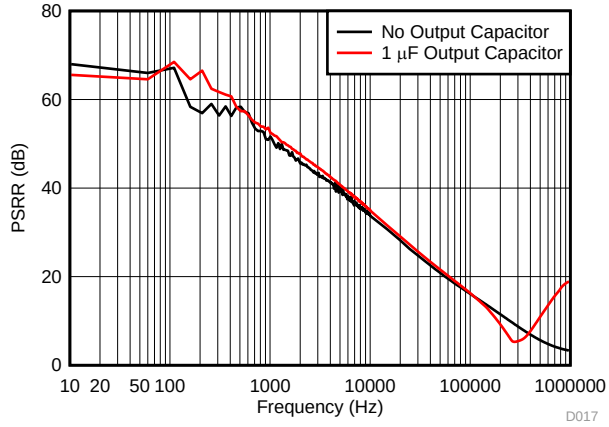
TLV73318PDBV

Figure 19. 1.8-V Foldback Current Limit vs I_{OUT} and Temperature



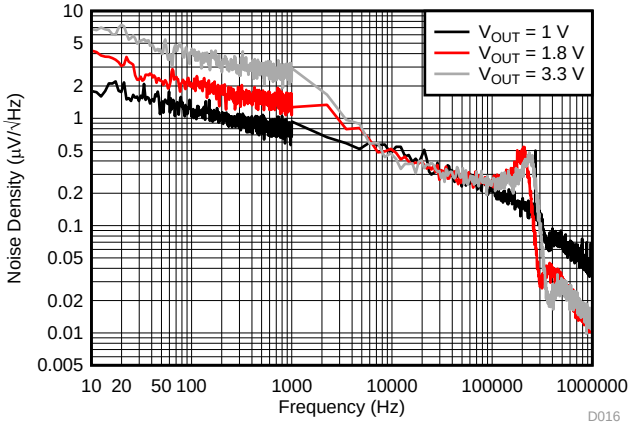
TLV73333PDBV

Figure 20. 3.3-V Foldback Current Limit vs I_{OUT} and Temperature



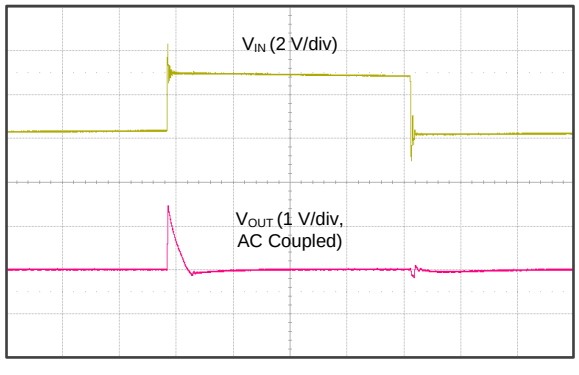
TLV73318PDQN, I_{OUT} = 300 mA

Figure 21. Power-Supply Rejection Ratio vs Frequency



I_{OUT} = 300 mA

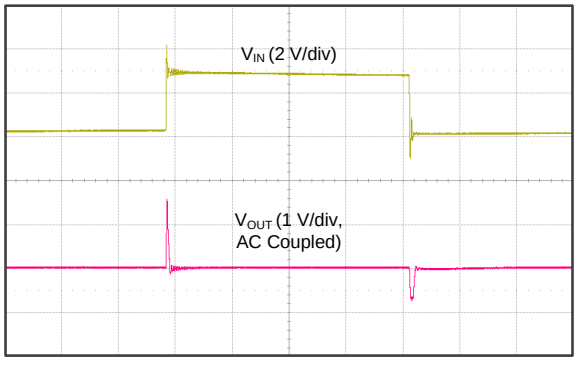
Figure 22. Output Spectral Noise Density



Time (20 µs/div)

TLV73318PDBV, I_{OUT} = 10 mA, 1-µF output capacitor

Figure 23. Line Transient



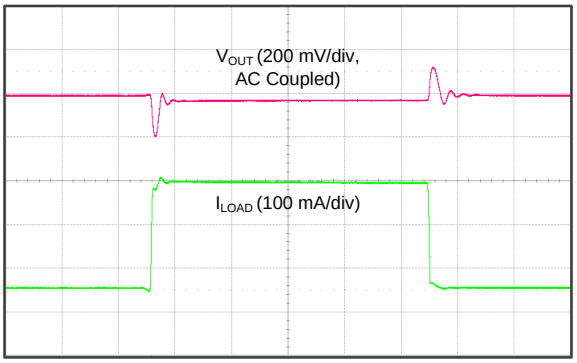
Time (20 µs/div)

TLV73318PDBV, I_{OUT} = 300 mA, 1-µF output capacitor

Figure 24. Line Transient

Typical Characteristics (continued)

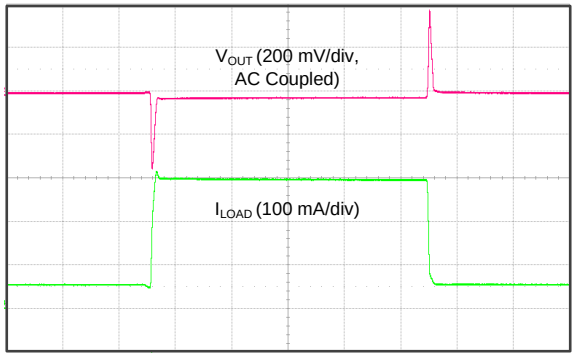
At operating temperature range (T_J = –40°C to 125°C), V_{IN} = V_{OUT}nom + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF, unless otherwise noted.



Time (20 µs/div)

TLV73310PDBV, V_{IN} = 2.0 V, 1-µF output capacitor, output current slew rate = 0.25 A/µs

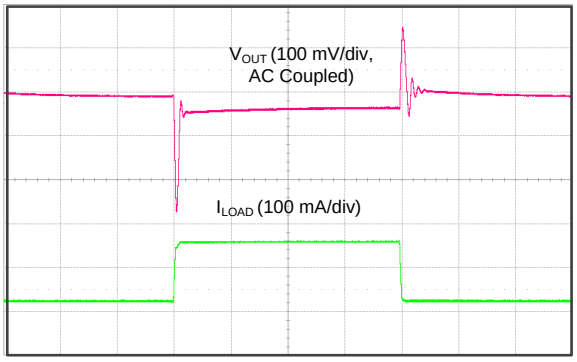
Figure 25. 1.0-V, 50-mA to 300-mA Load Transient



Time (20 µs/div)

TLV73310PDBV, V_{IN} = 2.0 V, no output capacitor, output current slew rate = 0.25 A/µs

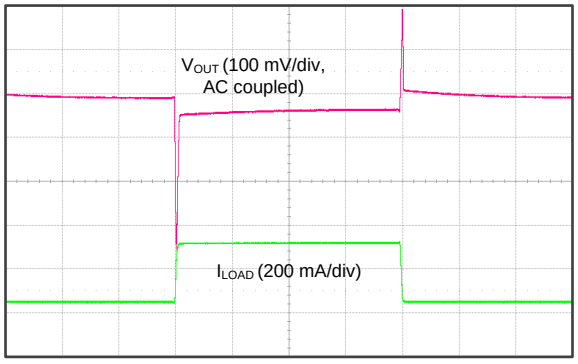
Figure 26. 1.0 V, 50-mA to 300-mA Load Transient



Time (20 µs/div)

TLV73333PDBV, V_{IN} = 3.8 V,1-µF output capacitor, output current slew rate = 0.25 A/µs

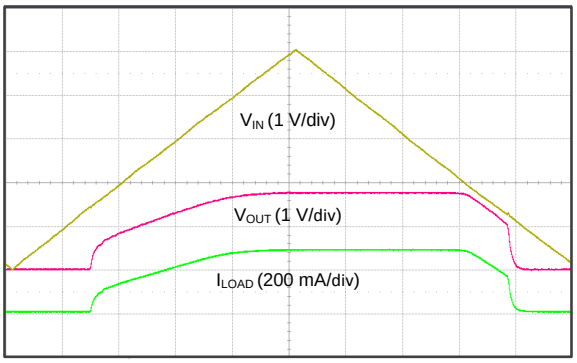
Figure 27. 3.3 V, 50-mA to 300-mA Load Transient



Time (50 µs/div)

TLV73333PDBV, V_{IN} = 3.8 V, no output capacitor, output current slew rate = 0.25 A/µs

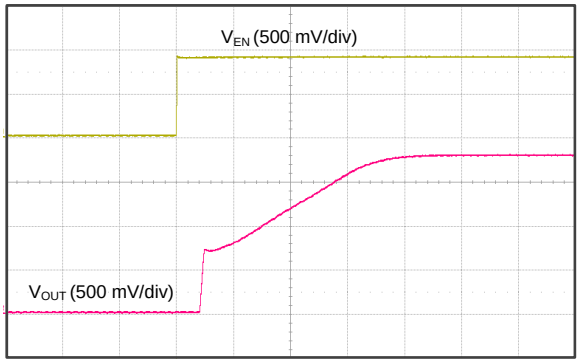
Figure 28. 3.3 V, 50-mA to 300-mA Load Transient



Time (100 µs/div)

TLV73318PDBV, R_L = 6.2 Ω, V_{EN} = V_{IN}, 1-µF output capacitor

Figure 29. V_{IN} Power-Up and Power-Down



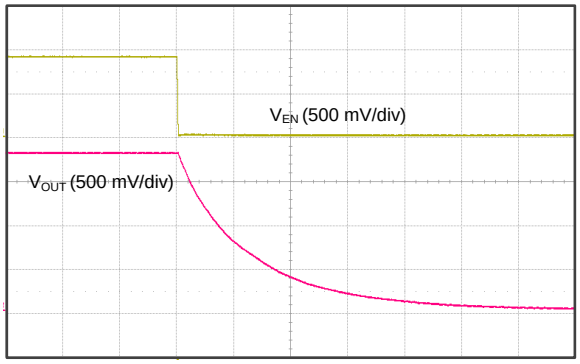
Time (100 µs/div)

TLV73318PDBV, R_L = 6.2 Ω, 1-µF output capacitor

Figure 30. Startup with EN

Typical Characteristics (continued)

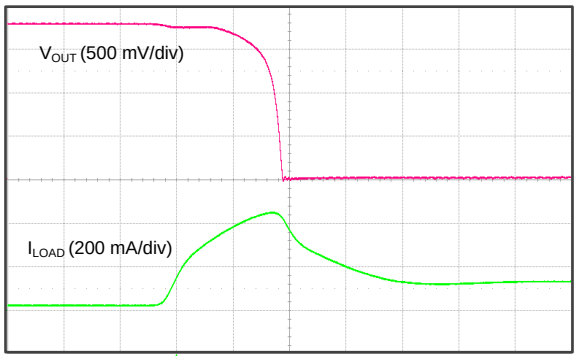
At operating temperature range (T_J = –40°C to 125°C), V_{IN} = V_{OUT}nom + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF, unless otherwise noted.



Time (100 µs/div)

TLV73318PDBV, I_{OUT} = 300 mA, 1-µF output capacitor

Figure 31. Shutdown Response with Enable



Time (100 µs/div)

TLV73318PDBV, 1-µF output capacitor

Figure 32. Foldback Current Limit Response

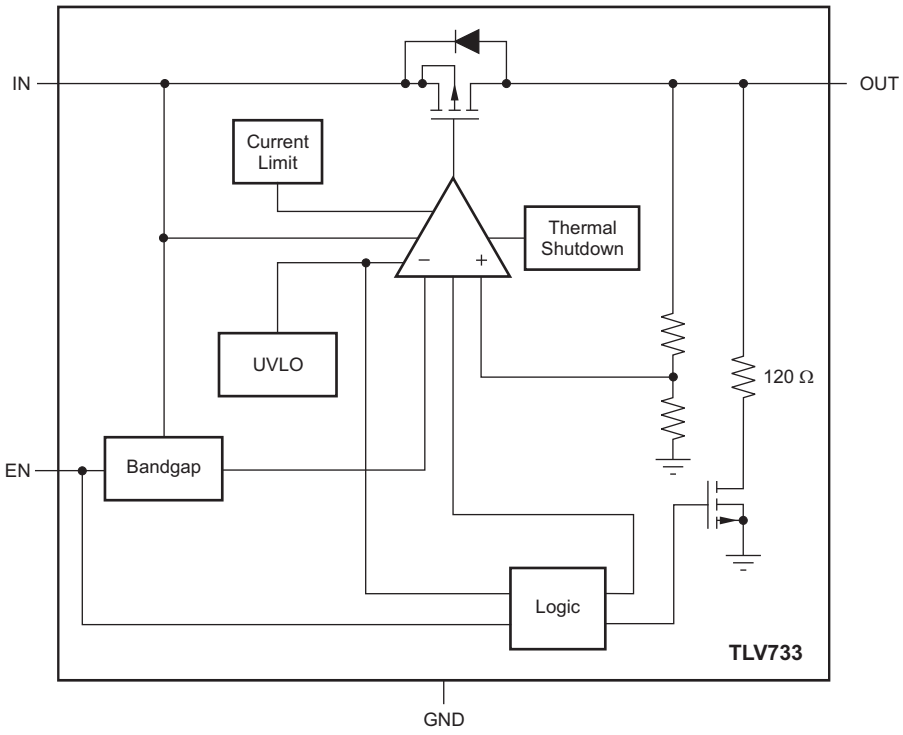
7 Detailed Description

7.1 Overview

The TLV733 belongs to a new family of next-generation, low-dropout regulators (LDOs). These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise, good PSRR with low dropout voltage, make this family of devices ideal for portable consumer applications.

This family of regulators offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this family of devices is –40°C to 125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TLV733 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage, $UVLO_{RISE}$. This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. During UVLO disable, the output is connected to ground with a 120-Ω pulldown resistor.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(HI)}$ (0.9 V, minimum). Turn off the device by forcing the EN pin to drop below 0.35 V. If shutdown capability is not required, connect EN to IN.

The TLV733 has an internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. The time constant is calculated in Equation 1:

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

7.3.3 Internal Foldback Current Limit

The TLV733 has an internal foldback current limit that protects the regulator during fault conditions. The current allowed through the device is reduced as the output voltage falls. When the output is shorted, the LDO supplies a typical current of 150 mA. The output voltage is not regulated when the device is in current limit. In this condition, the output voltage is the product of the regulated current and the load resistance. When the device output is shorted, the PMOS pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{OS}] until thermal shutdown is triggered and the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* table for more details.

The foldback current-limit circuit limits the current allowed through the device to current levels lower than the minimum current limit at nominal V_{OUT} current limit (I_{LIM}) during startup. See Figure 18 to Figure 20 for typical foldback current limit values. If the output is loaded by a constant-current load during startup, or if the output voltage is negative when the device is enabled, then the load current demanded by the load may exceed the foldback current limit and the device may not rise to the full output voltage. For constant-current loads, disable the output load until the TLV733 has fully risen to its nominal output voltage.

The TLV733 PMOS pass element has an intrinsic body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. Do not force the output voltage to exceed the input voltage because excessively high current may flow through the body diode.

7.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 160°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting it from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} –V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TLV733 internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the TLV733 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO rising voltage and has not decreased below the UVLO falling threshold.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the thermal shutdown temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout may result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO falling voltage, or has not yet exceeded the UVLO rising threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

When the device is disabled, the active pulldown resistor discharges the output.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT}nom + V_{DO}$ and $V_{IN} > UVLO_{RISE}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 160°C$
Dropout mode	$UVLO_{RISE} < V_{IN} < V_{OUT}nom + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 160°C$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{FALL}$	$V_{EN} < V_{EN(LO)}$	—	$T_J > 160°C$

8 Application and Implementation

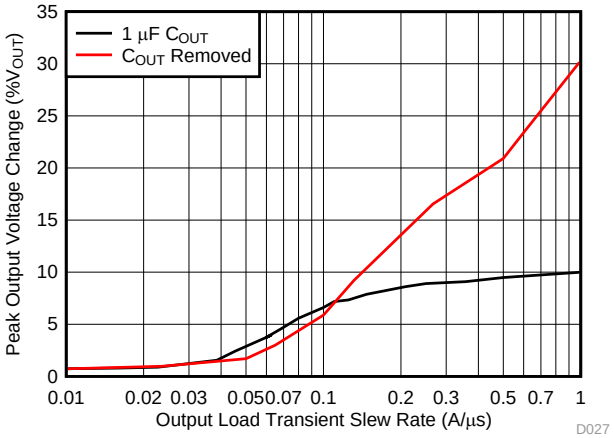
8.1 Application Information

8.1.1 Input and Output Capacitor Selection

The TLV733 uses an advanced internal control loop to obtain stable operation both with and without the use of input or output capacitors. Dynamic performance is improved with the use of an output capacitor, and may be improved with an input capacitor. An output capacitance of 0.1 µF or larger generally provides good dynamic response. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

Although an input capacitor is not required for stability, increased output impedance from the input supply may compromise the performance of the TLV733. Good analog design practice is to connect a 0.1-µF to 1-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is greater than 0.5 Ω. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

Figure 33 shows the transient performance improvements with an external 1-µF capacitor on the output versus no output capacitor. The data in this figure are taken with an increasing load step from 50 mA to 300 mA, and the peak output voltage deviation (load transient response) is measured. For low output current slew rates, (< 0.1 A/µs), the transient performance of the device is similar with or without an output capacitor. As the current slew rate is increased, the peak voltage deviation is significantly increased. For loads that exhibit fast current slew rates above 0.1 A/µs, use an output capacitor. For best performance, the maximum recommended output capacitance is 100 µF.



TLV73333PDBV, output current stepped from 50 mA to 300 mA, output voltage change measured at positive dI/dt

Figure 33. Output Voltage Deviation vs Load Step Slew Rate

Some applications benefit from the removal of the output capacitor. In addition to space and cost savings, the removal of the output capacitor lowers inrush current as a result of eliminating the required current flow into the output capacitor upon startup. In these cases, take care to ensure that the load is tolerant of the additional output voltage deviations.

Application Information (continued)

8.1.2 Dropout Voltage

The TLV733 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation. See Figure 7 to Figure 12 for typical dropout values.

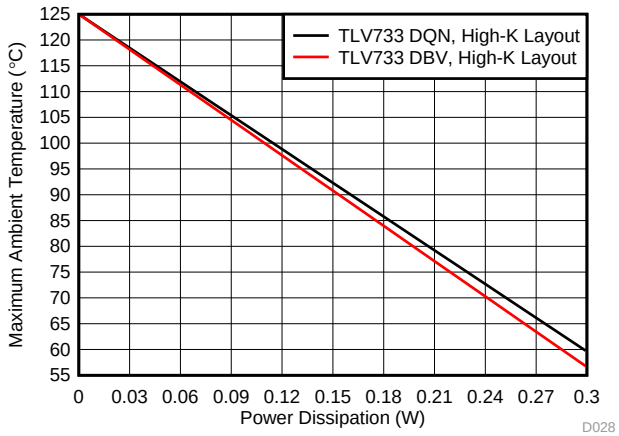
8.1.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation (P_D) depends on input voltage and load conditions. P_D is equal to the product of the output current and voltage drop across the output pass element, as shown in Equation 2.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Figure 34 shows the maximum ambient temperature versus the power dissipation of the TLV733 in the DQN package. This figure assumes the device is soldered on JEDEC standard high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to make sure the TLV733 does not operate continuously above a junction temperature of 125°C.



TLV733, high-K layout

Figure 34. Maximum Ambient Temperature vs Device Power Dissipation

8.2 Typical Applications

8.2.1 DC-DC Converter Post Regulation

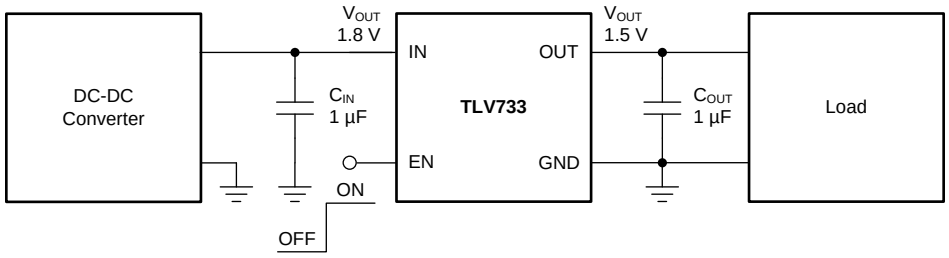


Figure 35. DC-DC Converter Post Regulation

8.2.1.1 Design Requirements

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.8 V, ±5%
Output voltage	1.5 V, ±1%
Output current	200-mA dc, 300-mA peak
Output voltage transient deviation	< 10%, 1-A/µs load step from 50 mA to 200 mA
Maximum ambient temperature	85°C

8.2.1.2 Design Considerations

Input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 1 µF are selected to give the maximum output capacitance in a small, low-cost package.

Figure 7 shows the 1.2-V option dropout voltage. Given that dropout voltages are higher for lower output-voltage options, and given that the 1.2-V option dropout voltage is typically less than 300 mV at 125°C, then the 1.5-V option dropout voltage is typically less than 300 mV at 125°C.

Verify that the maximum junction temperature is not exceeded by referring to Figure 34.

8.2.1.3 Application Curve

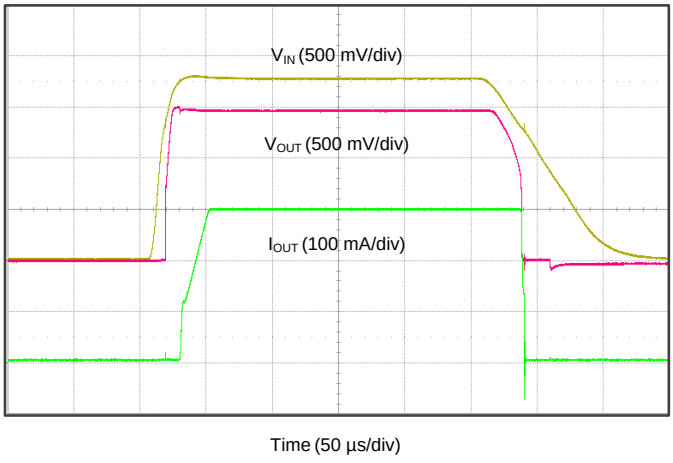


Figure 36. 1.8-V to 1.5-V Regulation at 300 mA

8.2.2 Capacitor-Free Operation from Battery Input Supply

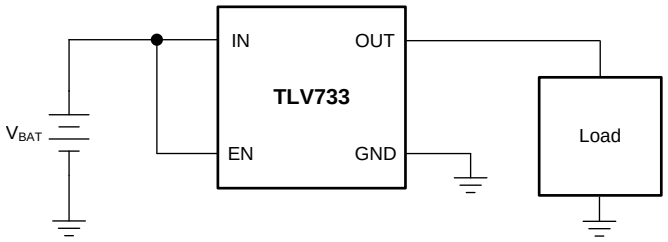


Figure 37. Capacitor-Free Operation from Battery Input Supply

8.2.2.1 Design Requirements

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.0 V to 1.8 V (two 1.5-V batteries)
Output voltage	1.0 V, ±1%
Input current	200 mA, maximum
Output load	100-mA dc
Maximum ambient temperature	70°C

8.2.2.2 Design Considerations

An input capacitor is not required for this design because of the low impedance connection directly to the battery.

No output capacitor allows for the minimal possible inrush current during startup, ensuring the 200-mA maximum input current is not exceeded.

Verify that the maximum junction temperature is not exceeded by referring to Figure 34.

8.2.2.3 Application Curve

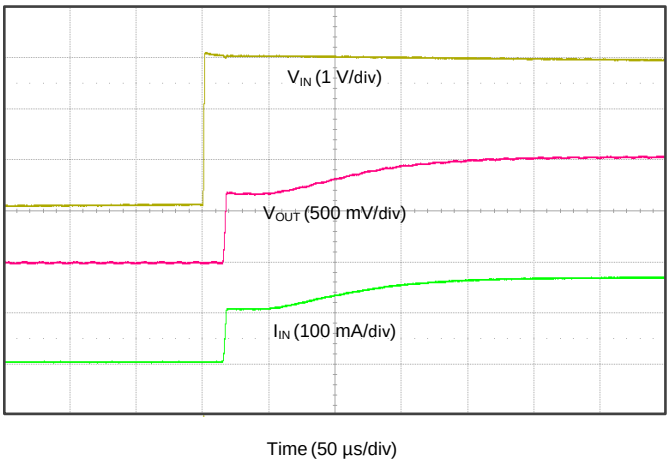


Figure 38. No Inrush Startup, 3.0-V to 1.0-V Regulation

9 Power-Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TLV733. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during startup or load transient events. If inductive impedances are unavoidable, use an input capacitor.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections, in order to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DQN package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

10.2 Layout Examples

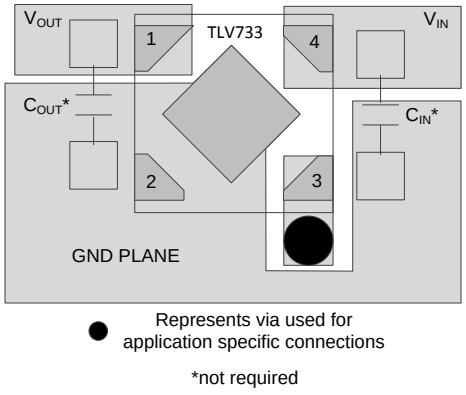


Figure 39. Layout Example for the DQN package

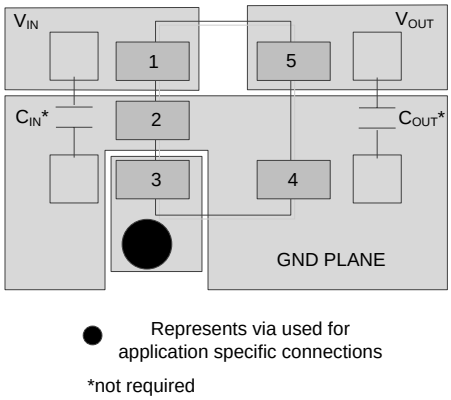


Figure 40. Layout Example for the DBV Package

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV733. The TLV73312PEVM-643 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.2 Device Nomenclature

Table 4. Device Nomenclature(1)(2)

PRODUCT	V_{OUT}
TLV733**xx(x)Pyyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **P** indicates an active output discharge feature. All members of the TLV733 family will actively discharge the output when the device is disabled. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.0 V to 3.3 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

TLV73312PDQN-643 Evaluation Module User Guide, SBVU024

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV73310PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VCCQ	Samples
TLV73310PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VCCQ	Samples
TLV73310PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	FG	Samples
TLV73310PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	FG	Samples
TLV73311PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBLW	Samples
TLV73311PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBLW	Samples
TLV73311PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	GR	Samples
TLV73311PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	GR	Samples
TLV73312PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VCDQ	Samples
TLV73312PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VCDQ	Samples
TLV73312PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	FI	Samples
TLV73312PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	FI	Samples
TLV73315PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VCFQ	Samples
TLV73315PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VCFQ	Samples
TLV73315PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	FJ	Samples
TLV73315PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	FJ	Samples
TLV73318PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VCGQ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV73318PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VCGQ	Samples
TLV73318PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	FK	Samples
TLV73318PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	FK	Samples
TLV733255PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		
TLV733255PDQNT	PREVIEW	X2SON	DQN	4	250	TBD	Call TI	Call TI	-40 to 125		
TLV73325PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VCHQ	Samples
TLV73325PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VCHQ	Samples
TLV73325PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	FL	Samples
TLV73325PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	FL	Samples
TLV733285PDBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TLV733285PDBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 125		
TLV733285PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		
TLV733285PDQNT	PREVIEW	X2SON	DQN	4	250	TBD	Call TI	Call TI	-40 to 125		
TLV73328PDBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TLV73328PDBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 125		
TLV73328PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		
TLV73328PDQNT	PREVIEW	X2SON	DQN	4	250	TBD	Call TI	Call TI	-40 to 125		
TLV73330PDBVR	PREVIEW	SOT-23	DBV	4	3000	TBD	Call TI	Call TI	-40 to 125		
TLV73330PDBVT	PREVIEW	SOT-23	DBV	4	250	TBD	Call TI	Call TI	-40 to 125		
TLV73330PDQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		
TLV73330PDQNT	PREVIEW	X2SON	DQN	4	250	TBD	Call TI	Call TI	-40 to 125		
TLV73333PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VCIQ	Samples
TLV73333PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VCIQ	Samples
TLV73333PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	FM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV73333PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	FM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

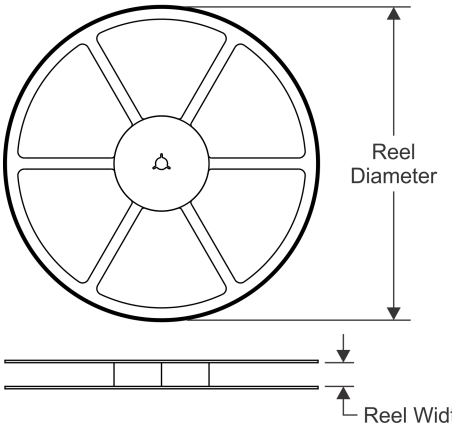
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

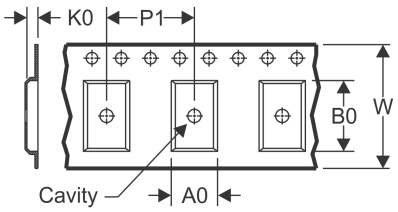
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

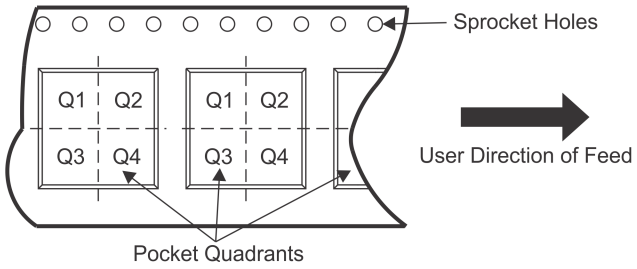


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

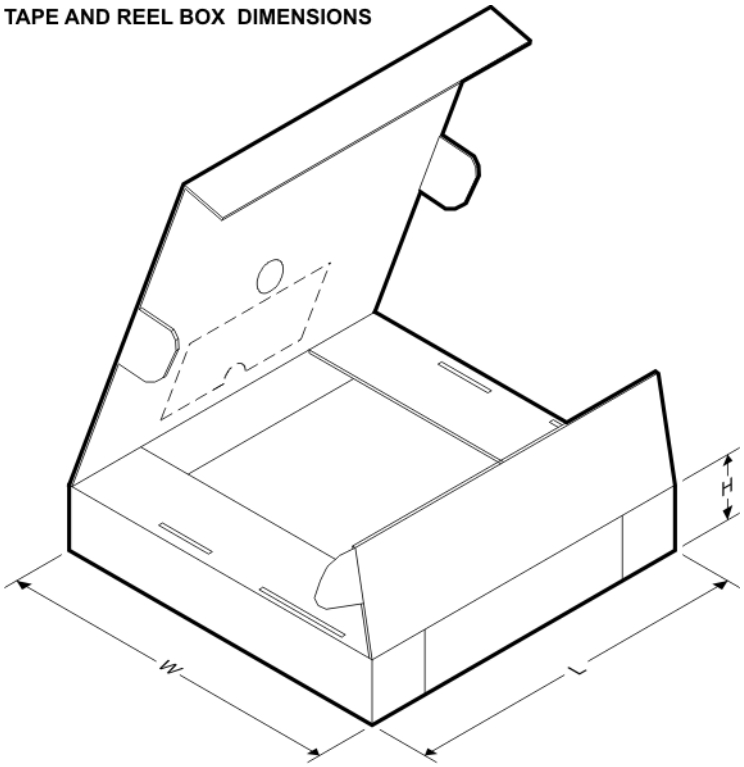


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV73310PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV73310PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV73310PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV73310PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV73311PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV73311PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV73311PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV73311PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV73312PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV73312PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV73312PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV73312PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV73315PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV73315PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV73315PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV73315PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV73318PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV73318PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV73318PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV73318PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV73325PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV73325PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV73325PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV73325PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV73333PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV73333PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV73333PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV73333PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

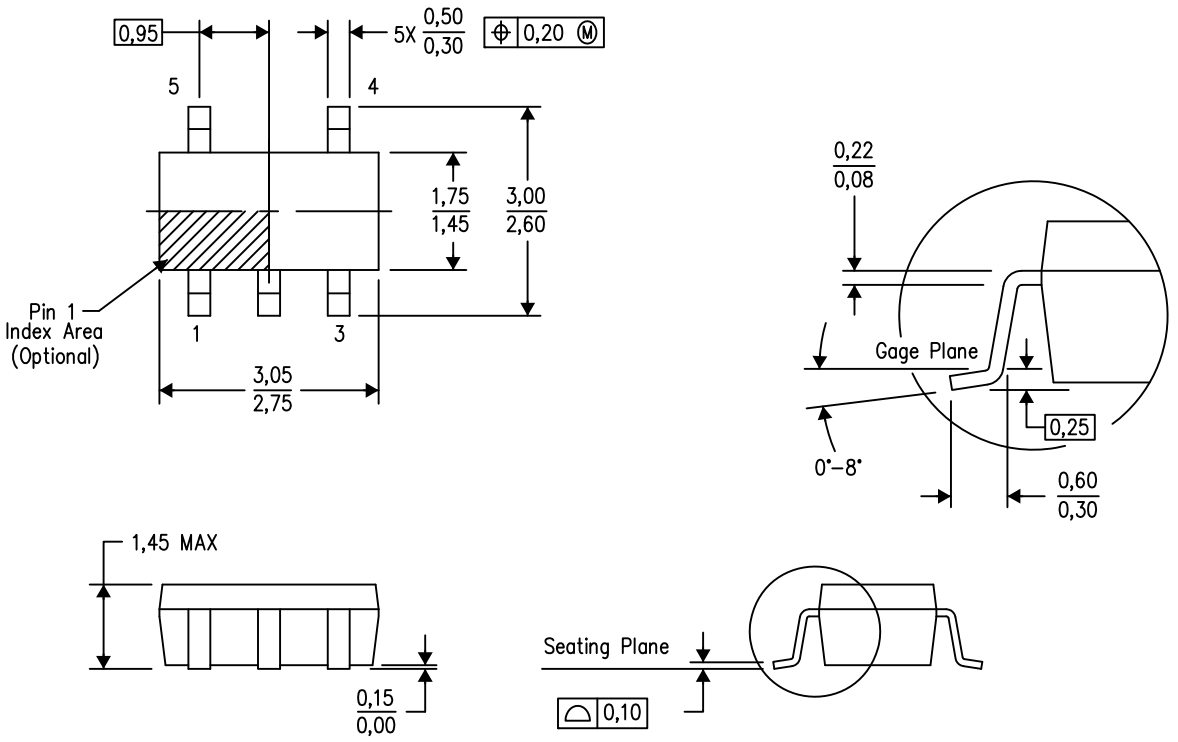


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV73310PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV73310PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV73310PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV73310PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV73311PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV73311PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV73311PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV73311PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV73312PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV73312PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV73312PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV73312PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV73315PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV73315PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV73315PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV73315PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV73318PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV73318PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV73318PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV73318PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV73325PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV73325PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV73325PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV73325PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV73333PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV73333PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV73333PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV73333PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0

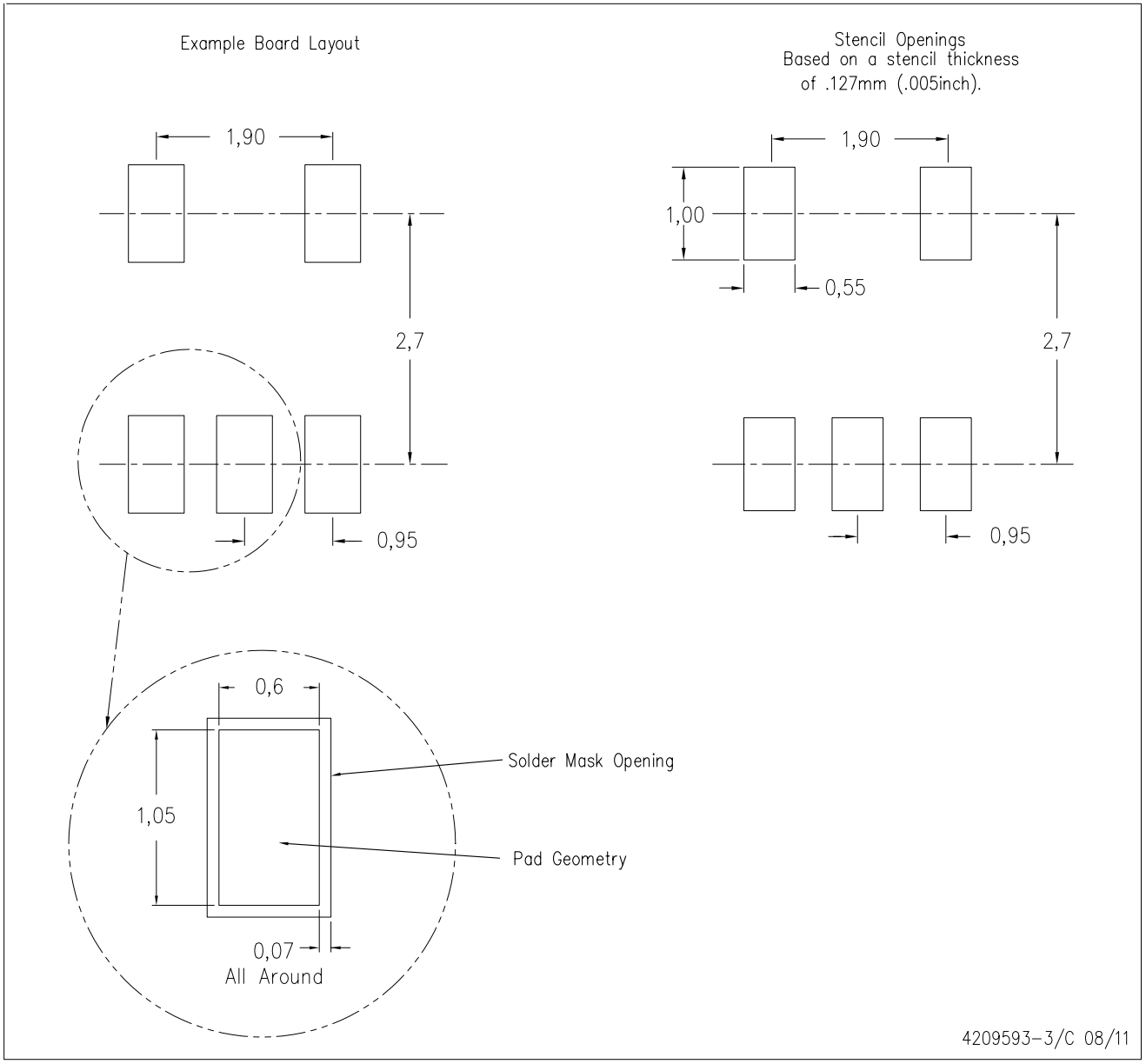
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

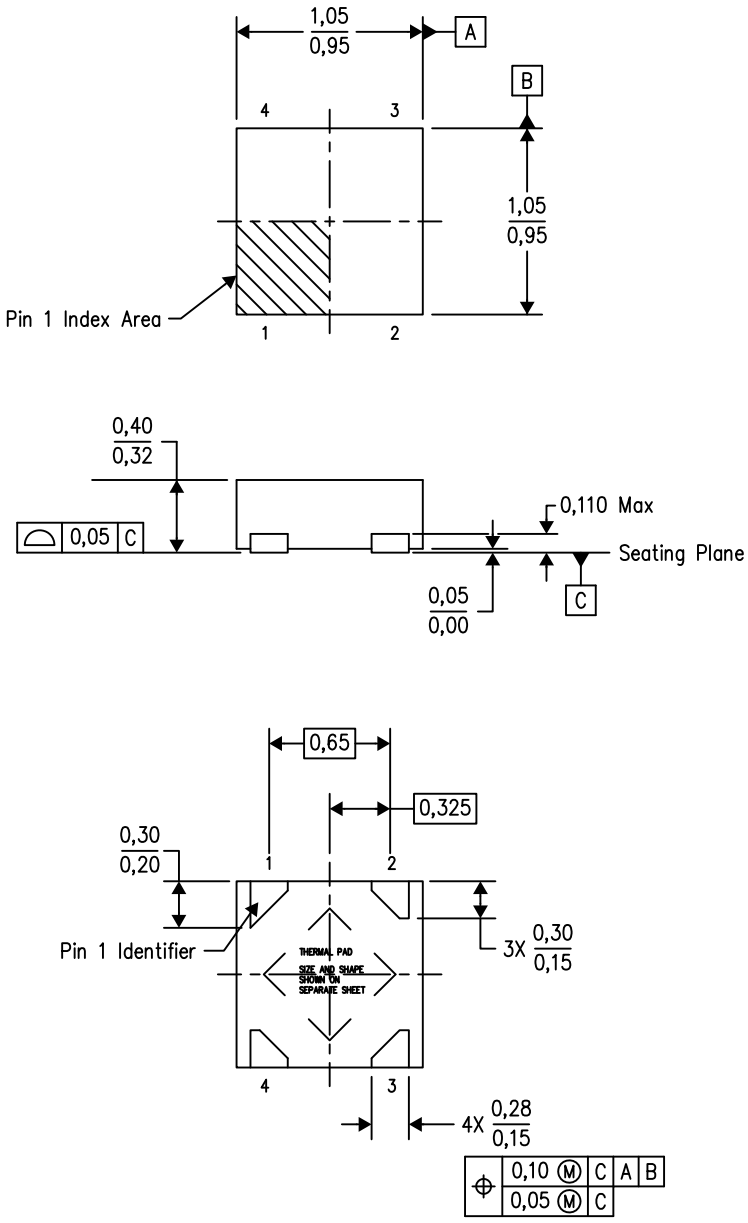
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



4210367/D 09/2012

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

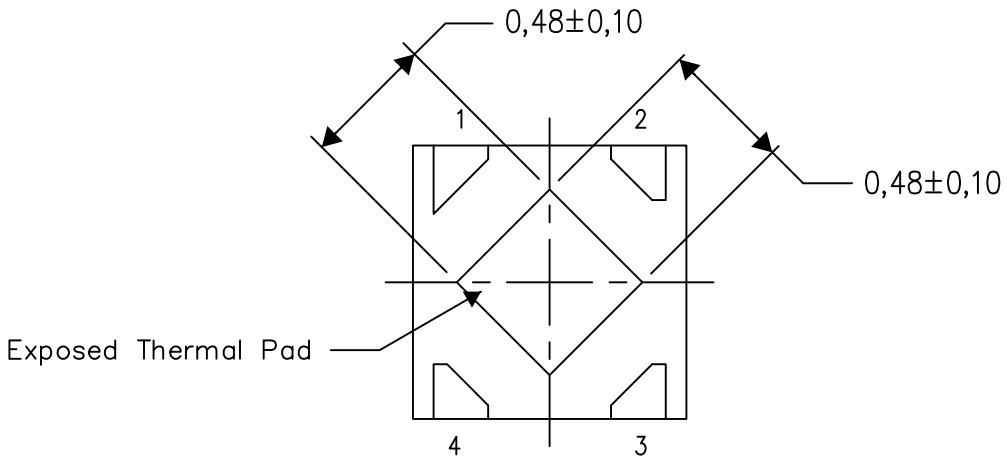
DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



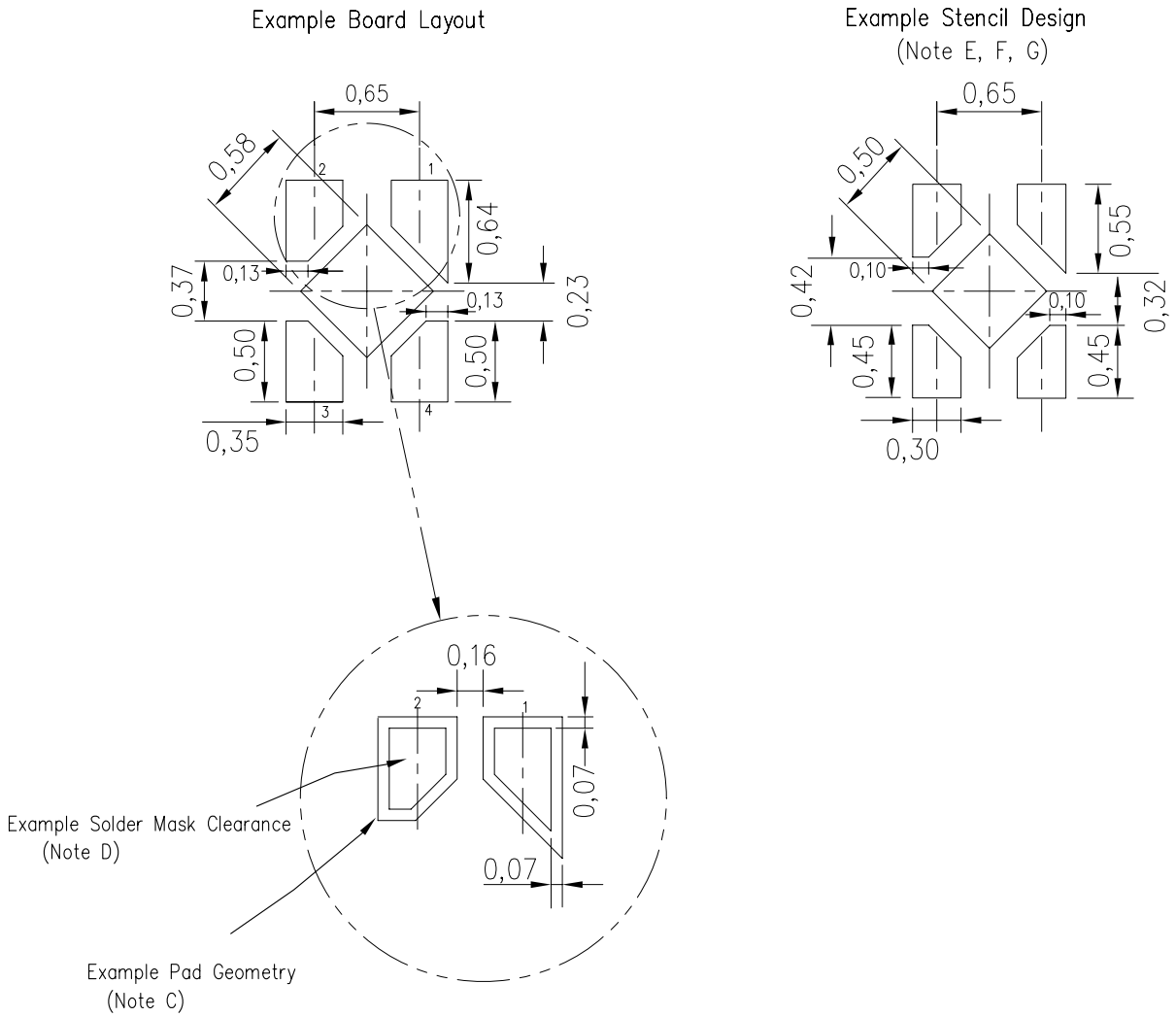
Bottom View

Exposed Thermal Pad Dimensions

4210393–3/E 04/12

NOTE: All linear dimensions are in millimeters

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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RFID	www.ti-rfid.com		
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