

Dual Positive-Edge-Triggered D-Type Flip-Flops With Clear and Preset

 Check for Samples: [SN54AHC74](#), [SN74AHC74](#)

FEATURES

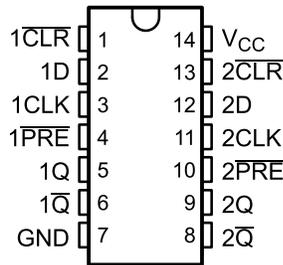
- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION

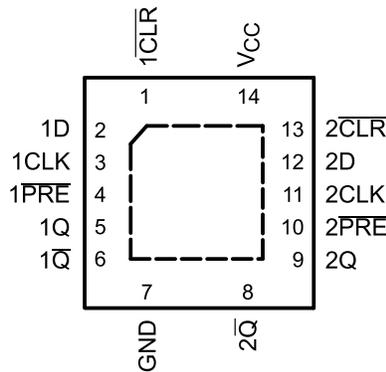
The 'AHC74 dual positive-edge-triggered devices are D-type flip-flops.

A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

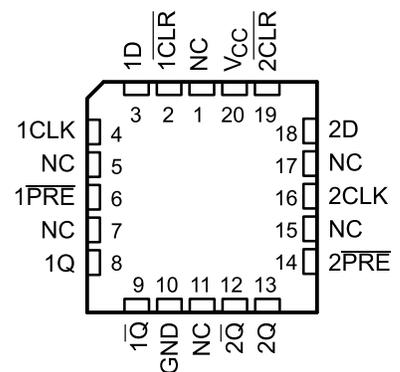
SN54AHC74 . . . J OR W PACKAGE
SN74AHC74 . . . D, DB, DGV, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74AHC74 . . . RGY PACKAGE
(TOP VIEW)



SN54AHC74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

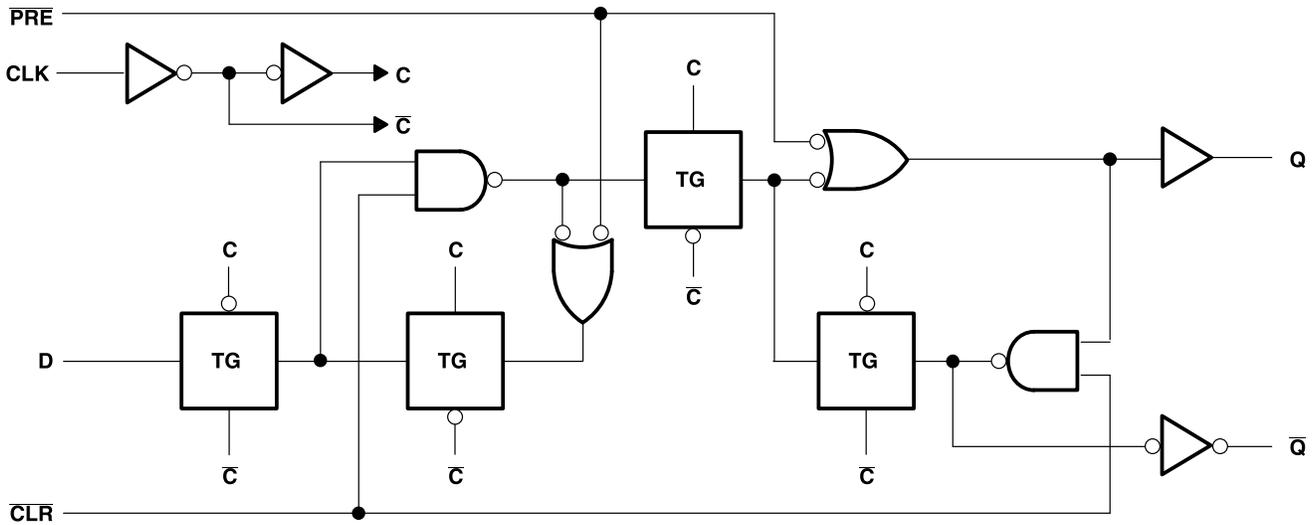


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. Function Table (Each Flip-Flop)

INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H ⁽¹⁾	H ⁽¹⁾
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	$\overline{\text{Q}}_0$

(1) This configuration is unstable; that is, it does not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.



Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		UNIT
Supply voltage range, V_{CC}		–0.5 V to 7 V
Input voltage range, V_I ⁽²⁾		–0.5 V to 7 V
Output voltage range, V_O ⁽²⁾		–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)		–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)		±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		±25 mA
Continuous current through V_{CC} or GND		±50 mA
Package thermal impedance, Θ_{JA}	D package	86°C/W
	DB package ⁽³⁾	96°C/W
	DGV package ⁽³⁾	127°C/W
	N package ⁽³⁾	80°C/W
	NS package ⁽³⁾	76°C/W
	PW package ⁽³⁾	113°C/W
	RGY package ⁽⁴⁾	47°C/W
Storage temperature range, T_{stg}		–65°C to 150°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions⁽¹⁾

		SN54AHC74		SN74AHC74		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5	1.5		V
		$V_{CC} = 3$ V	2.1	2.1		
		$V_{CC} = 5.5$ V	3.85	3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5	0.5	V
		$V_{CC} = 3$ V		0.9	0.9	
		$V_{CC} = 5.5$ V		1.65	1.65	
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		–50	–50	μA
		$V_{CC} = 3.3$ V ± 0.3 V		–4	–4	mA
		$V_{CC} = 5$ V ± 0.5 V		–8	–8	
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50	50	μA
		$V_{CC} = 3.3$ V ± 0.3 V		4	4	mA
		$V_{CC} = 5$ V ± 0.5 V		8	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V		100	100	ns/V
		$V_{CC} = 5$ V ± 0.5 V		20	20	
T_A	Operating free-air temperature	–55	125	–40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			-55°C to 125°C SN54AHC74		-40°C to 85°C SN74AHC74		-40°C to 125°C SN74AHC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 mA	2 V	1.9	2		1.9		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58		2.48		2.48		2.48			
	I _{OH} = -8 mA	4.5 V	3.94		3.8		3.8		3.8			
V _{OL}	I _{OL} = 50 mA	2 V			0.1		0.1		0.1		V	
		3 V			0.1		0.1		0.1			
		4.5 V			0.1		0.1		0.1			
	I _{OL} = 4 mA	3 V		0.36		0.5		0.44		0.5		
	I _{OH} = 8 mA	4.5 V		0.36		0.5		0.44		0.5		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 ⁽¹⁾		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		20		20		20	μA
C _i	V _I = V _{CC} or GND	5 V		2	10				10			pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54AHC74		-40°C to 85°C SN74AHC74		-40°C to 125°C SN74AHC74		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	PRE or CLR low	6		7		7		7	ns
		CLK	6		7		7		7	
t _{su}	Setup time before CLK↑	Data	6		7		7		7	ns
		PRE or CLR inactive	5		5		5		5	
t _h	Hold time, data after CLK↑		0.5		0.5		0.5		0.5	ns

Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54AHC74		-40°C to 85°C SN74AHC74		-40°C to 125°C SN74AHC74		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	PRE or CLR low	5		5		5		5	ns
		CLK	5		5		5		5	
t _{su}	Setup time before CLK↑	Data	5		5		5		5	ns
		PRE or CLR inactive	3		3		3		3	
t _h	Hold time, data after CLK↑		0.5		0.5		0.5		0.5	ns

Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC74		–40°C to 85°C SN74AHC74		–40°C to 125°C SN74AHC74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	80 ⁽¹⁾	125 ⁽¹⁾		70 ⁽¹⁾		70		70	MHz	
			$C_L = 50\text{ pF}$	50	75		45		45		45		
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	$C_L = 15\text{ pF}$	7.6 ⁽¹⁾	12.3 ⁽¹⁾		1 ⁽¹⁾	14.5 ⁽¹⁾	1	14.5	1	14.5	ns
t_{PHL}				7.6	12.3		1 ⁽¹⁾	14.5 ⁽¹⁾	1	14.5	1	14.5	
t_{PLH}	CLK	Q or $\overline{\text{Q}}$	$C_L = 15\text{ pF}$	6.7	11.9		1 ⁽¹⁾	14 ⁽¹⁾	1	14	1	14	ns
t_{PHL}				6.7	11.9		1 ⁽¹⁾	14 ⁽¹⁾	1	14	1	14	
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	$C_L = 50\text{ pF}$	10.1	15.8		1	18	1	18	1	18	ns
t_{PHL}				10.1	15.8		1	18	1	18	1	18	
t_{PLH}	CLK	Q or $\overline{\text{Q}}$	$C_L = 50\text{ pF}$	9.2	15.4		1	17.5	1	17.5	1	17.5	ns
t_{PHL}				9.2	15.4		1	17.5	1	17.5	1	17.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC74		–40°C to 85°C SN74AHC74		–40°C to 125°C SN74AHC74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	130 ⁽¹⁾	170 ⁽¹⁾		110 ⁽¹⁾		110		110	MHz	
			$C_L = 50\text{ pF}$	90	115		75		75		75		
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	$C_L = 15\text{ pF}$	4.8 ⁽¹⁾	7.7 ⁽¹⁾		1 ⁽¹⁾	9 ⁽¹⁾	1	9	1	9	ns
t_{PHL}				4.8 ⁽¹⁾	7.7 ⁽¹⁾		1 ⁽¹⁾	9 ⁽¹⁾	1	9	1	9	
t_{PLH}	CLK	Q or $\overline{\text{Q}}$	$C_L = 15\text{ pF}$	4.6 ⁽¹⁾	7.3 ⁽¹⁾		1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5	1	8.5	ns
t_{PHL}				4.6 ⁽¹⁾	7.3 ⁽¹⁾		1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5	1	8.5	
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	$C_L = 50\text{ pF}$	6.3	9.7		1	11	1	11	1	11	ns
t_{PHL}				6.3	9.7		1	11	1	11	1	11	
t_{PLH}	CLK	Q or $\overline{\text{Q}}$	$C_L = 50\text{ pF}$	6.1	9.3		1	10.5	1	10.5	1	10.5	ns
t_{PHL}				6.1	9.3		1	10.5	1	10.5	1	10.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see ⁽¹⁾)

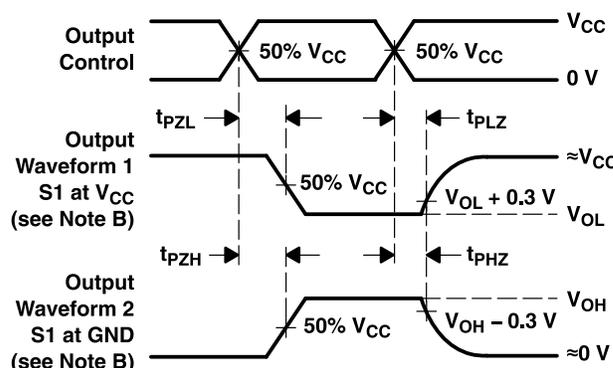
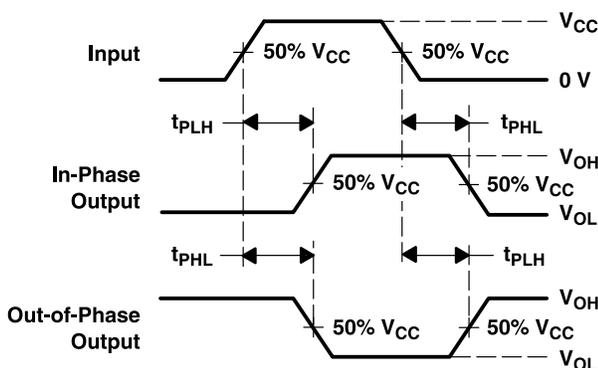
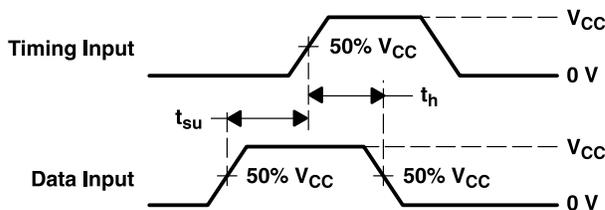
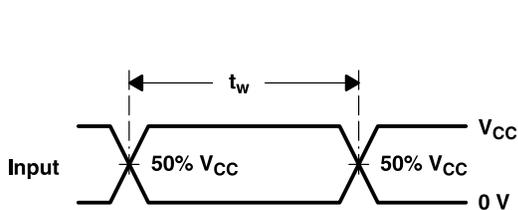
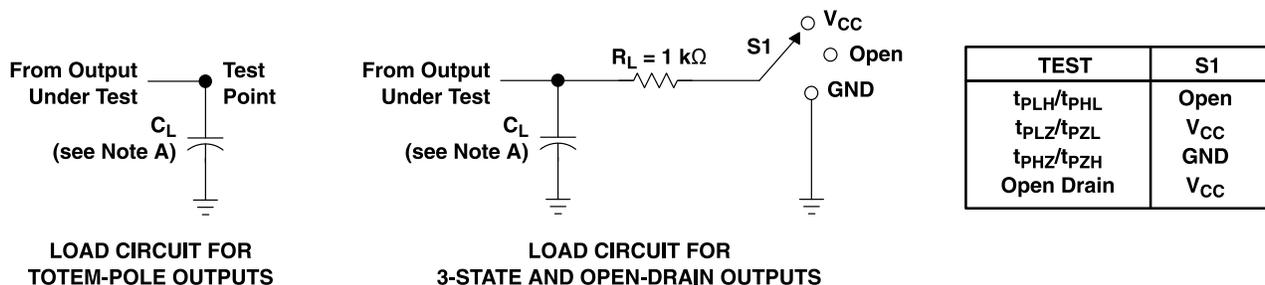
PARAMETER	DESCRIPTION	SN74AHC74		UNIT
		MIN	MAX	
$V_{\text{OL(P)}}$	Quiet output, maximum dynamic V_{OL}	0.8		V
$V_{\text{OL(V)}}$	Quiet output, minimum dynamic V_{OL}	–0.8		V
$V_{\text{OH(V)}}$	Quiet output, minimum dynamic V_{OH}	4.7		V
$V_{\text{IH(D)}}$	High-level dynamic input voltage	3.5		V
$V_{\text{IL(D)}}$	Low-level dynamic input voltage		1.5	V

(1) Characteristics are for surface-mount packages only.

Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance No load, $f = 1\text{ MHz}$	32	pF



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision J (September 2002) to Revision K	Page
• Updated document to new TI data sheet format.	1
• Added ESD warning.	2
• Removed Ordering Information table.	2
• Updated operating temperature range.	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9686001Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9686001Q2A SNJ54AHC 74FK	Samples
5962-9686001QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9686001QC A SNJ54AHC74J	Samples
5962-9686001QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9686001QD A SNJ54AHC74W	Samples
SN74AHC74D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC74	Samples
SN74AHC74DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	-40 to 125		
SN74AHC74DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA74	Samples
SN74AHC74DBRE4	ACTIVE	SSOP	DB	14		TBD	Call TI	Call TI	-40 to 125		Samples
SN74AHC74DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA74	Samples
SN74AHC74DE4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125		Samples
SN74AHC74DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC74	Samples
SN74AHC74DGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA74	Samples
SN74AHC74DGVRE4	ACTIVE	TVSOP	DGV	14		TBD	Call TI	Call TI	-40 to 125		Samples
SN74AHC74DGVRG4	ACTIVE	TVSOP	DGV	14		TBD	Call TI	Call TI	-40 to 125		Samples
SN74AHC74DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC74	Samples
SN74AHC74DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC74	Samples
SN74AHC74DRG4	ACTIVE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125		Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC74N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC74N	Samples
SN74AHC74NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC74N	Samples
SN74AHC74NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC74	Samples
SN74AHC74NSRE4	ACTIVE	SO	NS	14		TBD	Call TI	Call TI	-40 to 125		Samples
SN74AHC74NSRG4	ACTIVE	SO	NS	14		TBD	Call TI	Call TI	-40 to 125		Samples
SN74AHC74PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA74	Samples
SN74AHC74PWE4	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		Samples
SN74AHC74PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA74	Samples
SN74AHC74PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		
SN74AHC74PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA74	Samples
SN74AHC74PWRE4	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		Samples
SN74AHC74PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA74	Samples
SN74AHC74RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA74	Samples
SN74AHC74RGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA74	Samples
SNJ54AHC74FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9686001Q2A SNJ54AHC 74FK	Samples
SNJ54AHC74J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9686001QC A SNJ54AHC74J	Samples
SNJ54AHC74W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9686001QD A SNJ54AHC74W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AHC74, SN74AHC74 :

● Catalog: [SN74AHC74](#)

● Enhanced Product: [SN74AHC74-EP](#), [SN74AHC74-EP](#)

- Military: [SN54AHC74](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

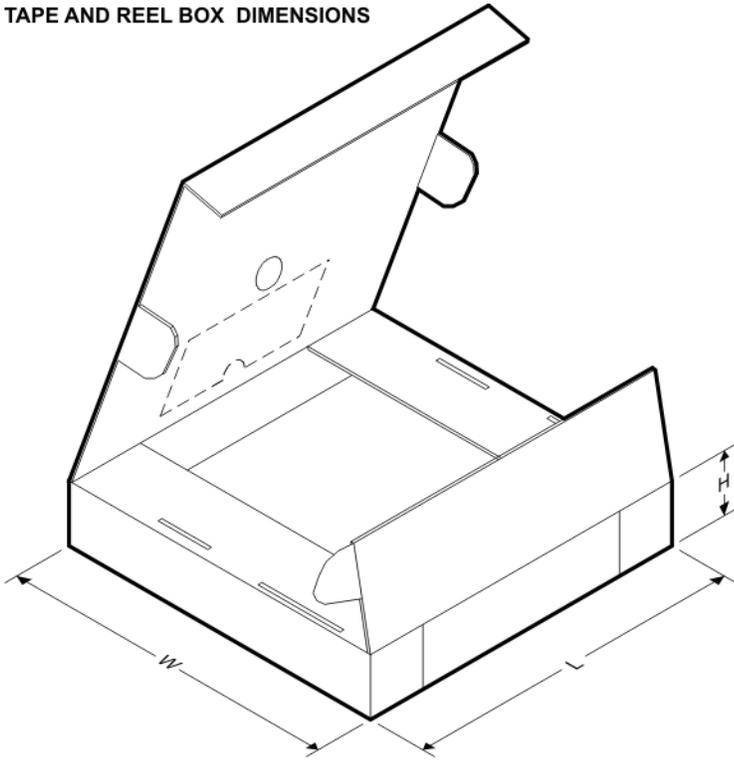
TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC74DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AHC74DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC74PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC74RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



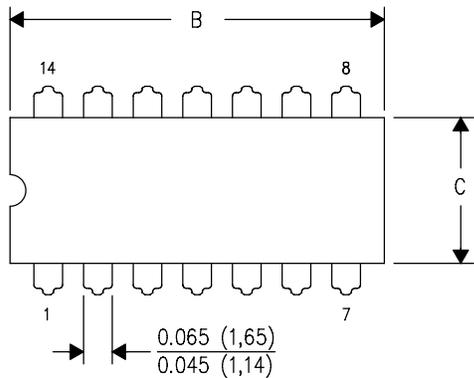
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC74DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74AHC74DGVR	TVSOP	DGV	14	2000	367.0	367.0	35.0
SN74AHC74DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74AHC74PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74AHC74RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

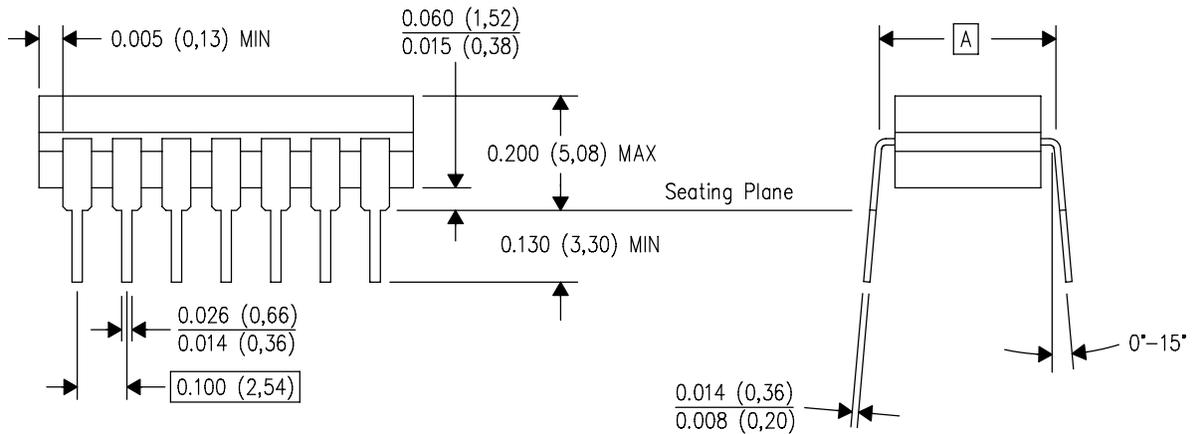
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

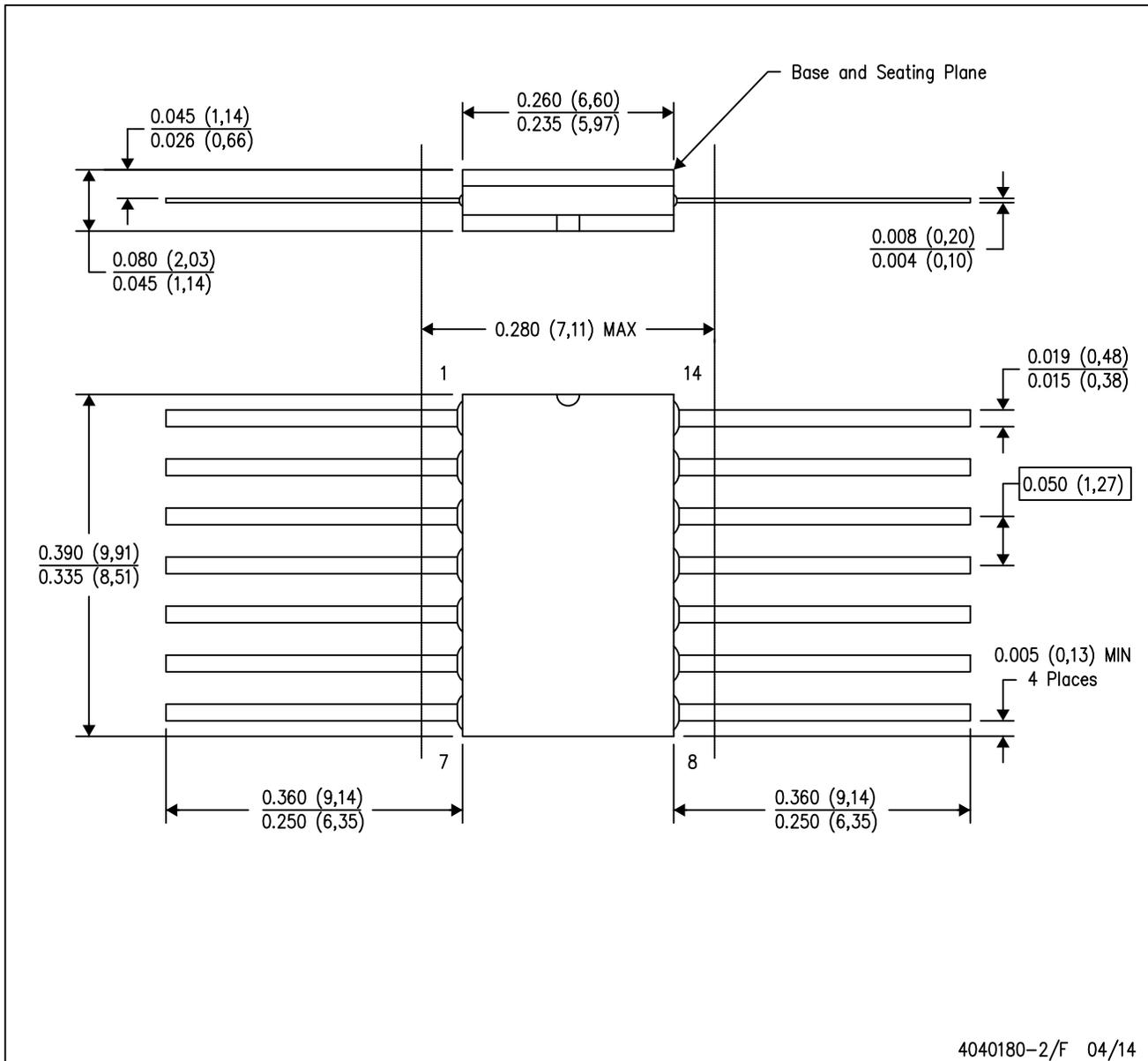


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

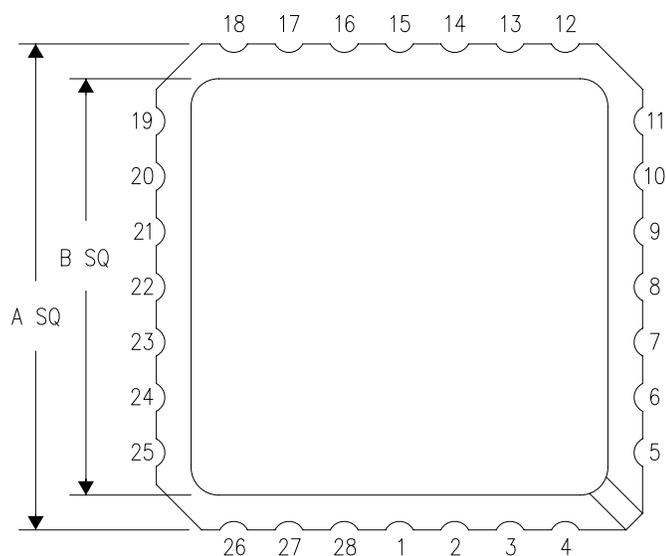


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

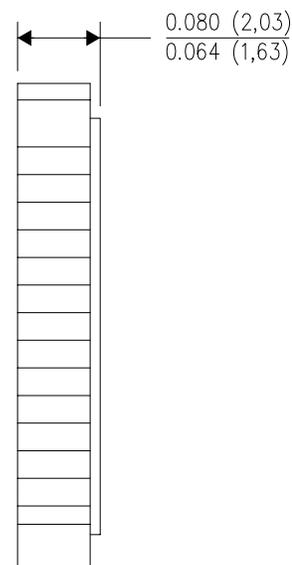
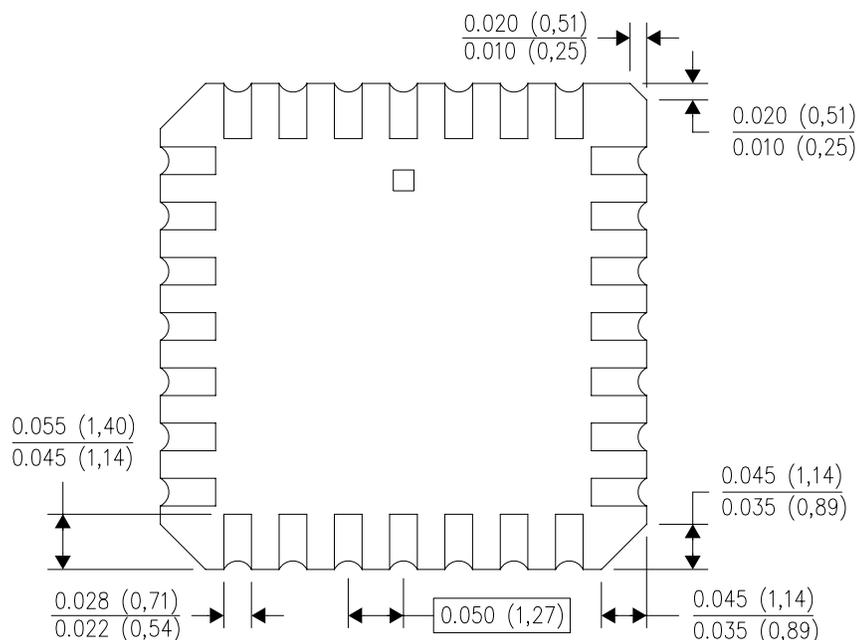
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



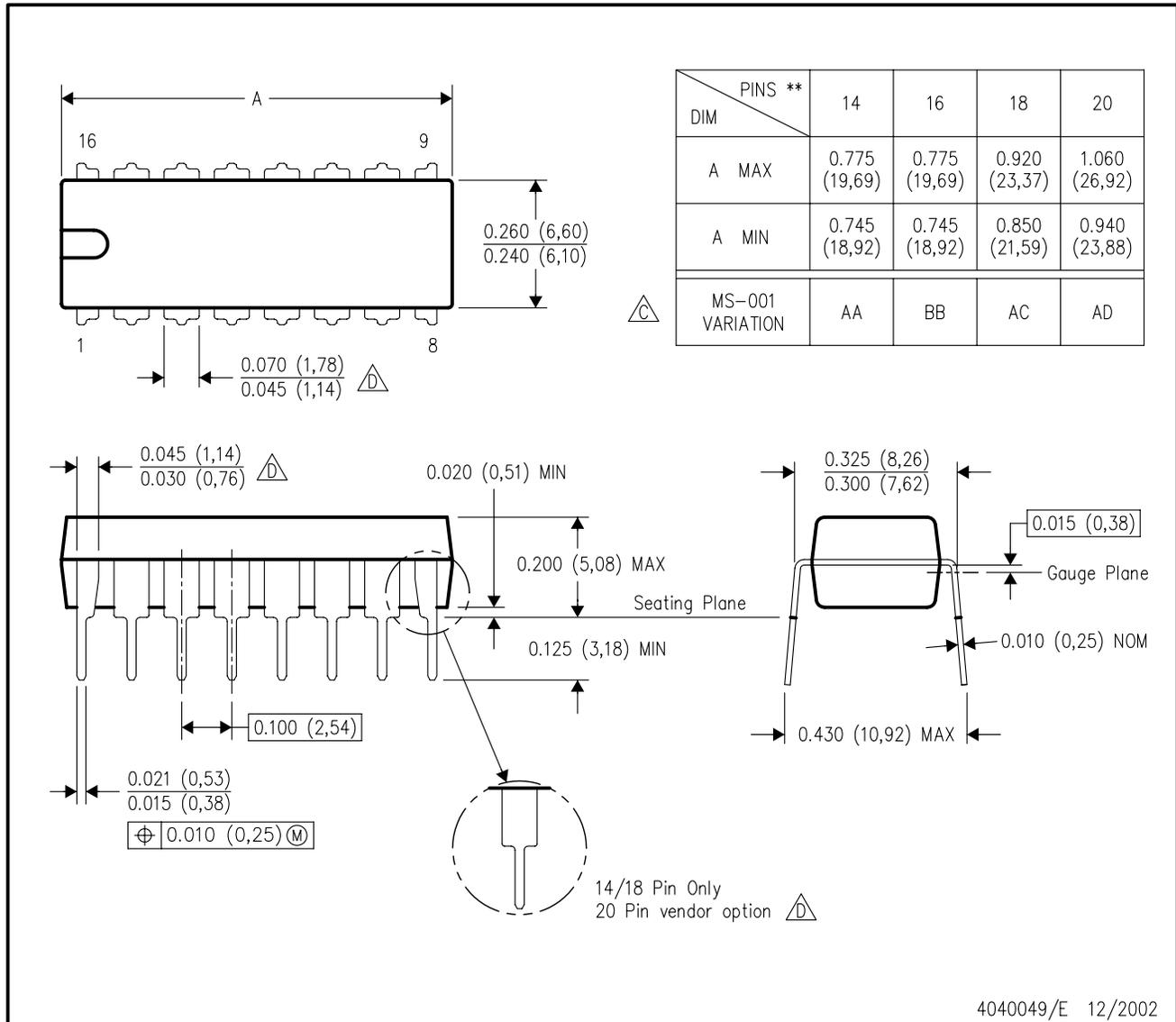
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

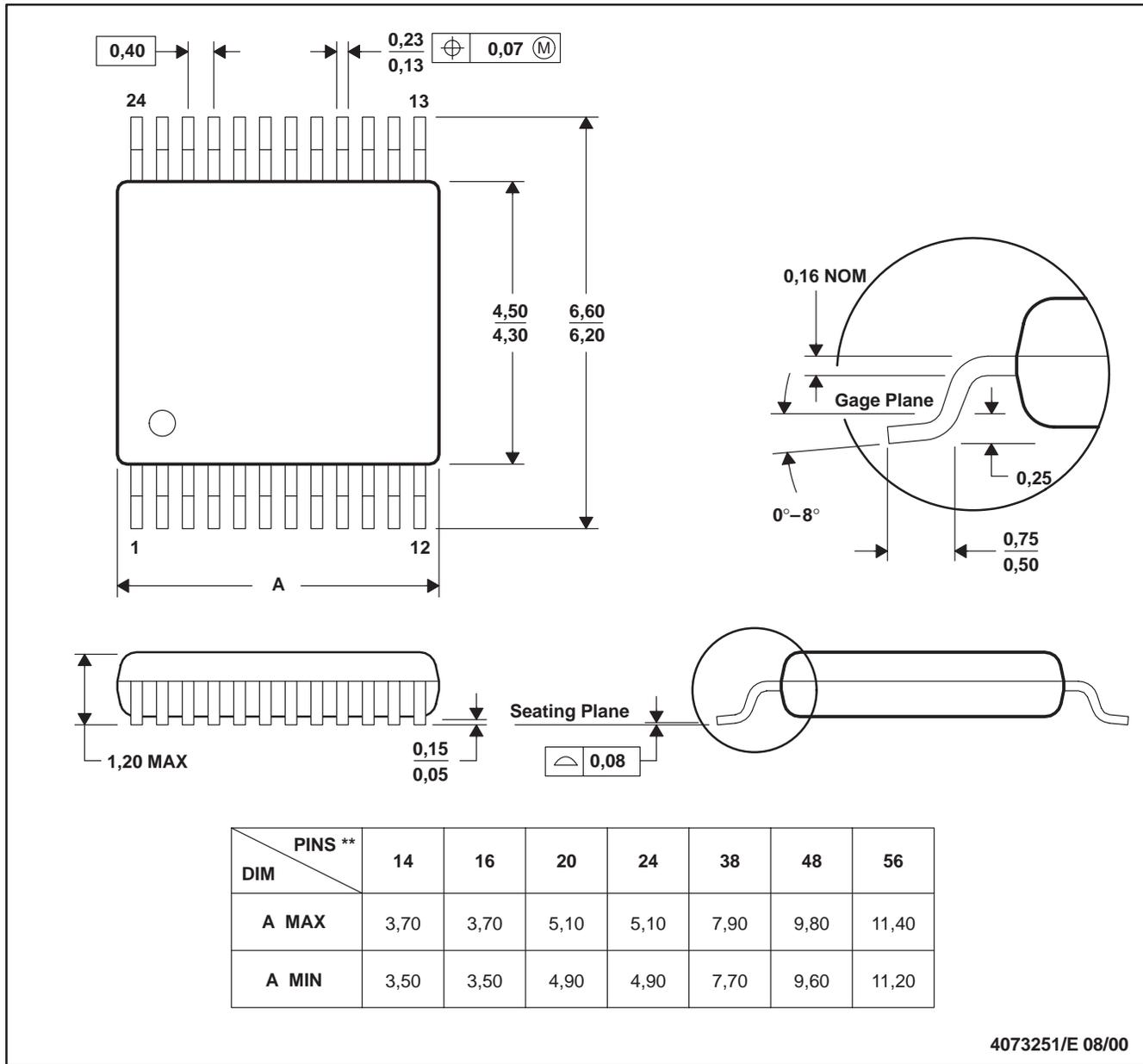


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

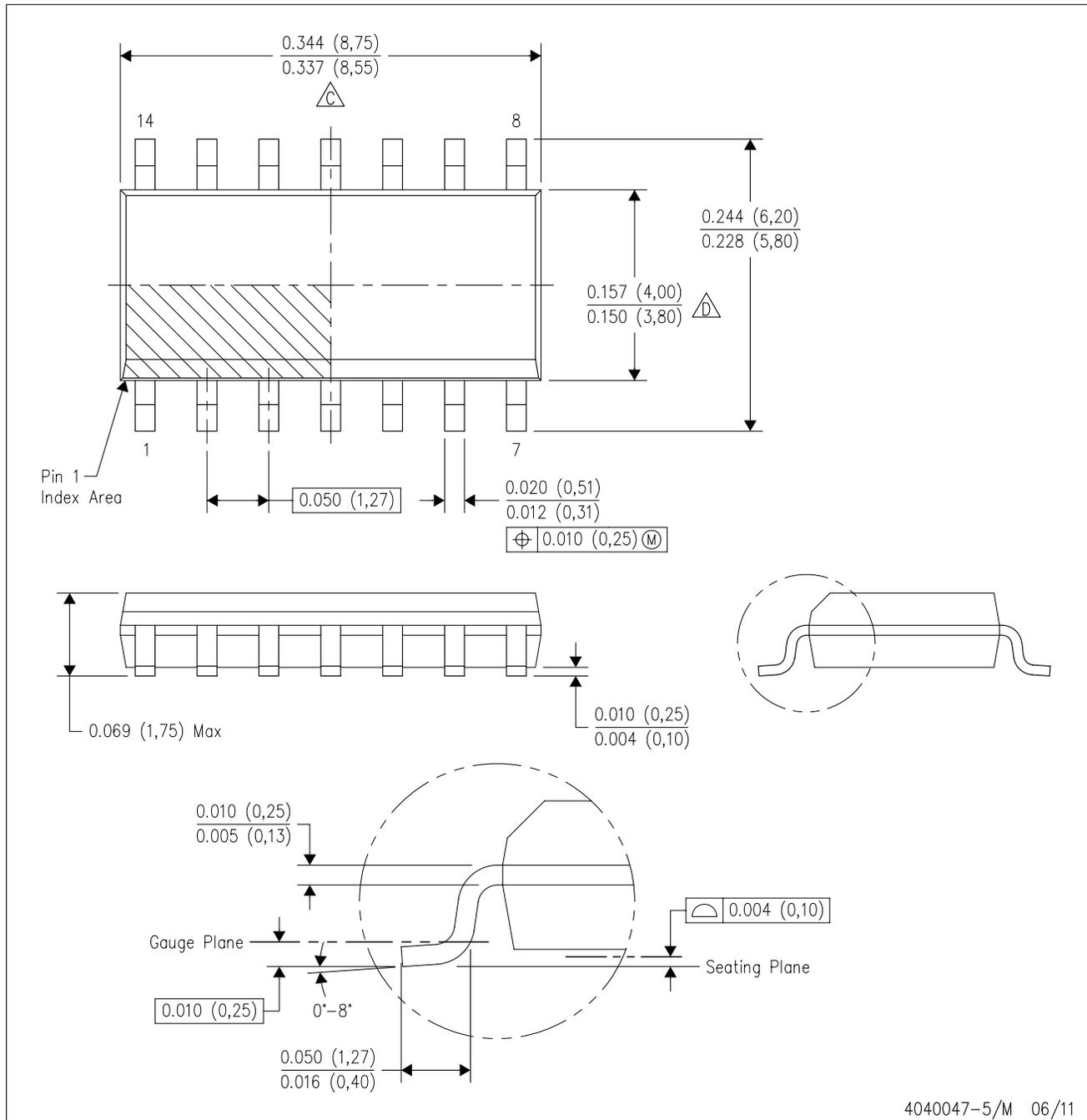
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

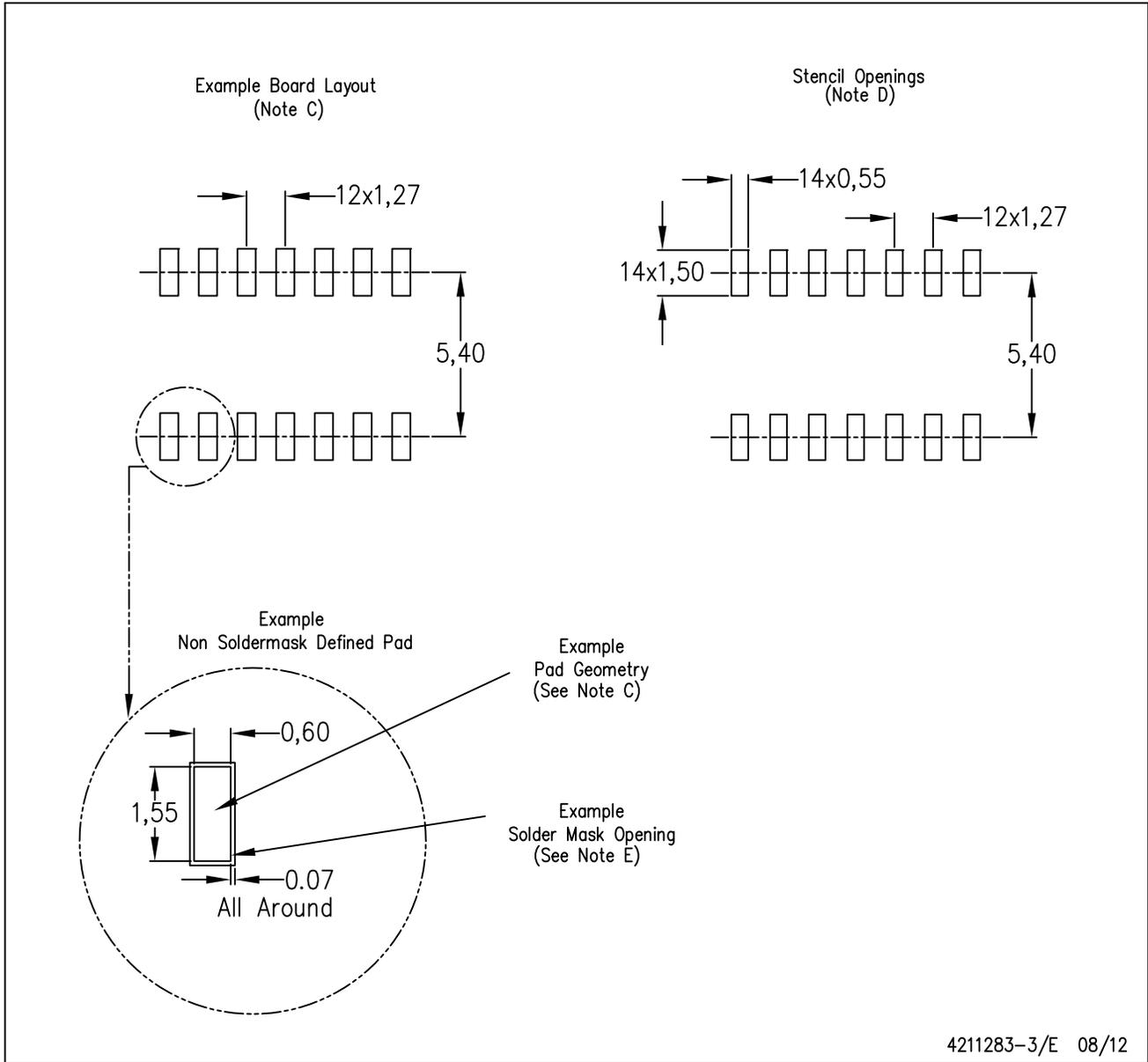
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

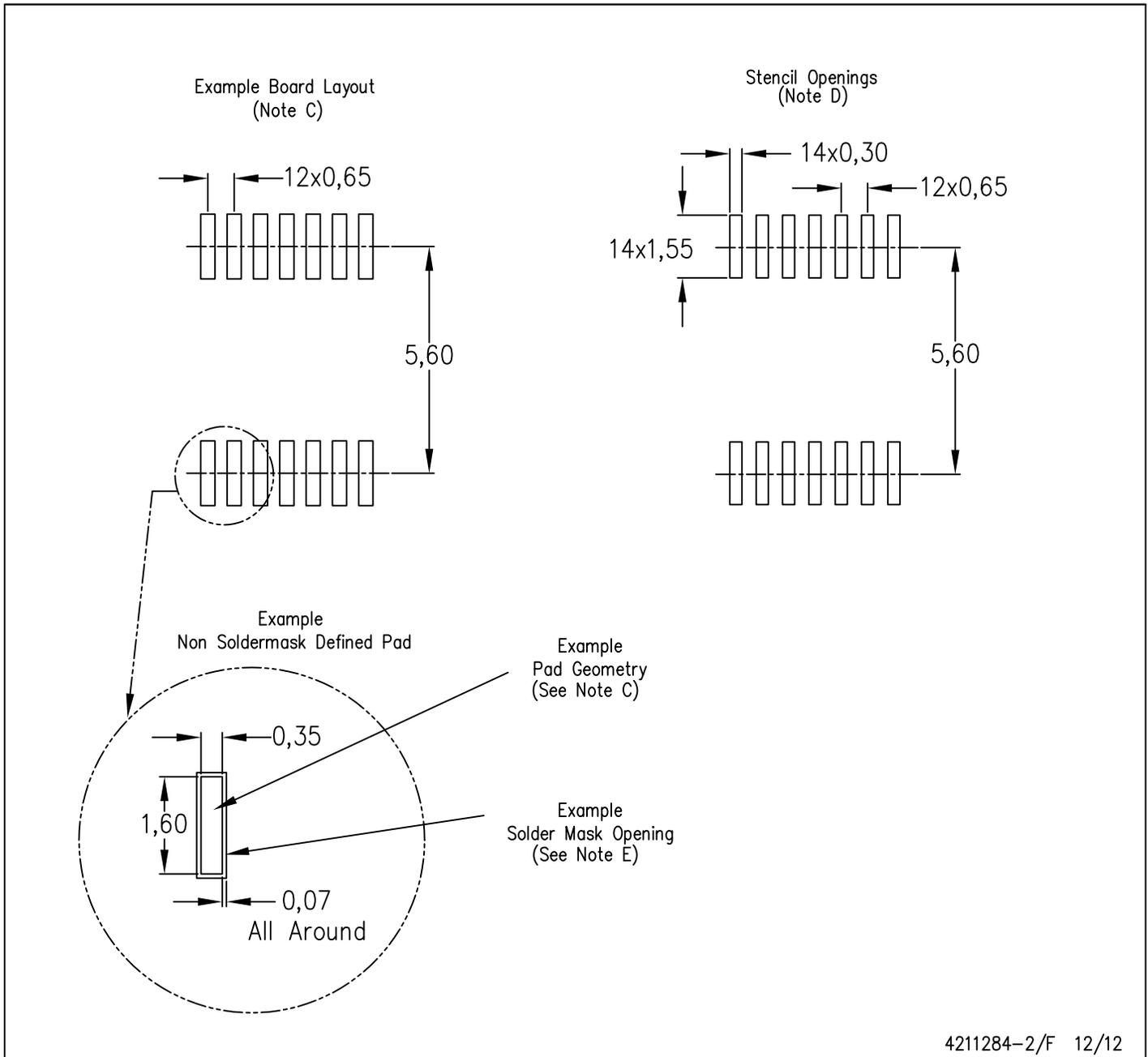
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

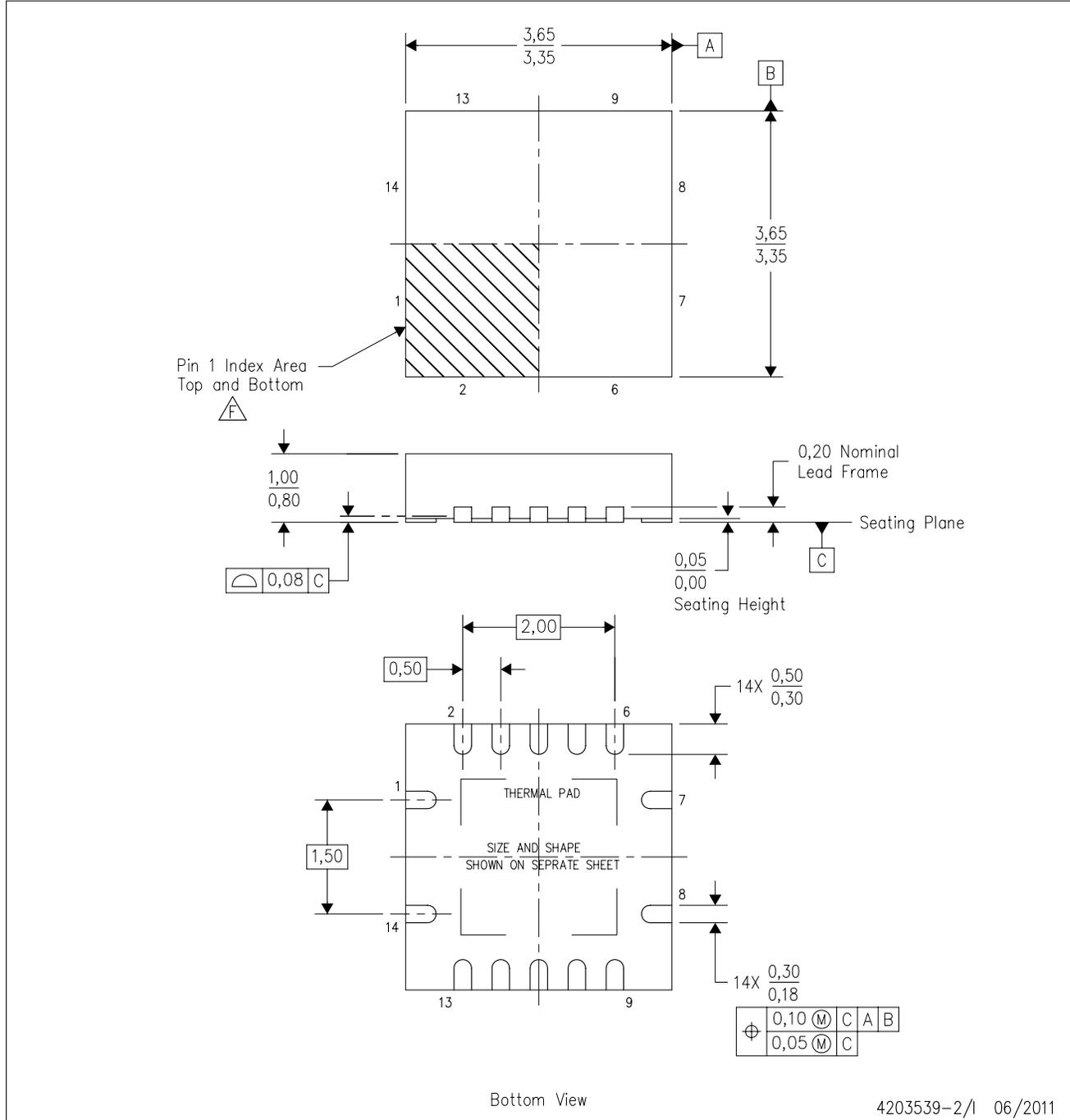
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

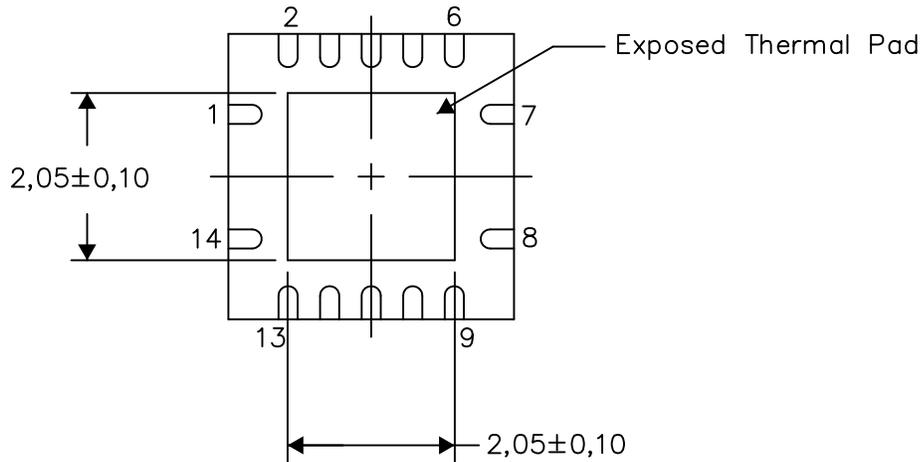
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

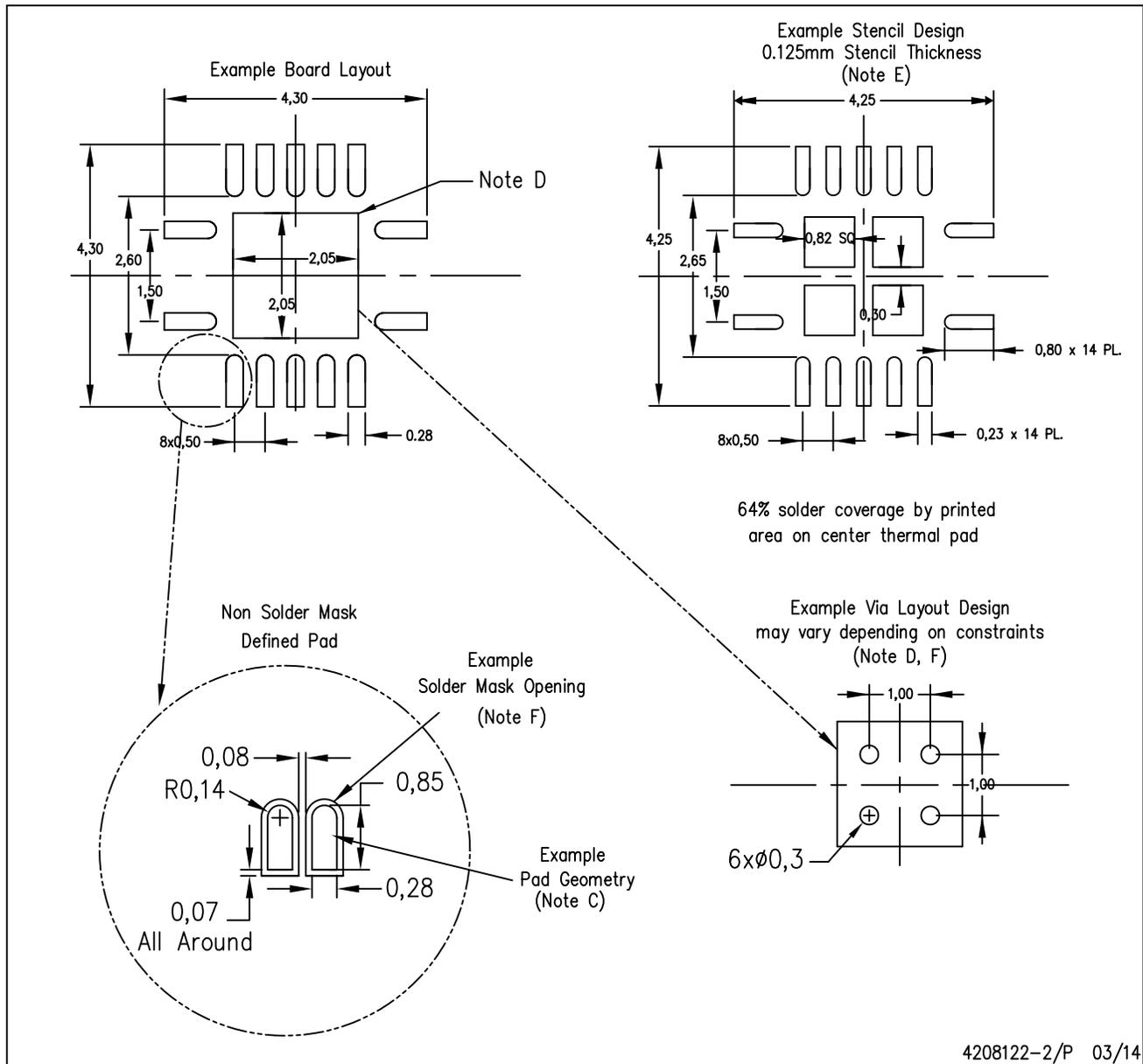
Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



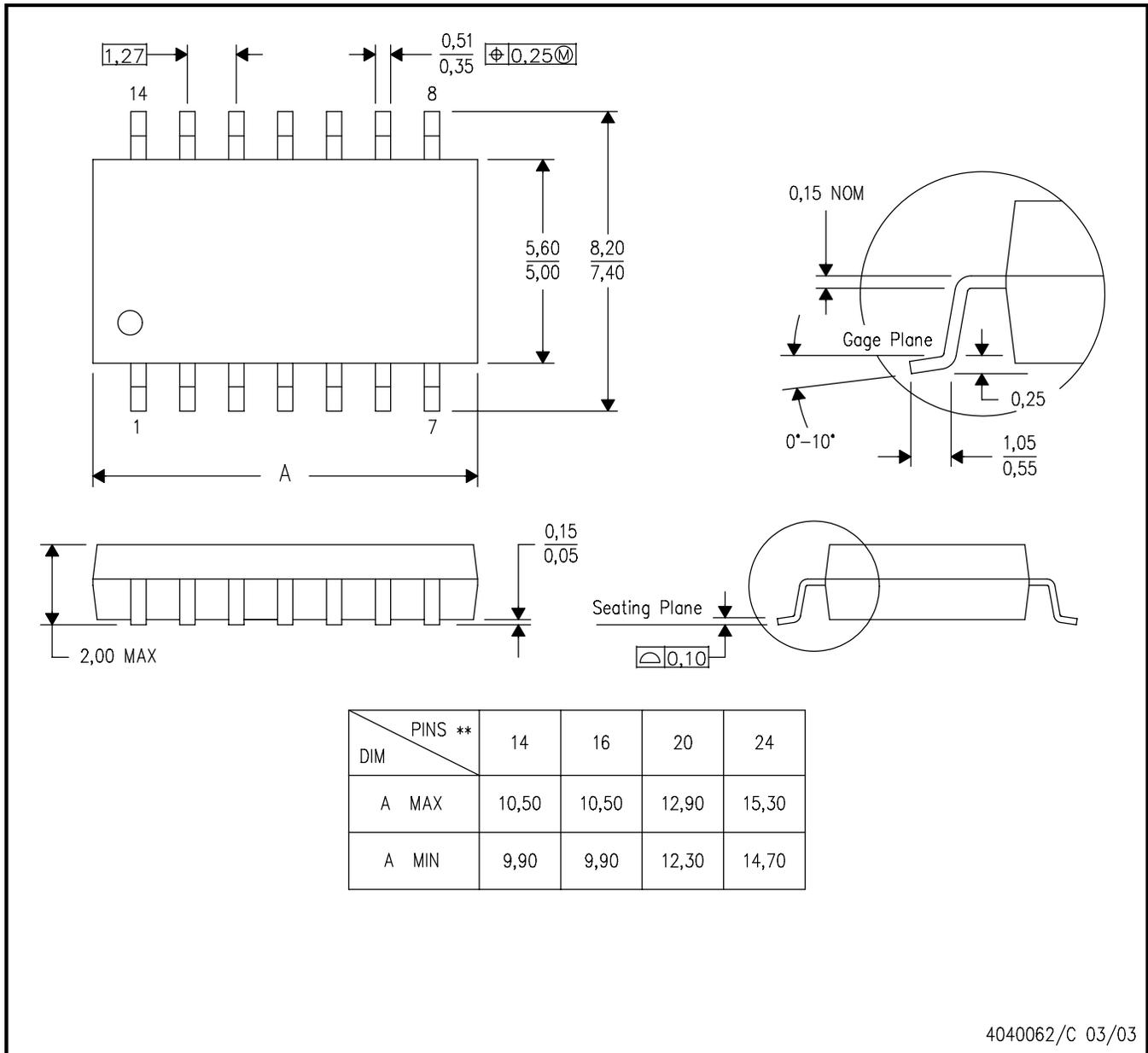
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

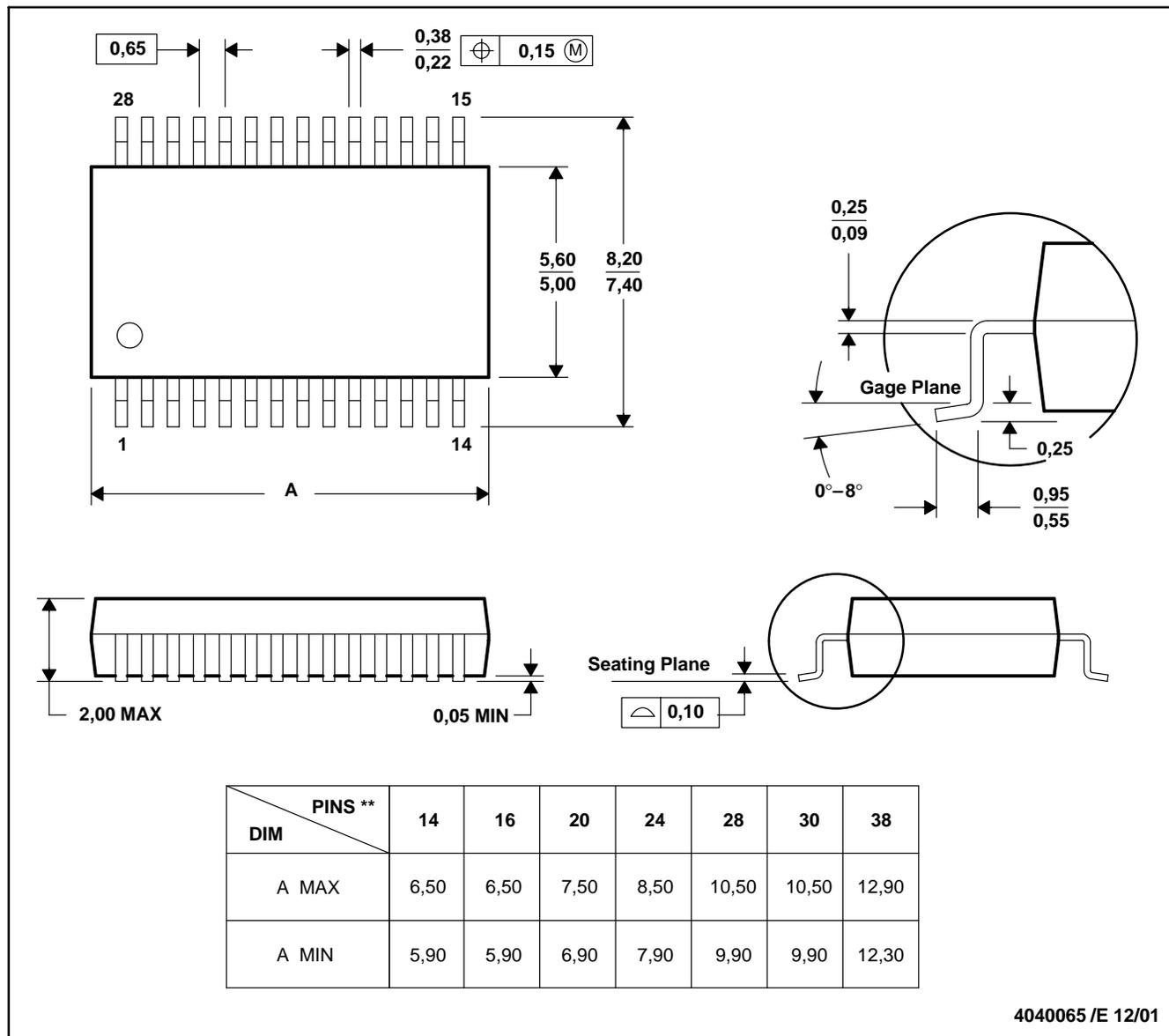


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

4040065 /E 12/01

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Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype [ameyasales1](#) [ameyasales2](#)

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com