

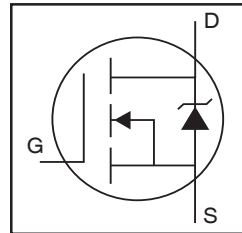
Features

- Advanced Process Technology
- Ultra Low On-Resistance
- Logic Level Gate Drive
- Advanced Process Technology
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *

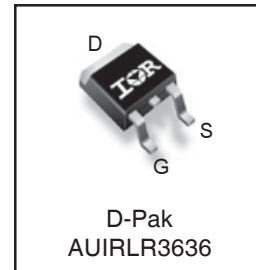
Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

HEXFET® Power MOSFET



V_{DS}	60V
$R_{DS(on)}$ typ. max.	5.4mΩ 6.8mΩ
I_D (Silicon Limited)	99A①
I_D (Package Limited)	50A



G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AU1RLR3636	D-pak	Tube	75	AU1RLR3636
		Tape and Reel	2000	AU1RLR3636TR
		Tape and Reel Left	3000	AU1RLR3636TRL
		Tape and Reel Right	3000	AU1RLR3636TRR

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	99 ①	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	70 ①	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	50	
I_{DM}	Pulsed Drain Current ②	396	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	143	W
	Linear Derating Factor	0.95	W/°C
V_{GS}	Gate-to-Source Voltage	±16	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ③	170	mJ
I_{AR}	Avalanche Current ②	See Fig.14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ
dv/dt	Peak Diode Recovery ④	22	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	1.05	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑤	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at <http://www.irf.com/>

Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.07	—	V/°C	Reference to 25°C, I _D = 5mA②
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	5.4	6.8	mΩ	V _{GS} = 10V, I _D = 50A ⑤
		—	6.6	8.3		V _{GS} = 4.5V, I _D = 50A ⑤
V _{GS(th)}	Gate Threshold Voltage	1.0	—	2.5	V	V _{DS} = V _{GS} , I _D = 100μA
g _{fs}	Forward Transconductance	31	—	—	S	V _{DS} = 25V, I _D = 50A
R _{G(int)}	Internal Gate Resistance	—	0.6	—	Ω	
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 60V, V _{GS} = 0V
		—	—	250		V _{DS} = 60V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -16V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Q _g	Total Gate Charge	—	33	49	nC	I _D = 50A
Q _{gs}	Gate-to-Source Charge	—	11	—		V _{DS} = 30V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	15	—		V _{GS} = 4.5V ⑤
Q _{sync}	Total Gate Charge Sync. (Q _g - Q _{gd})	—	18	—		I _D = 50A, V _{DS} = 0V, V _{GS} = 4.5V
t _{d(on)}	Turn-On Delay Time	—	45	—	ns	V _{DD} = 39V
t _r	Rise Time	—	216	—		I _D = 50A
t _{d(off)}	Turn-Off Delay Time	—	43	—		R _G = 7.5 Ω
t _f	Fall Time	—	69	—		V _{GS} = 4.5V ⑤
C _{iss}	Input Capacitance	—	3779	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	332	—		V _{DS} = 50V
C _{rss}	Reverse Transfer Capacitance	—	163	—		f = 1.0MHz
C _{oss} eff. (ER)	Effective Output Capacitance (Energy Related)⑦	—	437	—		V _{GS} = 0V, V _{DS} = 0V to 48V ⑦, See Fig.11
C _{oss} eff. (TR)	Effective Output Capacitance (Time Related) ⑥	—	636	—		V _{GS} = 0V, V _{DS} = 0V to 48V ⑥

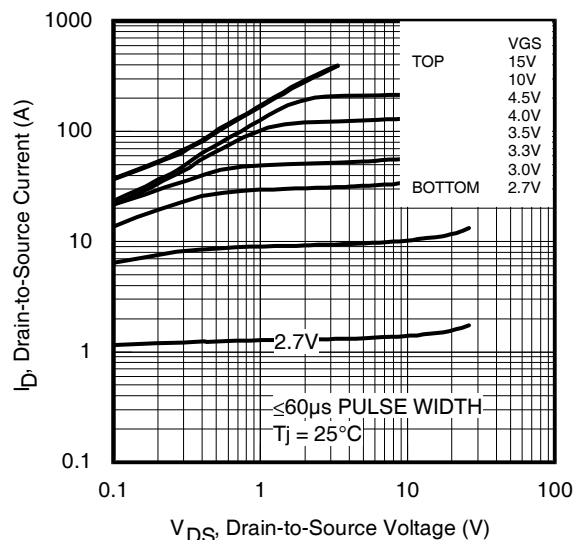
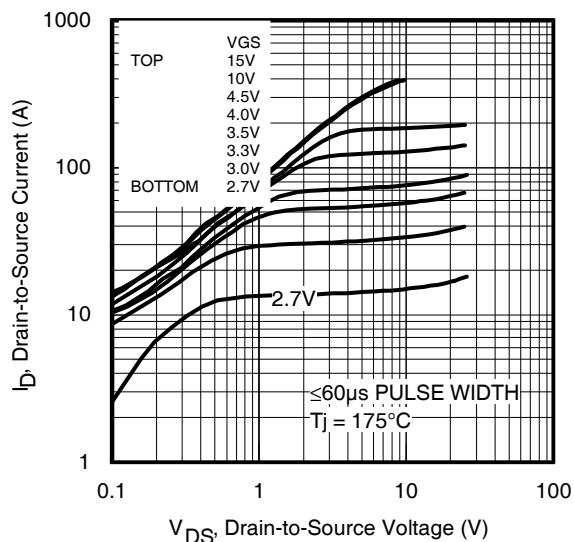
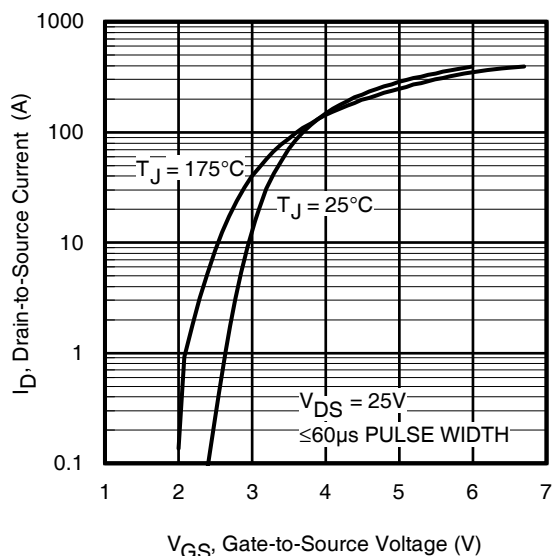
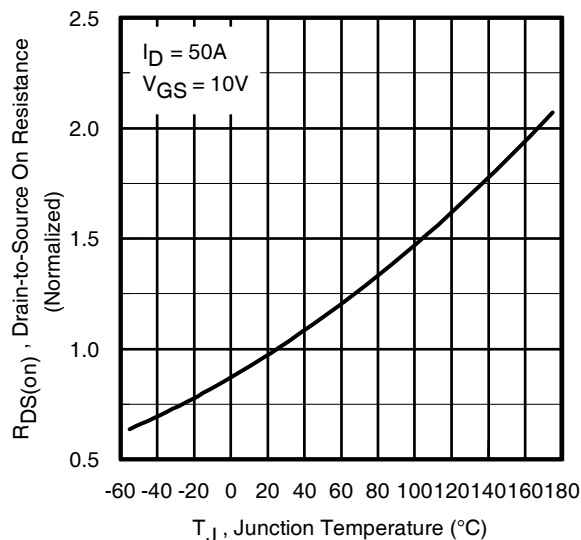
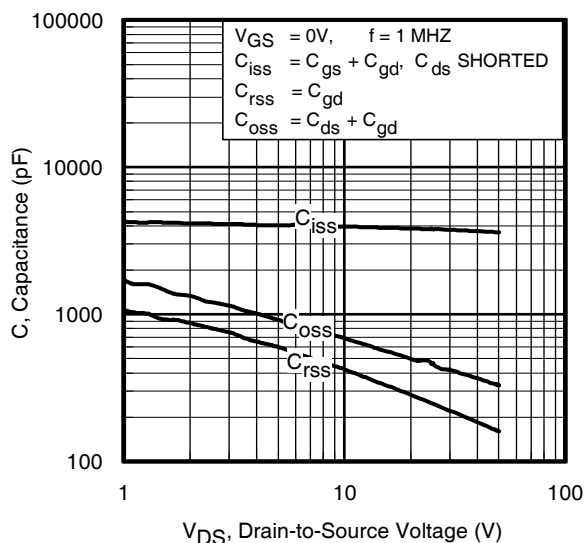
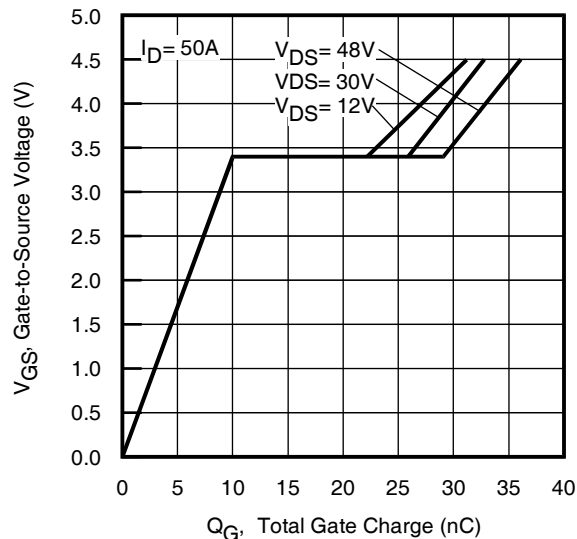
Diode Characteristics

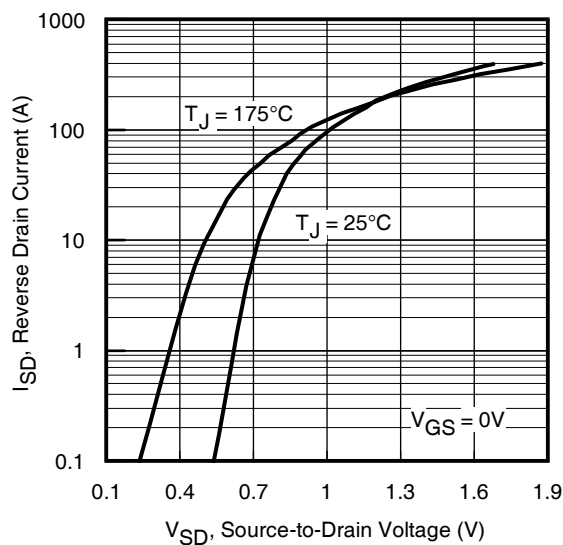
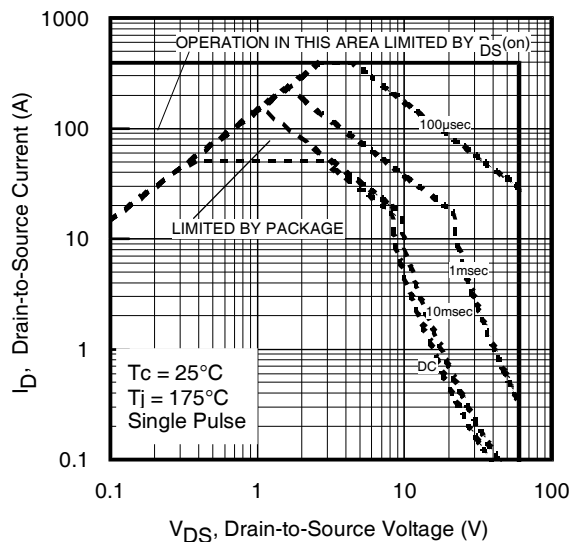
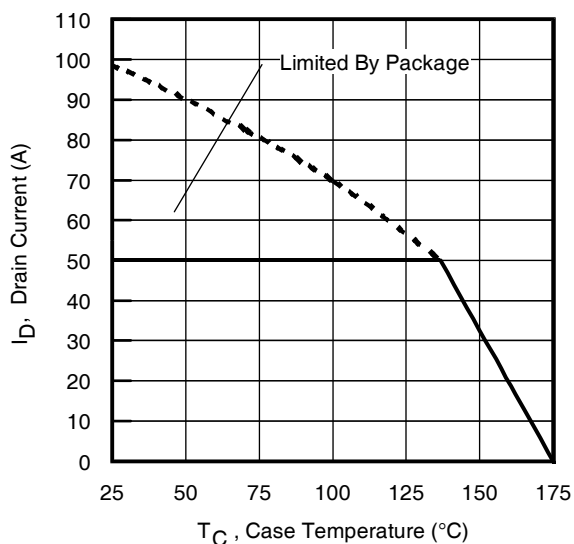
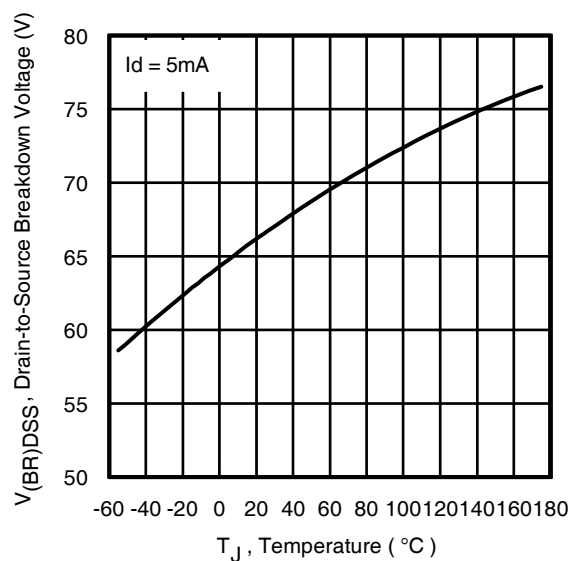
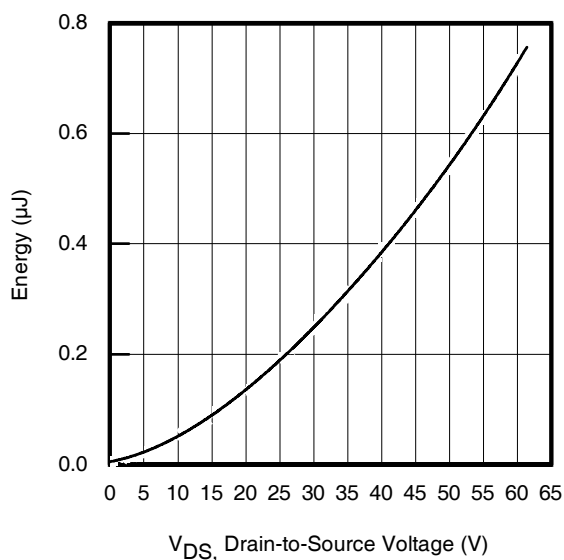
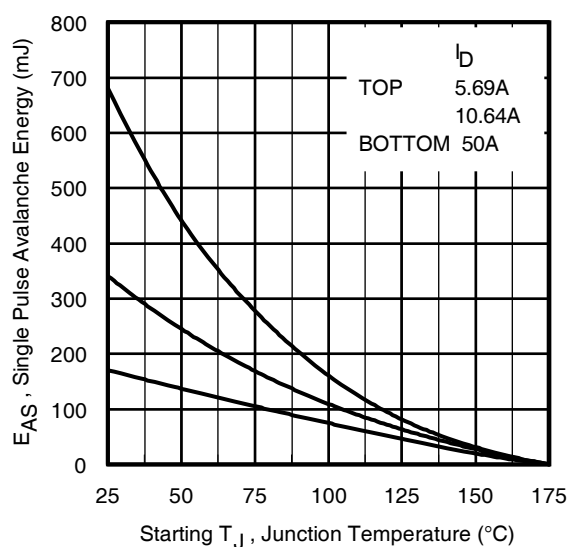
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	99 ①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ②	—	—	396		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 50A, V _{GS} = 0V ⑤
t _{rr}	Reverse Recovery Time	—	27	—	ns	T _J = 25°C V _R = 51V,
		—	32	—		T _J = 125°C I _F = 50A
Q _{rr}	Reverse Recovery Charge	—	31	—	nC	T _J = 25°C di/dt = 100A/μs ⑤
		—	43	—		T _J = 125°C
I _{RRM}	Reverse Recovery Current	—	2.1	—	A	T _J = 25°C
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

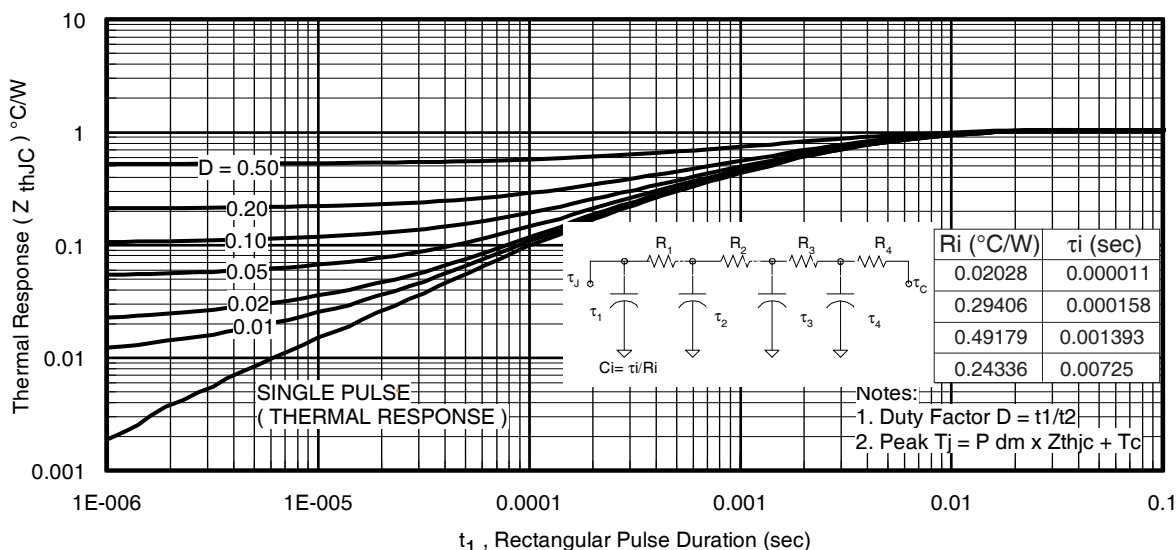
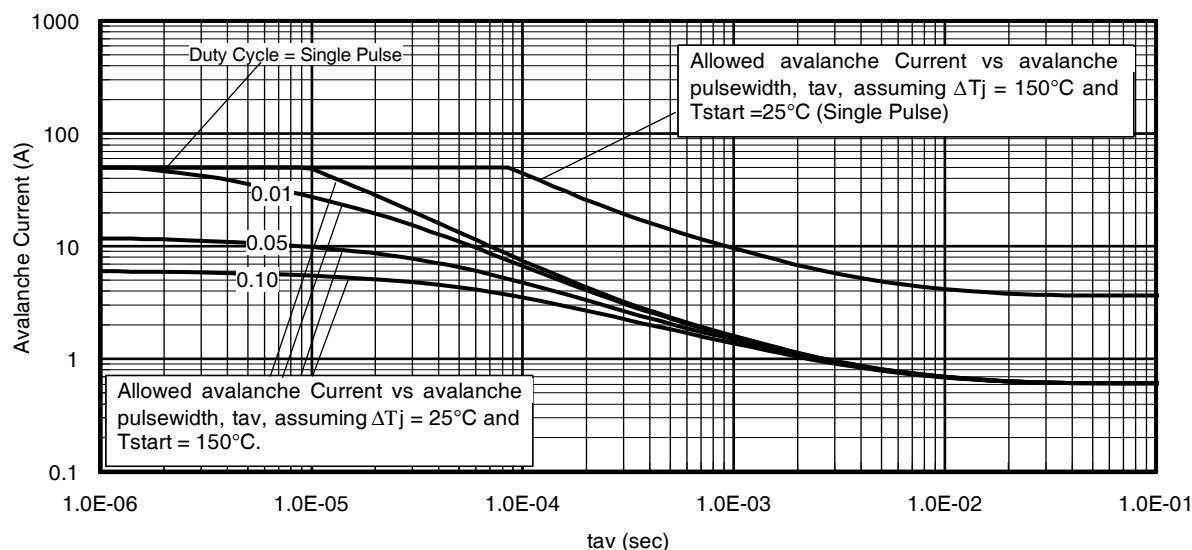
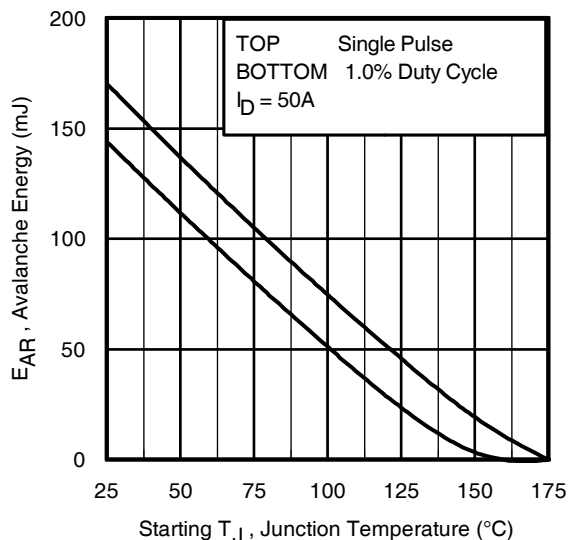
Notes:

- ① Calculated continuous current based on maximum allowable junction temperature Bond wire current limit is 50A. Note that current limitation arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.136 mH
R_G = 25Ω, I_{AS} = 50A, V_{GS} = 10V. Part not recommended for use above this value.
- ④ I_{SD} ≤ 50A, di/dt ≤ 1109 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.

- ⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniquea refer to application note # AN- 994 echniques refer to application note #AN-994.
- ⑨ R_θ is measured at T_J approximately 90°C.


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Drain-to-Source Breakdown Voltage

Fig 11. Typical C_{OSS} Stored Energy

Fig 12. Maximum Avalanche Energy vs. Drain Current

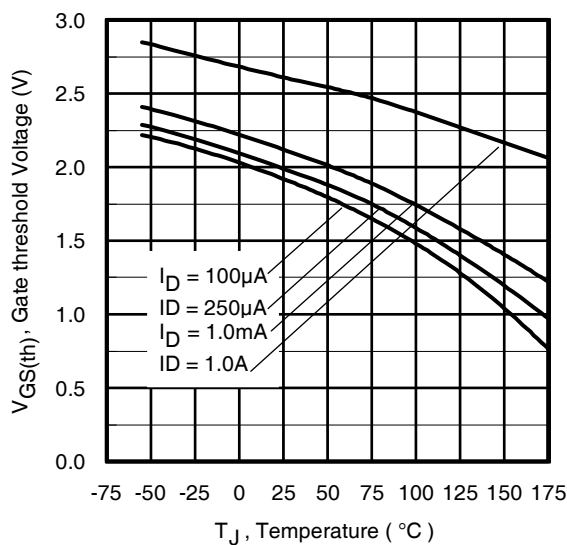
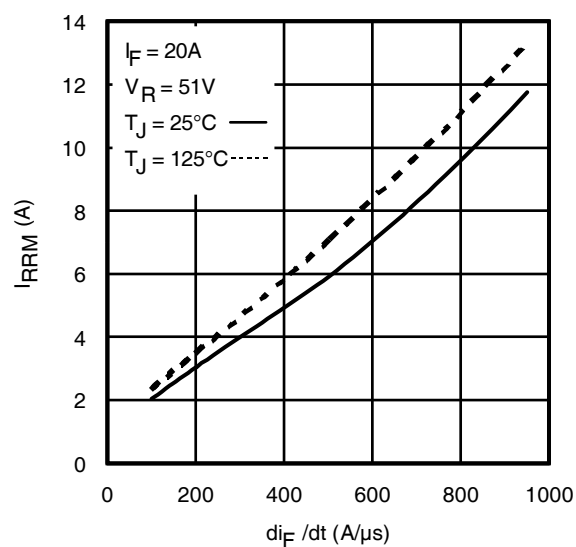
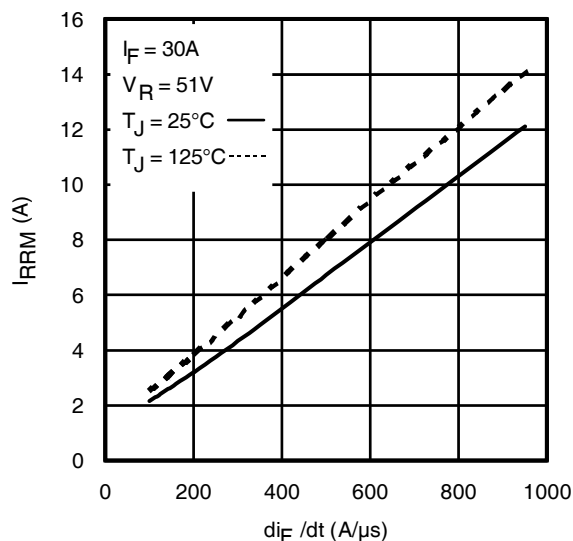
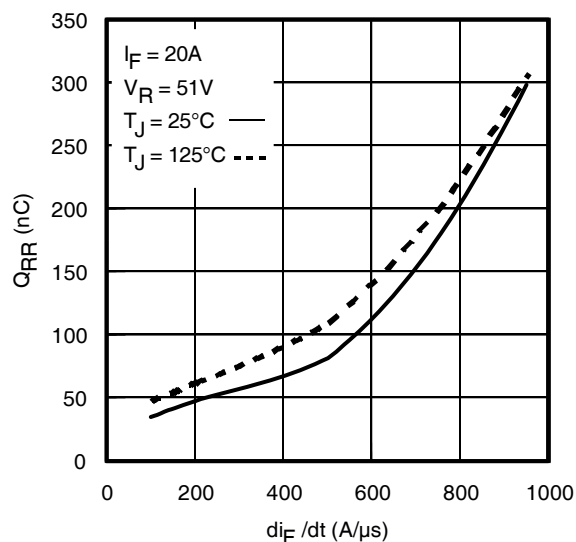
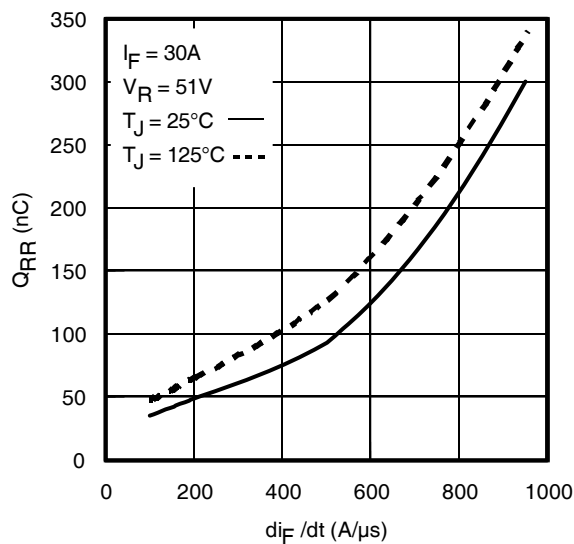

Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Typical Avalanche Current vs. Pulsewidth

Fig 15. Maximum Avalanche Energy vs. Temperature
Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) \cdot \Delta T / Z_{thJC}$$

$$I_{av} = 2 \Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


Fig 16. Threshold Voltage vs. Temperature

Fig. 17 - Typical Recovery Current vs. di_F/dt

Fig. 18 - Typical Recovery Current vs. di_F/dt

Fig. 19 - Typical Stored Charge vs. di_F/dt

Fig. 20 - Typical Stored Charge vs. di_F/dt

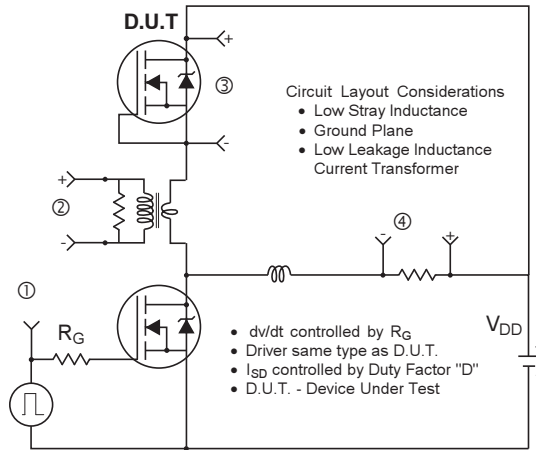
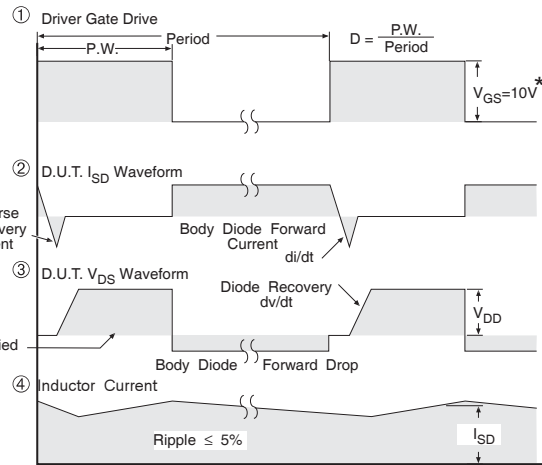


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



* $V_{GS} = 5V$ for Logic Level Devices

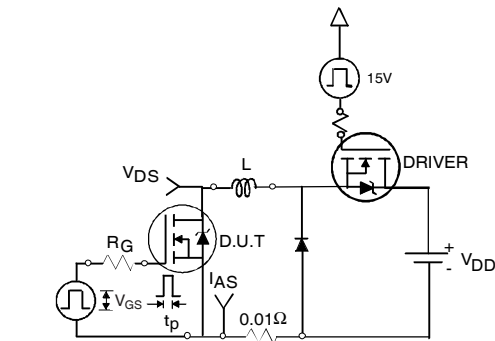


Fig 22a. Unclamped Inductive Test Circuit

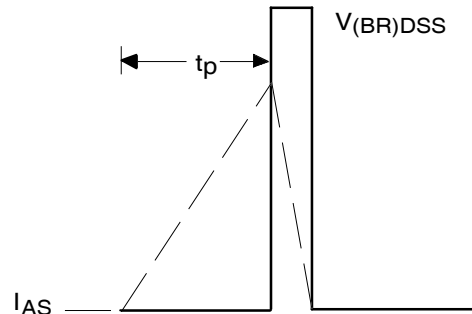


Fig 22b. Unclamped Inductive Waveforms

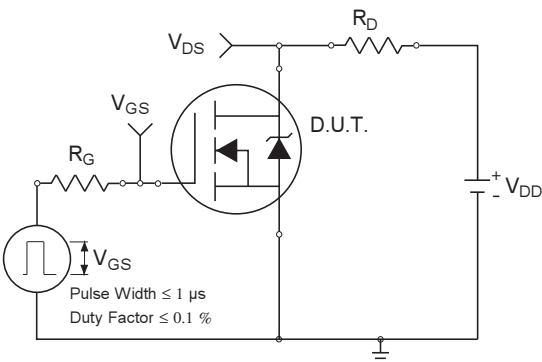


Fig 23a. Switching Time Test Circuit

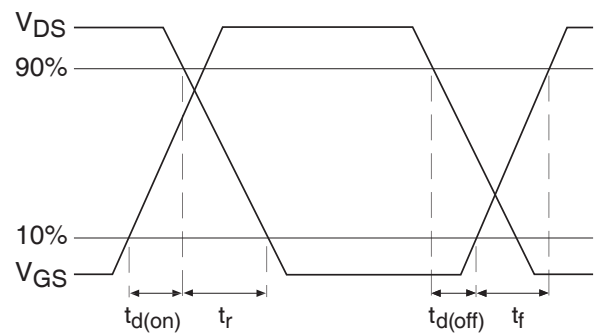


Fig 23b. Switching Time Waveforms

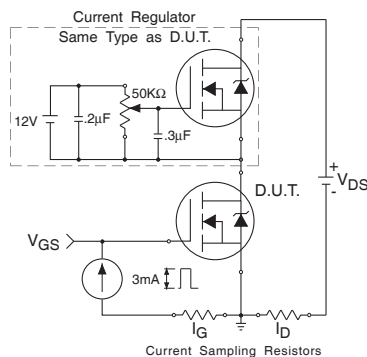


Fig 24a. Gate Charge Test Circuit

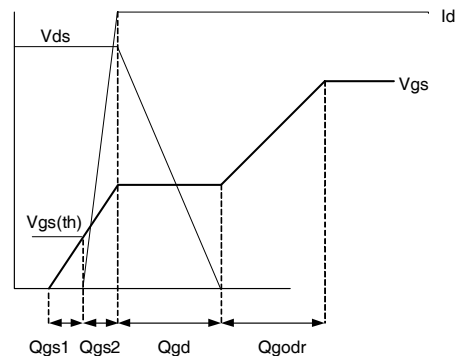
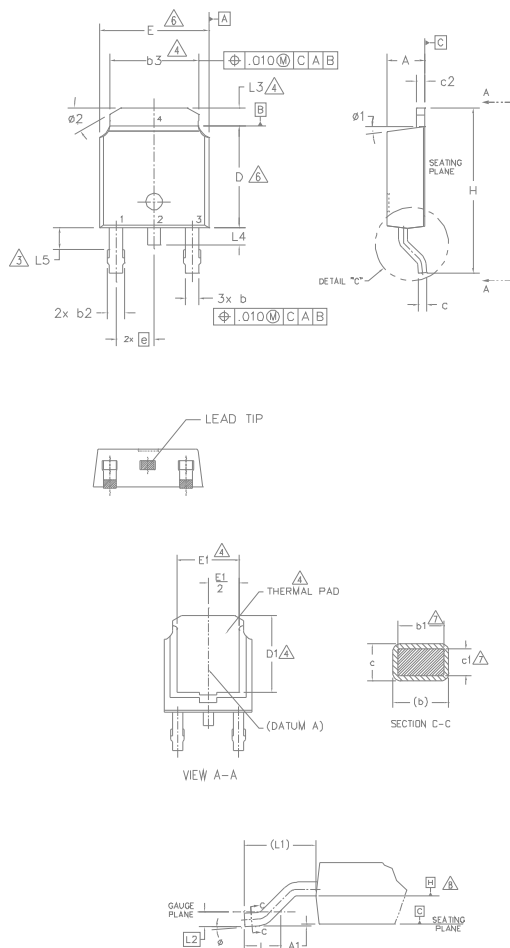


Fig 24b. Gate Charge Waveform

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	7
A1	—	0.13	—	.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	.031	4
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	7
c1	0.41	0.56	.016	.022	
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	—	.205	—	
E	6.35	6.73	.250	.265	4
E1	4.32	—	.170	—	
e	2.29 BSC		.090 BSC		4
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		3
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4	—	1.02	—	.040	3
L5	1.14	1.52	.045	.060	
ø	0"	10"	0"	10"	
ø1	0"	15"	0"	15"	3
ø2	25"	35"	25"	35"	

LEAD ASSIGNMENTS

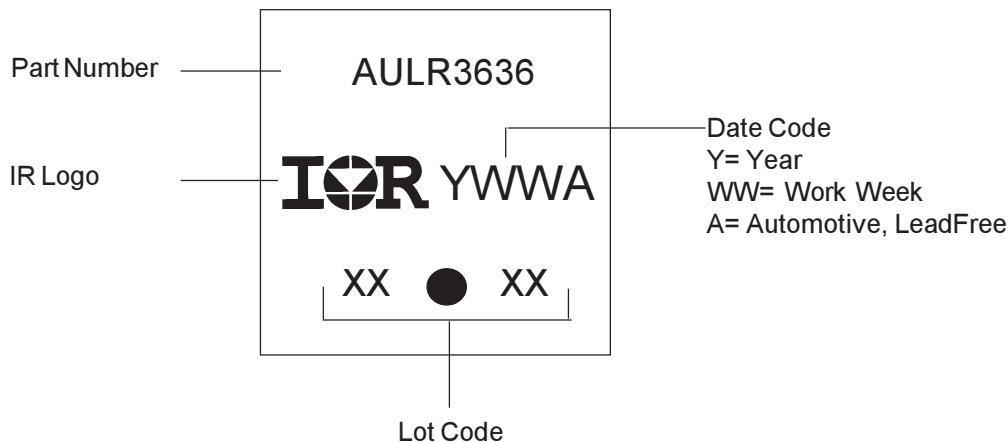
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

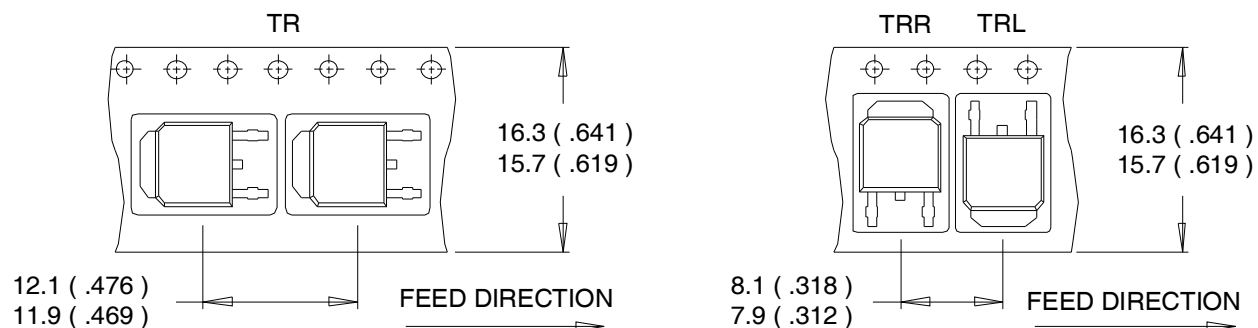
D-Pak (TO-252AA) Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

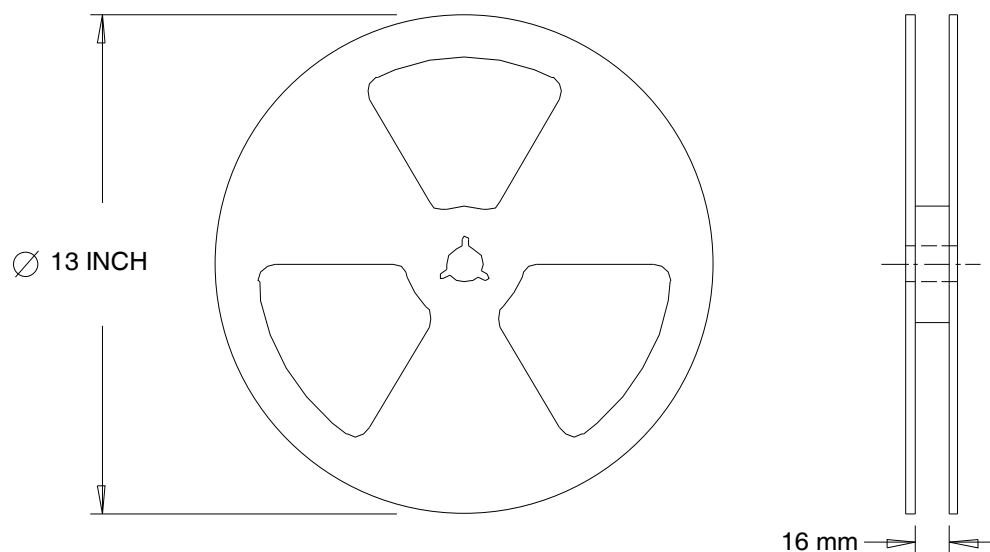
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level		Automotive (per AEC-Q101) ^{††}	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D-PAK	MSL1
ESD	Machine Model	Class M4 (+/- 600V) ^{†††} AEC-Q101-002	
	Human Body Model	Class H1C (+/- 2000V) ^{†††} AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V) ^{†††} AEC-Q101-005	
RoHS Compliant		Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

^{††} Exceptions (if any) to AEC-Q101 requirements are noted in the qualification report.

^{†††} Highest passing voltage.

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For technical support, please contact IR's Technical Assistance Center

<http://www.irf.com/technical-info/>

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Revision History

Date	Comments
3/18/2014	- Added "Logic Level Gate Drive" bullet in the features section on page 1 - Updated data sheet with new IR corporate template
4/9/2014	- Updated package outline on page 8. - Updated typo on the fig.19 and fig.20, unit of y-axis from "A" to "nC" on page 6.

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