74HC4066; 74HCT4066

Quad single-pole single-throw analog switch

Rev. 7 — 2 April 2013 **Product data sheet**

1. General description

The 74HC4066; 74HCT4066 is a quad single pole, single throw analog switch. Each switch features two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Input levels nE inputs:
  - For 74HC4066: CMOS level
  - For 74HCT4066: TTL level
- Low ON resistance:
  - 50 Ω (typical) at V_{CC} = 4.5 V
  - 45 Ω (typical) at V_{CC} = 6.0 V
  - 35 Ω (typical) at V_{CC} = 9.0 V
- Specified in compliance with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4066N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HCT4066N				
74HC4066D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT4066D				
74HC4066DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT4066DB				
74HC4066PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT4066PW				
74HC4066BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT4066BQ				

4. Functional diagram

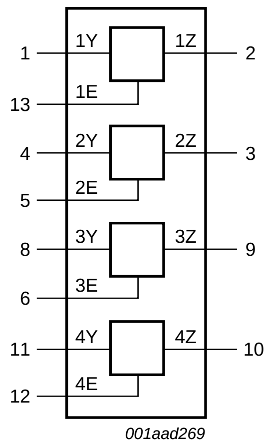


Fig 1. Logic symbol

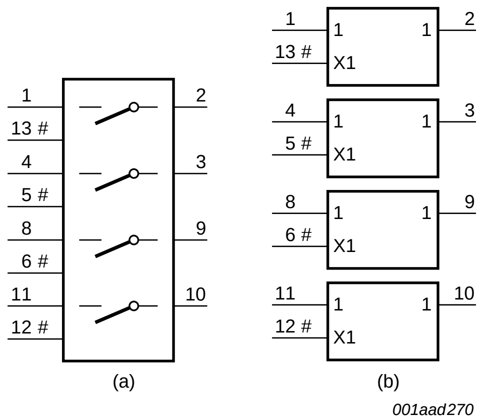


Fig 2. IEC logic symbol

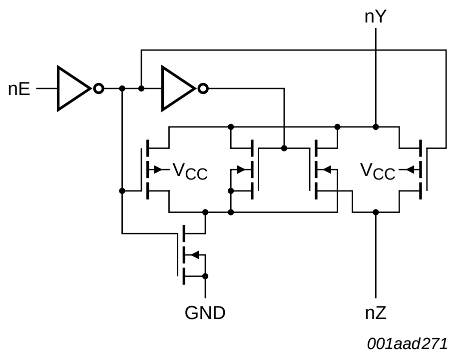


Fig 3. Schematic diagram (one switch)

5. Pinning information

5.1 Pinning

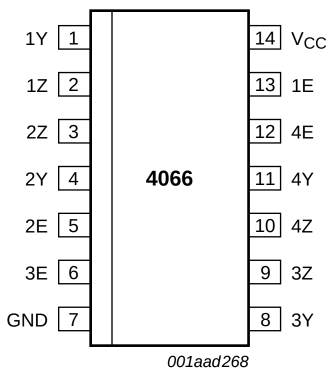
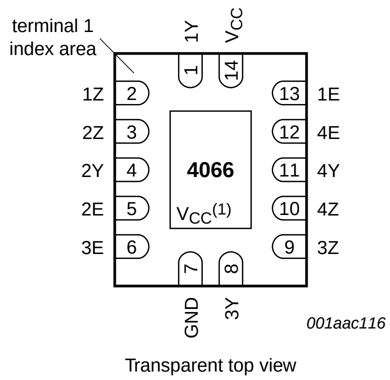


Fig 4. Pin configuration for DIP14, SO14, SSOP14 and TSSOP14



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to VCC.

Fig 5. Pin configuration for DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1Z, 2Z, 3Z, 4Z	2, 3, 9, 10	independent input or output
1Y, 2Y, 3Y, 4Y	1, 4, 8, 11	independent input or output
GND	7	ground (0 V)
1E, 2E, 3E, 4E	13, 5, 6, 12	enable input (active HIGH)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input nE	Switch
L	OFF
H	ON

[1] H = HIGH voltage level;
L = LOW voltage level.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+11.0	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{SK}	switch clamping current	$V_{SW} < –0.5$ V or $V_{SW} > V_{CC} + 0.5$ V		-	±20	mA
I_{SW}	switch current	$V_{SW} = –0.5$ V to $V_{CC} + 0.5$ V	[1]	-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-	–50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]			
		DIP14 package			-	750
		SO14, (T)SSOP14 and DHVQFN14 packages			-	500
P	power dissipation	per switch		-	100	mW

[1] To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Yn. In this case there is no limit for the voltage drop across the switch, but the voltages at Yn and Z may not exceed V_{CC} or GND.

[2] For DIP14 package: P_{tot} derates linearly with 12 mW/K above 70 °C.
For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4066			74HCT4066			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	10.0	4.5	5.0	5.5	V
V_I	input voltage		GND	-	V_{CC}	GND	-	V_{CC}	V
V_{SW}	switch voltage		GND	-	V_{CC}	GND	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V
		V_{CC} = 10.0 V	-	-	35	-	-	-	ns/V

9. Static characteristics

Table 6. R_{ON} resistance per switch for types 74HC4066 and 74HCT4066

$V_I = V_{IH}$ or V_{IL}; for test circuit see Figure 6.
V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.
For 74HC4066: V_{CC} – GND = 2.0 V, 4.5 V, 6.0 V and 9.0 V.
For 74HCT4066: V_{CC} – GND = 4.5 V.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	V_{is} = V_{CC} to GND							
		V_{CC} = 2.0 V; I_{SW} = 100 μA	[2]	-	-	-	-	-	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 μA		-	54	-	118	142	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 μA		-	42	-	105	126	Ω
		V_{CC} = 9.0 V; I_{SW} = 1000 μA		-	32	-	88	105	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_{is} = GND							
		V_{CC} = 2.0 V; I_{SW} = 100 μA	[2]	-	80	-	-	-	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 μA		-	35	-	95	115	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 μA		-	27	-	82	100	Ω
		V_{CC} = 9.0 V; I_{SW} = 1000 μA		-	20	-	70	85	Ω
		V_{is} = V_{CC}							
		V_{CC} = 2.0 V; I_{SW} = 100 μA	[2]	-	100	-	-	-	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 μA		-	42	-	106	128	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 μA		-	35	-	94	113	Ω
		V_{CC} = 9.0 V; I_{SW} = 1000 μA		-	20	-	78	95	Ω

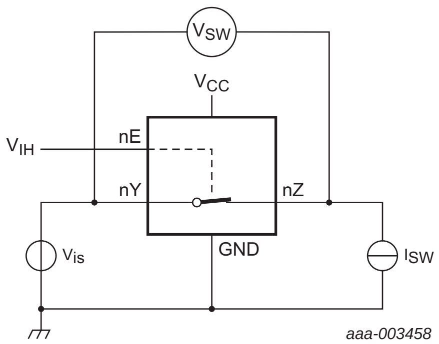
Table 6. R_{ON} resistance per switch for types 74HC4066 and 74HCT4066 *…continued*

$V_I = V_{IH}$ or V_{IL}; for test circuit see Figure 6.
V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.
For 74HC4066: $V_{CC} - GND$ = 2.0 V, 4.5 V, 6.0 V and 9.0 V.
For 74HCT4066: $V_{CC} - GND$ = 4.5 V.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
ΔR_{ON}	ON resistance mismatch between channels	$V_{is} = V_{CC}$ to GND							
		V_{CC} = 2.0 V	[2]	-	-	-	-	-	Ω
		V_{CC} = 4.5 V		-	5	-	-	-	Ω
		V_{CC} = 6.0 V		-	4	-	-	-	Ω
		V_{CC} = 9.0 V		-	3	-	-	-	Ω

[1] Typical values are measured at T_{amb} = 25 °C.

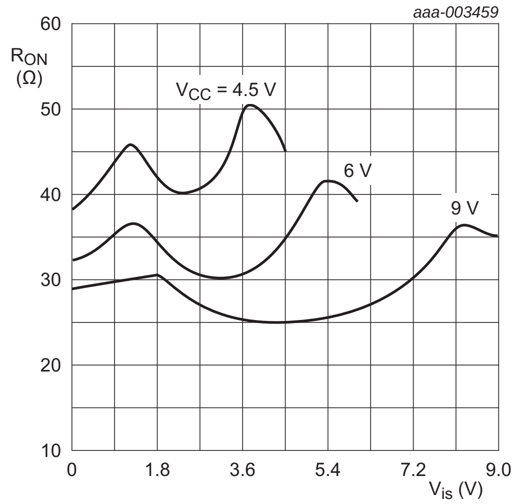
[2] At supply voltages ($V_{CC} - GND$) approaching 2 V, the analog switch ON resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.



V_{is} = 0 V to V_{CC}

$$R_{ON} = \frac{V_{SW}}{I_{SW}}$$

Fig 6. Test circuit for measuring R_{ON}



V_{is} = 0 V to V_{CC}

Fig 7. Typical R_{ON} as a function of input voltage V_{is}

Table 7. Static characteristics 74HC4066

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).
V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
		V_{CC} = 9.0 V	6.3	4.7	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.80	V
		V_{CC} = 9.0 V	-	4.3	2.70	V
I_I	input leakage current	V_I = V_{CC} or GND				
		V_{CC} = 6.0 V	-	-	±1.0	μA
		V_{CC} = 10.0 V	-	-	±2.0	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} – GND; see Figure 8				
		per channel	-	-	±1.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} – GND; see Figure 9	-	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{is} = GND or V_{CC}; V_{os} = V_{CC} or GND				
		V_{CC} = 6.0 V	-	-	20.0	μA
		V_{CC} = 10.0 V	-	-	40.0	μA
C_I	input capacitance		-	3.5	-	pF
C_{sw}	switch capacitance		-	8	-	pF
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
		V_{CC} = 9.0 V	6.3	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.50	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.80	V
		V_{CC} = 9.0 V	-	-	2.70	V
I_I	input leakage current	V_I = V_{CC} or GND				
		V_{CC} = 6.0 V	-	-	±1.0	μA
		V_{CC} = 10.0 V	-	-	±2.0	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} – GND; see Figure 8				
		per channel	-	-	±1.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} – GND; see Figure 9	-	-	±1.0	μA

Table 7. Static characteristics 74HC4066 *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).
V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{CC}	supply current	$V_I = V_{CC}$ or GND; V_{is} = GND or V_{CC}; $V_{os} = V_{CC}$ or GND				
		V_{CC} = 6.0 V	-	-	40	μA
		V_{CC} = 10.0 V	-	-	80	μA

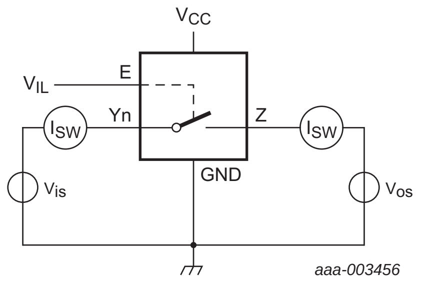
[1] Typical values are measured at T_{amb} = 25 °C.

Table 8. Static characteristics 74HCT4066

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).
V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 5.5 V; $V_I = V_{IH}$ or V_{IL}; $\|V_{SW}\| = V_{CC} - GND$; see Figure 8				
		per channel	-	-	±1.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 5.5 V; $V_I = V_{IH}$ or V_{IL}; $\|V_{SW}\| = V_{CC} - GND$; see Figure 9	-	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; V_{is} = GND or V_{CC}; $V_{os} = V_{CC}$ or GND; V_{CC} = 4.5 V to 5.5 V	-	-	20.0	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V	-	100	450	μA
C_I	input capacitance		-	3.5	-	pF
C_{sw}	switch capacitance		-	8	-	pF
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 5.5 V; $V_I = V_{IH}$ or V_{IL}; $\|V_{SW}\| = V_{CC} - GND$; see Figure 8				
		per channel	-	-	±1.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 5.5 V; $V_I = V_{IH}$ or V_{IL}; $\|V_{SW}\| = V_{CC} - GND$; see Figure 9	-	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; V_{is} = GND or V_{CC}; $V_{os} = V_{CC}$ or GND; V_{CC} = 4.5 V to 5.5 V	-	-	40	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V	-	-	490	μA

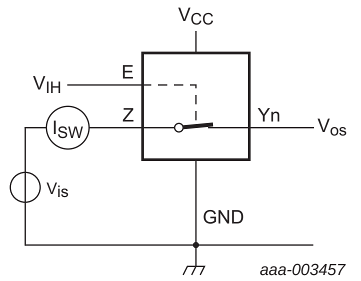
[1] Typical values are measured at T_{amb} = 25 °C.



$V_{is} = V_{CC}$ and V_{os} = GND

V_{is} = GND and $V_{os} = V_{CC}$

Fig 8. Test circuit for measuring OFF-state leakage current



$V_{is} = V_{CC}$ and V_{os} = open

V_{is} = GND and V_{os} = open

Fig 9. Test circuit for measuring ON-state leakage current

10. Dynamic characteristics

Table 9. Dynamic characteristics 74HC4066

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF unless specified otherwise; for test circuit see Figure 12.
V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nY to nZ or nZ to nY; $R_L = \infty\ \Omega$; see Figure 10	[2]						
		V_{CC} = 2.0 V		-	8	75	-	90	ns
		V_{CC} = 4.5 V		-	3	15	-	18	ns
		V_{CC} = 6.0 V		-	2	13	-	15	ns
		V_{CC} = 9.0 V		-	2	10	-	12	ns
t_{off}	turn-off time	nE to nY or nZ; see Figure 11	[4]						
		V_{CC} = 2.0 V		-	44	190	-	225	ns
		V_{CC} = 4.5 V		-	16	38	-	45	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	13	-	-	-	ns
		V_{CC} = 6.0 V		-	13	33	-	38	ns
		V_{CC} = 9.0 V		-	16	26	-	30	ns
t_{on}	turn-on time	nE to nY or nZ; see Figure 11	[3]						
		V_{CC} = 2.0 V		-	36	125	-	150	ns
		V_{CC} = 4.5 V		-	13	25	-	30	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	11	-	-	-	ns
		V_{CC} = 6.0 V		-	10	21	-	26	ns
		V_{CC} = 9.0 V		-	8	16	-	20	ns
C_{PD}	power dissipation capacitance	per switch; V_I = GND to V_{CC}	[5]	11		-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_{on} is the same as t_{PHZ} and t_{PLZ}.

[4] t_{off} is the same as t_{PZH} and t_{PZL}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

$\Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ = sum of outputs;

C_L = output load capacitance in pF;

C_{sw} = switch capacitance in pF;

V_{CC} = supply voltage in V.

Table 10. Dynamic characteristics 74HCT4066

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF unless specified otherwise; for test circuit see Figure 12.
V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nY to nZ or nZ to nY; $R_L = \infty\ \Omega$; see Figure 10	[2]						
		V_{CC} = 4.5 V		-	3	15	-	18	ns
t_{off}	turn-off time	nE to nY or nZ; see Figure 11	[4]						
		V_{CC} = 4.5 V		-	20	44	-	53	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	16	-	-	-	ns
t_{on}	turn-on time	nE to nY or nZ; see Figure 11	[3]						
		V_{CC} = 4.5 V		-	12	30	-	36	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	12	-	-	-	ns
C_{PD}	power dissipation capacitance	per switch; V_I = GND to (V_{CC} − 1.5 V)	[5]	-	12	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_{on} is the same as t_{PHZ} and t_{PLZ}.

[4] t_{off} is the same as t_{PZH} and t_{PZL}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

$\Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ = sum of outputs;

C_L = output load capacitance in pF;

C_{sw} = switch capacitance in pF;

V_{CC} = supply voltage in V.

11. Waveforms

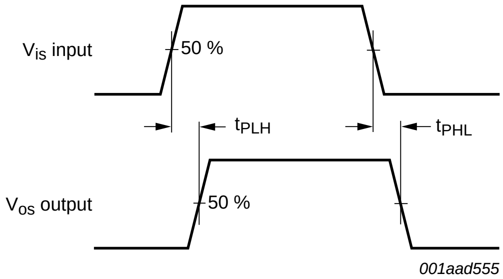
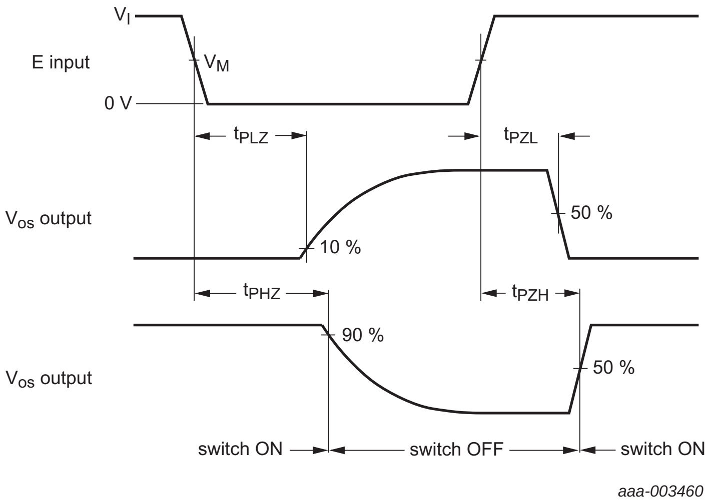


Fig 10. Input (V_{is}) to output (V_{os}) propagation delays

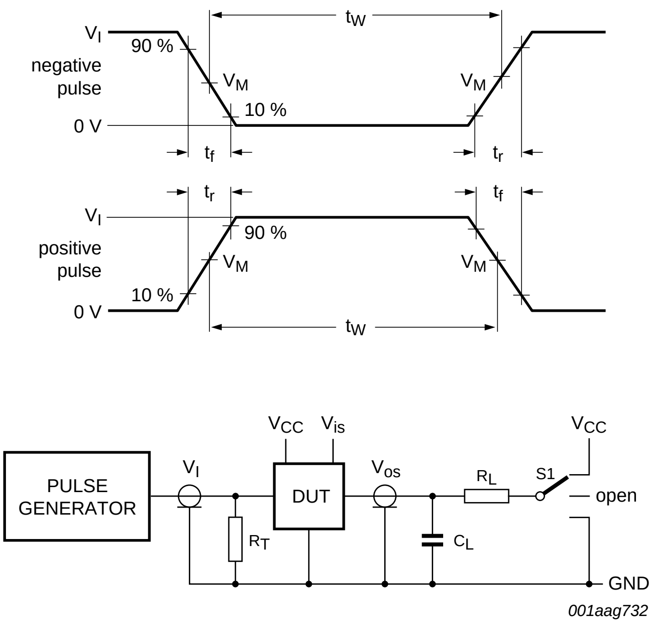


Measurement points are shown in Table 11.

Fig 11. Turn-on and turn-off times

Table 11. Measurement points

Type	V_I	V_M
74HC4066	V_{CC}	$0.5V_{CC}$
74HCT4066	3.0 V	1.3 V



Test data is given in Table 12.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistor.

S1 = Test selection switch.

Fig 12. Load circuitry for measuring switching times

Table 12. Test data

Test	Input			Output		S1 position
	Control E	Switch Yn (Z)	t_r, t_f	Switch Z (Yn)		
	V_I[1]	V_{is}		C_L	R_L	
t_{PHL}, t_{PLH}	GND	GND to V_{CC}	6 ns	50 pF	-	open
t_{PHZ}, t_{PZH}	GND to V_{CC}	V_{CC}	6 ns	50 pF, 15 pF	1 kΩ	GND
t_{PLZ}, t_{PZL}	GND to V_{CC}	GND	6 ns	50 pF, 15 pF	1 kΩ	V_{CC}

[1] For 74HCT4066: maximum input voltage V_I = 3.0 V.

12. Additional dynamic characteristics

Table 13. Additional dynamic characteristics

Recommended conditions and typical values; GND = 0 V; T_{amb} = 25 °C.
V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
THD	total harmonic distortion	f_i = 1 kHz; R_L = 10 kΩ; C_L = 50 pF; see Figure 13					%
		V_{CC} = 4.5 V; V_I = 4.0 V (p-p)		-	0.04	-	%
		V_{CC} = 9.0 V; V_I = 8.0 V (p-p)		-	0.02	-	%
		f_i = 10 kHz; R_L = 10 kΩ; C_L = 50 pF; see Figure 13					
		V_{CC} = 4.5 V; V_I = 4.0 V (p-p)		-	0.12	-	%
		V_{CC} = 9.0 V; V_I = 8.0 V (p-p)		-	0.06	-	%
$f_{(-3dB)}$	−3 dB frequency response	R_L = 50 Ω; C_L = 10 pF; see Figure 15	[2]				
		V_{CC} = 4.5 V		-	180	-	MHz
		V_{CC} = 9.0 V		-	200	-	MHz
α_{iso}	isolation (OFF-state)	R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; see Figure 14	[1]				
		V_{CC} = 4.5 V		-	−50	-	dB
		V_{CC} = 9.0 V		-	−50	-	dB
V_{ct}	crosstalk voltage	between digital input and switch (peak to peak value); R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; see Figure 16					
		V_{CC} = 4.5 V		-	110	-	mV
		V_{CC} = 9.0 V		-	220	-	mV
Xtalk	crosstalk	between switches; R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; see Figure 17	[1]				
		V_{CC} = 4.5 V		-	−60	-	dB
		V_{CC} = 9.0 V		-	−60	-	dB

[1] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).

[2] Adjust input voltage V_{is} to 0 dBm level at V_{os} for f_i = 1 MHz (0 dBm = 1 mW into 50 Ω). After set-up, f_i is increased to obtain a reading of −3 dB at V_{os}.

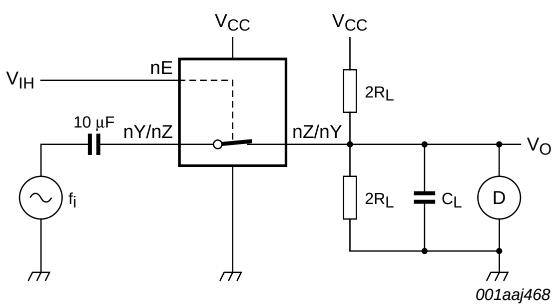
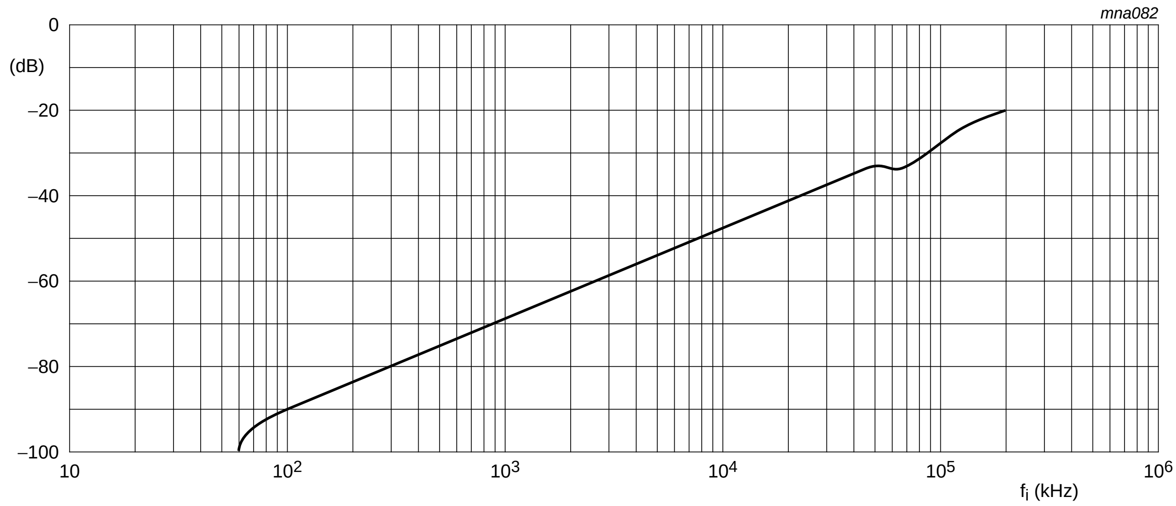
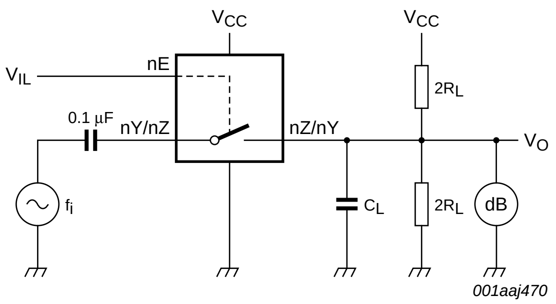


Fig 13. Test circuit for measuring total harmonic distortion



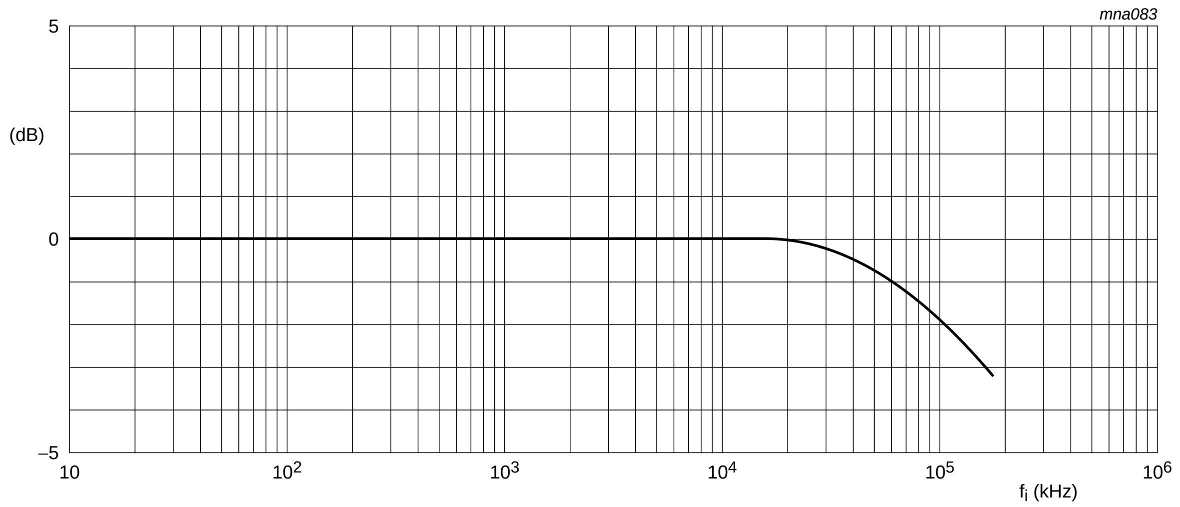
a. Isolation (OFF-state)



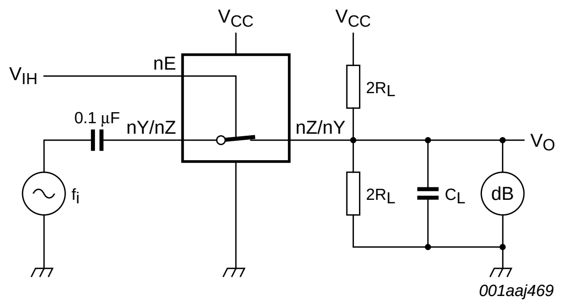
b. Test circuit

V_{CC} = 4.5 V; GND = 0 V; R_L = 600 Ω; R_{source} = 1 kΩ.

Fig 14. Isolation (OFF-state) as a function of frequency



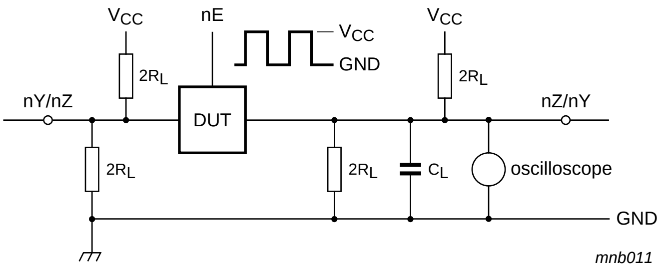
a. Typical −3 dB frequency response



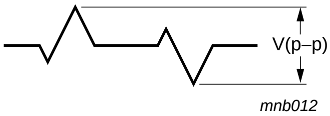
b. Test circuit

V_{CC} = 4.5 V; GND = 0 V; R_L = 50 Ω; R_{source} = 1 kΩ.

Fig 15. −3 dB frequency response



a. Circuit



b. Crosstalk voltage

Fig 16. Test circuit for measuring crosstalk voltage (between the digital input and the switch)

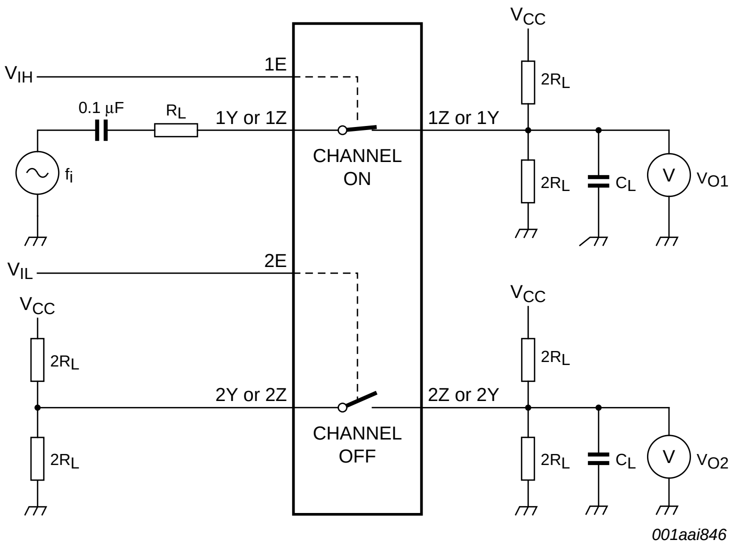
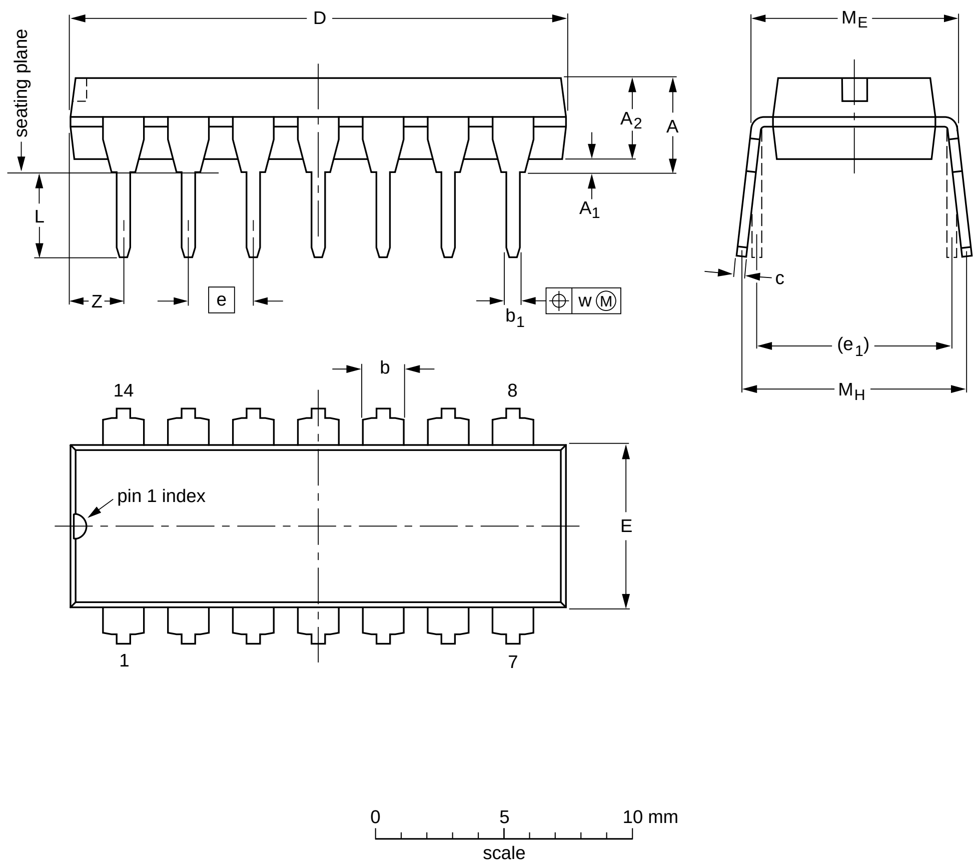


Fig 17. Test circuit for measuring crosstalk (between the switches)

13. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

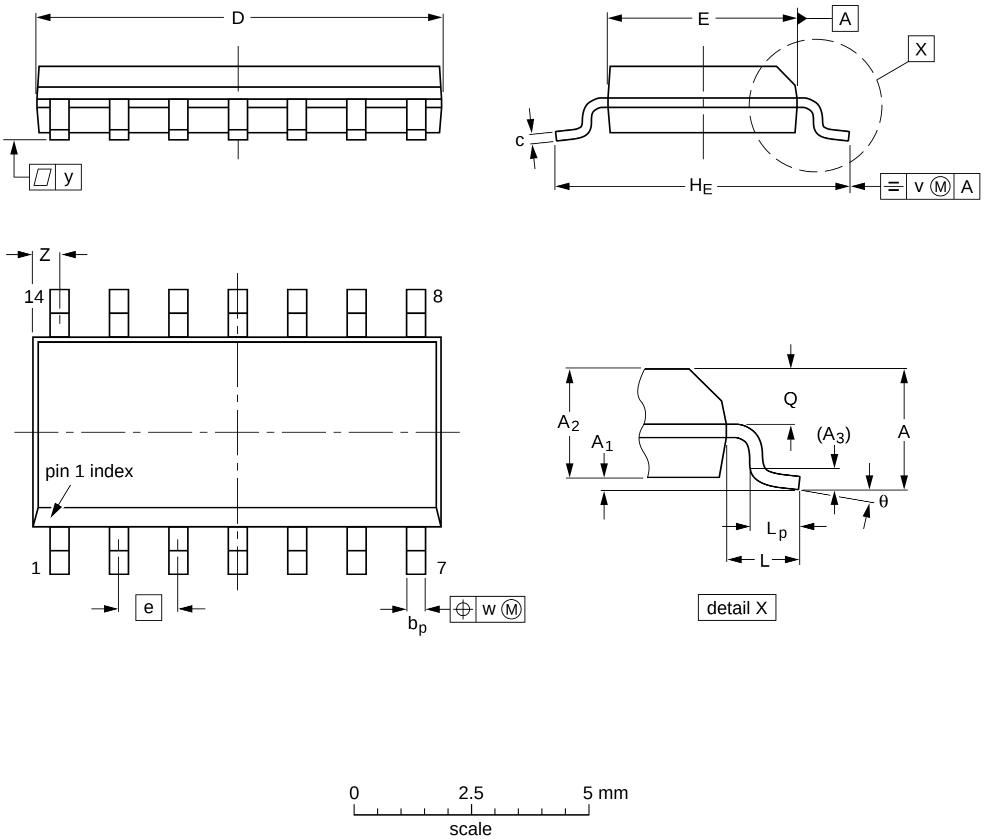
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 18. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

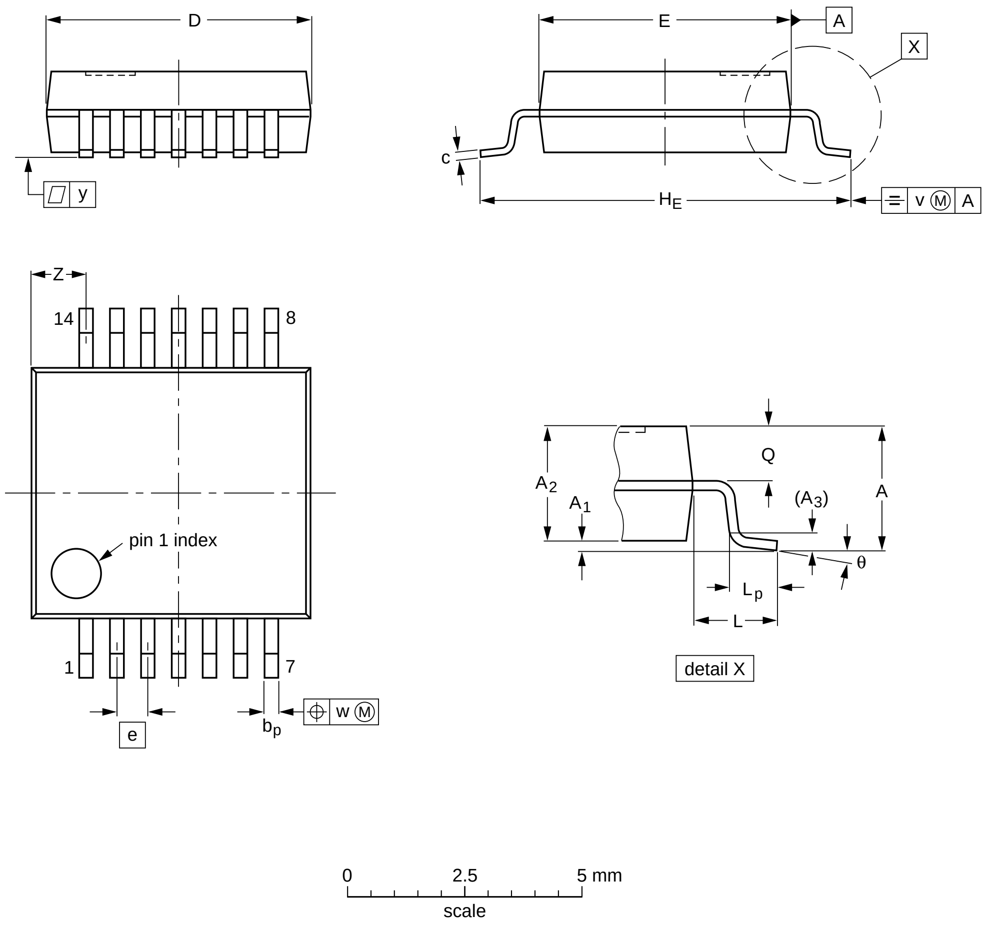
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 19. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

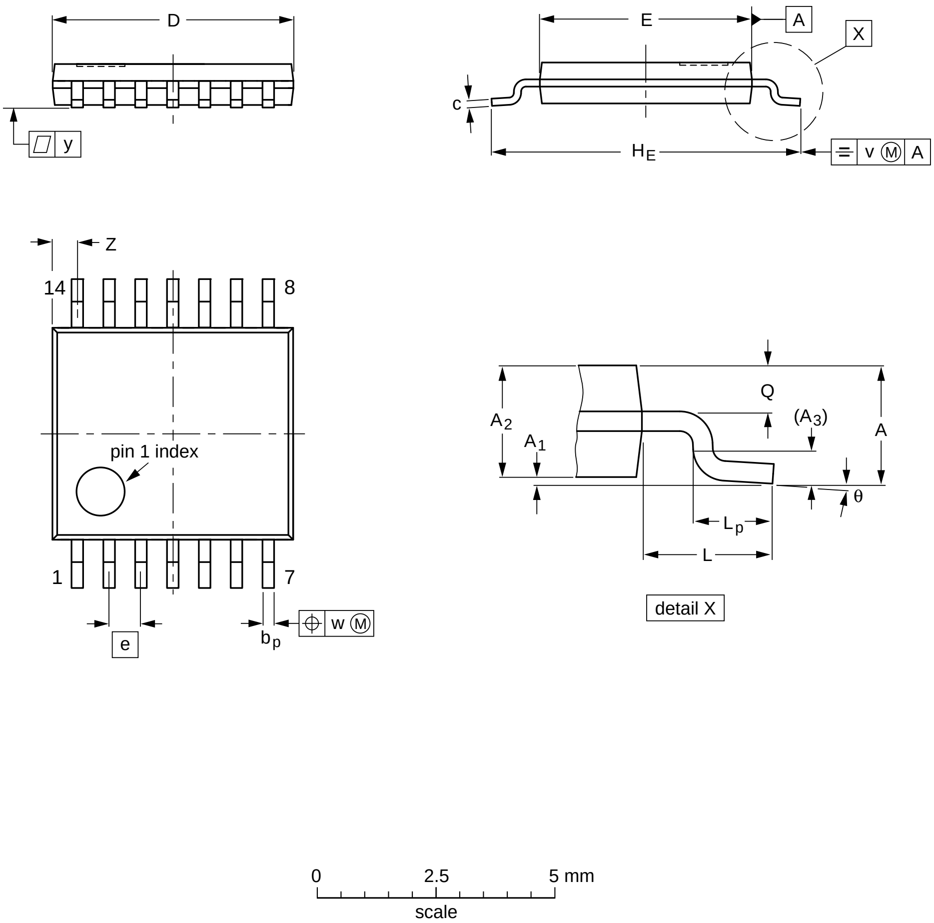
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 20. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

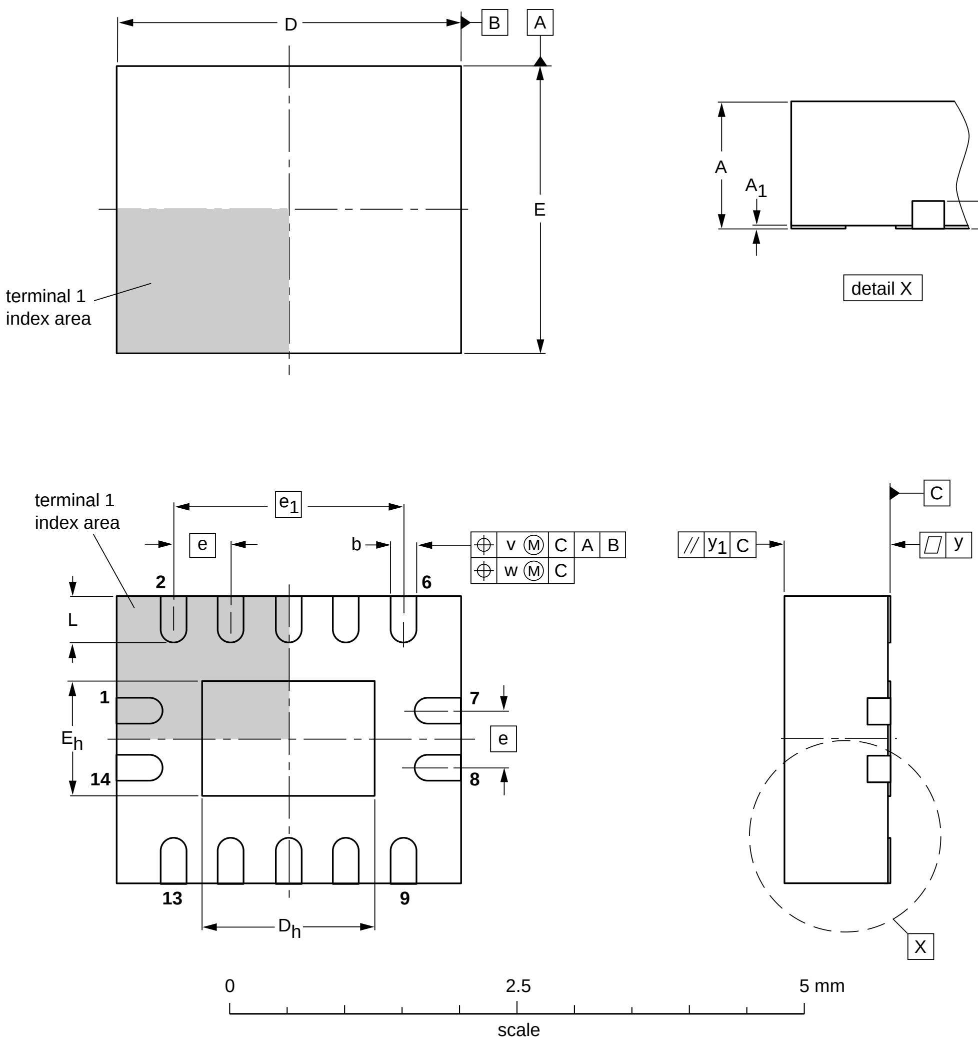
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 21. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 22. Package outline SOT762-1 (DHVQFN14)

14. Abbreviations

Table 14. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4066 v.7	20130402	Product data sheet	-	74HC_HCT4066 v.6
Modifications:	• Descriptive title corrected (errata). • New general description (errata).			
74HC_HCT4066 v.6	20120718	Product data sheet	-	74HC_HCT4066 v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT4066 v.5	20041111	Product data sheet	-	74HC_HCT4066 v.4
74HC_HCT4066 v.4	20030617	Product data sheet	-	74HC_HCT4066_CNV v.3
74HC_HCT4067_CNV v.3	19981110	Product data sheet	-	74HC_HCT4066_CNV v.2
74HC_HCT4066_CNV v.2	19981002	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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