14.2-Gbps Quad 1:2-2:1 MUX, Linear-Redriver With Signal Conditioning

Check for Samples: SN65LVCP114

FEATURES

- **Quad 2:1 Mux / 1:2 Demux**
- **Multi-Rate Operation up to 14.2 Gbps Serial Data Rate**
- **Linear Receiver Equalization Which Increases Margin at System Level of Decision Feedback Equalizer**
- **Bandwidth: 18 GHz, Typical**
- **Per-Lane P/N Pair Inversion**
- **Port or Single Lane Switching**
- **Low Power: 150 mW/Channel, Typical**
- **Loopback Mode on All Three Ports**
- **I²C Control in Addition to GPIO**
- **DIAG Mode That Outputs Data of Line Side Port to Both Fabric Side Ports**
- **2.5-V/3.3-V Single Power Supply**
- **PBGA Package 12-mm × 12-mm × 1-mm, 0.8-mm Terminal Pitch**
- **Excellent Impedance Matching to 100-Ω PCB Transmission Lines**
- **Small Package Size Provides Board Real Estate Saving**
- **Adjustable Output Swing Provides Flexible EMI and Crosstalk Control**
- **Low Power**
- **Supports 10GBASE-KR Applications With Ability to Transparency for Link Training**

APPLICATIONS

- **High-Speed Redundancy Switch in Telecom and Data Communication**
- **Backplane Interconnect for 10G-KR, 16GFC**

DESCRIPTION

The SN65LVCP114 is an asynchronous, protocol-agnostic, low-latency QUAD mux, linear-redriver optimized for use in systems operating at up to 14.2 Gbps. The device linearly compensates for channel loss in backplane and active-cable applications. The architecture of SN65LVCP114 linear-redriver is designed to work effectively with ASIC or FPGA products implementing digital equalization using decision feedback equalizer (DFE) technology. The SN65LVCP114 mux, linear-redriver preserves the integrity (composition) of the received signal, ensuring optimum DFE and system performance. The SN65LVCP114 provides a low-power mux-demux, linear-redriver solution while at the same time extending the effectiveness of DFE.

SN65LVCP114 is configurable via GPIO or an I²C interface.

A single 2.5-V or 3.3-V power supply supports the operation of the SN65LVCP114.

The SN65LVCP114 is packaged in a 12-mm × 12-mm × 1-mm PBGA package with 0.8-mm pitch.

The SN65LVCP114 has three ports; each port is a quad lane. The switch logic of SN65LVCP114 can be implemented to support a 2:1 MUX per lane, 1:2 DEMUX per lane, and independent lane switching. The receive equalization can be independently programmed for each of the ports. The SN65LVCP114 supports loopback on all three ports.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL IMPLEMENTATION

SN65LVCP114 can be implemented on the transmit side or the receive side of a backplane channel as shown in Figure 1.

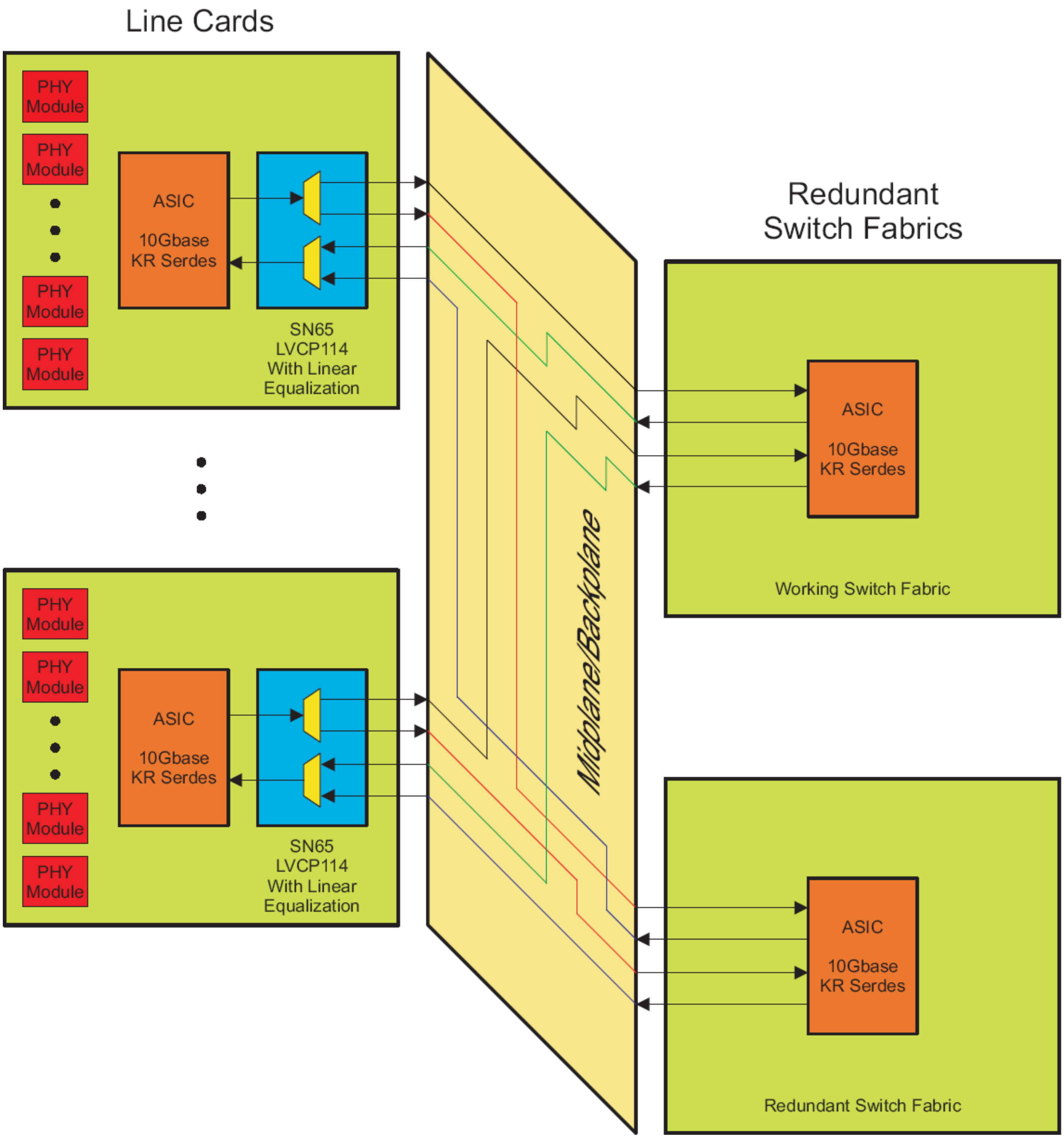

Figure 1. SN65LVCP114 Typical Implementation

BLOCK DIAGRAM

A simplified block diagram of the SN65LVCP114 is shown in Figure 2 for input quad channels AIN and BIN through the 2:1 MUX and output quad channel COUT, together with the input quad channel CIN through the 1:2 DEMUX through output quad channels AOUT and BOUT. The MUX and DEMUX channels contain a linear receive equalizer and an output linear driver.

The SN65LVCP114 provides both GPIO and I^{2}C interfaces to control the configuration of the device. A detailed description of the SN65LVCP114 pin functions is provided in .

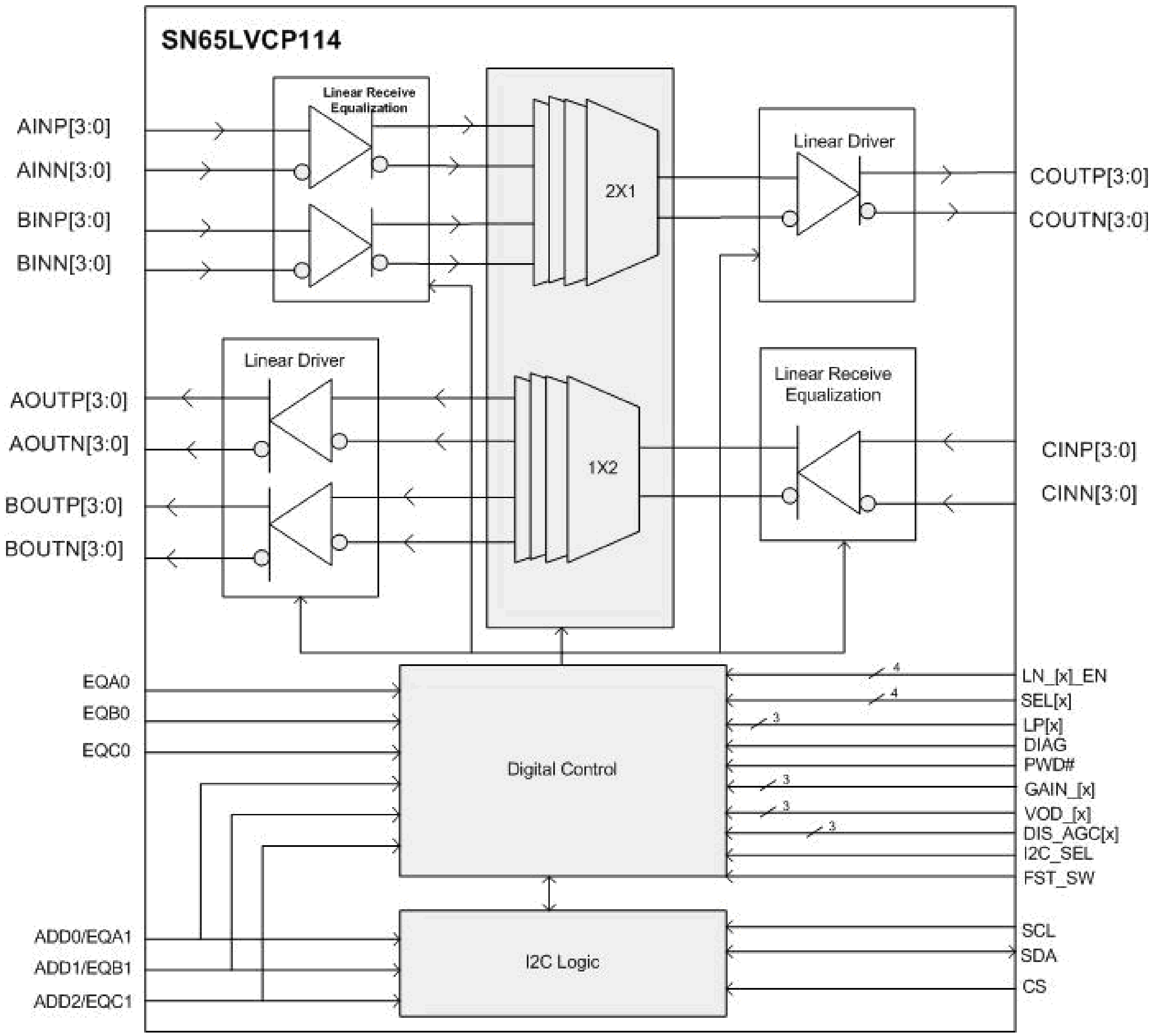

Figure 2. Simplified Block Diagram of SN65LVCP114

PACKAGE

The package for the SN65LVCP114 is a 12-mm × 12-mm × 1-mm, 167 pin PBGA with 0.8-mm pitch. The top view with the pin names is shown in Figure 3.

TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	ADD0/ EQA1	ADD1/ EQB1	EQC0	I2C_SEL	PWD#	AINP0	AINN0	GND	AINP1	AINN1	LN_2_EN	LPC	LPB	LPA	14
13	CINN0	VCC	CS	FST_SW	VCC	GND	VCC	VCC	GND	LN_1_EN	LN_3_EN	AOUTP2	VCC	REXT	13
12	CINP0	GND	COUTN0	GND	AOUTP0	AOUTN0	GND	AOUTP1	AOUTN1	LN_0_EN	DIAG	AOUTN2	GND	AINP2	12
11	GND	VCC	COUTP0									GND	VCC	AINN2	11
10	CINN1	VCC	GND		GND	GND	GND	GND	GND	GND		AOUTP3	VCC	GND	10
9	CINP1	GND	COUTN1		GND	GND	GND	GND	GND	GND		AOUTN3	GND	AINP3	9
8	GND	VCC	COUTP1		GND	GND	GND	GND	GND	GND		GND	GND	AINN3	8
7	CINN2	VCC	GND		GND	GND	GND	GND	GND	GND		BOUTP0	VCC	GND	7
6	CINP2	GND	COUTN2		GND	GND	GND	GND	GND	GND		BOUTN0	GND	BINP0	6
5	GND	VCC	COUTP2			GND	GND	GND	GND	GND		GND	VCC	BINN0	5
4	CINN3	VCC	GND									BOUTP1	VCC	GND	4
3	CINP3	GND	COUTN3	EQA0	GAIN_C	BOUTN3	BOUTP3	GND	BOUTN2	BOUTP2	GND	BOUTN1	GND	BINP1	3
2	SDA	SCL	COUTP3	GAIN_B	GAIN_A	GND	VCC	VCC	GND	VCC	VOD_C	VOD_B	VOD_A	BINN1	2
1	ADD2/ EQC1	DIS_AGC_A	DIS_AGC_B	DIS_AGC_C	BINN3	BINP3	GND	BINN2	BINP2	EQ_B0	SEL3	SEL2	SEL1	SEL0	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Figure 3. Package Pinout

PIN DESCRIPTIONS

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	BALLS		
LINE-SIDE HIGH-SPEED I/O			
CINP0 CINN0	A12 A13	Input (with 50-Ω termination to input common mode)	Differential input, lane 0 line side.
CINP1 CINN1	A9 A10	Input (with 50-Ω termination to input common mode)	Differential input, lane 1 line side
CINP2 CINN2	A6 A7	Input (with 50-Ω termination to input common mode)	Differential input, lane 2 line side
CINP3 CINN3	A3 A4	Input (with 50-Ω termination to input common mode)	Differential input, lane 3 line side
COUTP0 COUTN0	C11 C12	Output	Differential output, lane 0 line side
COUTP1 COUTN1	C8 C9	Output	Differential output, lane 1 line side
COUTP2 COUTN2	C5 C6	Output	Differential output, lane 2 line side
COUTP3 COUTN3	C2 C3	Output	Differential output, lane 3 line side

PIN DESCRIPTIONS (continued)

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	BALLS		
SWITCH-SIDE HIGH-SPEED I/O			
AINP0 AINN0	F14G14	Input (with 50-Ω termination to input common mode)	Differential input, lane 0, fabric switch_A_side
AINP1 AINN1	J14 K14	Input (with 50-Ω termination to input common mode)	Differential input, lane 1, fabric switch_A_side
AINP2 AINN2	P12 P11	Input (with 50-Ω termination to input common mode)	Differential input, lane 2, fabric switch_A_side
AINP3 AINN3	P9 P8	Input (with 50-Ω termination to input common mode)	Differential input, lane 3, fabric switch_A_side
BINP0 BINN0	P6 P5	Input (with 50-Ω termination to input common mode)	Differential input, lane 0, fabric switch_B_side
BINP1 BINN1	P3 P2	Input (with 50-Ω termination to input common mode)	Differential input, lane 1, fabric switch_B_side
BINP2 BINN2	J1 H1	Input (with 50-Ω termination to input common mode)	Differential input, lane 2, fabric switch_B_side
BINP3 BINN3	F1 E1	Input (with 50-Ω termination to input common mode)	Differential input, lane 3, fabric switch_B_side
AOUTP0 AOUTN0	E12 F12	Output	Differential output, lane 0, fabric switch_A_side
AOUTP1 AOUTN1	H12 J12	Output	Differential output, lane 1, fabric switch_A_side
AOUTP2 AOUTN2	M13 M12	Output	Differential output, lane 2, fabric switch_A_side
AOUTP3 AOUTN3	M10 M9	Output	Differential output, lane 3, fabric switch_A_side
BOUTP0 BOUTN0	M7 M6	Output	Differential output, lane 0, fabric switch_B_side
BOUTP1 BOUTN1	M4 M3	Output	Differential output, lane 1, fabric switch_B_side
BOUTP2 BOUTN2	K3 J3	Output	Differential output, lane 2, fabric switch_B_side
BOUTP3 BOUTN3	G3 F3	Output	Differential output, lane 3, fabric switch_B_side
CONTROL SIGNALS			
ADD0/EQA1 ADD1/EQB1 ADD2/EQC1	A14 B14 A1	Input, 2.5-V/3.3-V CMOS - 3-state	**GPIO mode** EQ control pins. EQA1 and EQA0 pins are 3-state and control the EQ gain of port A. EQ control pins. EQB1 and EQB0 pins are 3-state and control the EQ gain of port B. EQ control pins. EQC1 and EQC0 pins are 3-state and control the EQ gain of port C. **I^{2}C mode** ADD0 along with pins ADD1 and ADD2 comprise the three bits of the I^{2}C slave address.

EQ[x]0	EQ[x]0	Peaking in dB
0	0	1.3
0	HiZ	2
0	1	3.6
HiZ	0	5
HiZ	HiZ	6.5
HiZ	1	8.3
1	0	10
1	HiZ	11.9
1	1	13.9

PIN DESCRIPTIONS (continued)

<table>
<tr><th colspan="2">PIN</th><th rowspan="2">DIRECTION TYPE SUPPLY</th><th colspan="2" rowspan="2">DESCRIPTION</th></tr>
<tr><th>SIGNAL</th><th>BALLS</th></tr>
<tr><td>EQA0
EQB0
EQC0</td><td>D3
K1
C14</td><td>Input, 2.5-V/3.3-V CMOS - 3-state</td><td>GPIO mode
EQ control pins. EQA1 and EQA0 pins are 3-state and control theEQ gain of port A.
EQ control pins. EQB1 and EQB0 pins are 3-state and control theEQ gain of port B.
EQ control pins. EQC1 and EQC0 pins are 3-state and control theEQ gain of port C.
<table>
<tr><th>EQ[x]0</th><th>EQ[x]0</th><th>Peaking in dB</th></tr>
<tr><td>0</td><td>0</td><td>1.3</td></tr>
<tr><td>0</td><td>HiZ</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>3.6</td></tr>
<tr><td>HiZ</td><td>0</td><td>5</td></tr>
<tr><td>HiZ</td><td>HiZ</td><td>6.5</td></tr>
<tr><td>HiZ</td><td>1</td><td>8.3</td></tr>
<tr><td>1</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>HiZ</td><td>11.9</td></tr>
<tr><td>1</td><td>1</td><td>13.9</td></tr>
</table></td><td>I^{2}C mode
No action needed</td></tr>
<tr><td>LPA
LPB
LPC</td><td>P14
N14
M14</td><td>Input (with 48-kΩ pulldown)
2.5-V/3.3-V CMOS</td><td>GPIO mode
LPx enables loopback for port x
HIGH: Loopback enabled
LOW: Loopback disabled
See Table 2 and Figure 13 for device logic</td><td>I^{2}C mode
No action needed</td></tr>
<tr><td>SEL0
SEL1
SEL2
SEL3</td><td>P1
N1
M1
L1</td><td>Input (with 48-kΩ pulldown)
2.5-V/3.3-V CMOS</td><td>GPIO mode
SELx, A/B switch control for lane x
HIGH: port B is selected
LOW: port A is selected
See Table 2 and Figure 12 for device logic</td><td>I^{2}C mode
No action needed</td></tr>
<tr><td>REXT</td><td>P13</td><td>Input, analog</td><td colspan="2">External bias resistor, 1,200 Ω to ground</td></tr>
<tr><td>CS</td><td>C13</td><td>Input (with 48-kΩ pulldown)
2.5-V/3.3-V CMOS</td><td>GPIO mode
No action needed</td><td>I^{2}C mode
HIGH: acts as chip select
LOW: disables I^{2}C interface</td></tr>
<tr><td>$\overline{PWD}$</td><td>E14</td><td>Input (with 48-kΩ pullup)
2.5-V/3.3-V CMOS</td><td colspan="2">LOW: Powers down the device, inputs off and outputs disabled, resets I^{2}C
HIGH: Normal operation</td></tr>
<tr><td>DIAG</td><td>L12</td><td>Input (with 48-kΩ pulldown)
2.5-V/3.3-V CMOS</td><td>GPIO mode
HIGH: Enables the same data on the line side (Port C) to be output on both fabric side ports (Port A and Port B).
LOW: Normal operation
See Table 2 and Figure 12 for device logic.</td><td>I^{2}C mode
No action needed</td></tr>
<tr><td>LN_0_EN
LN_1_EN
LN_2_EN
LN_3_EN</td><td>K12
K13
L14
L13</td><td>Input (with 48-kΩ pullup)
2.5-V/3.3-V CMOS</td><td>GPIO mode
LN_x_EN = High, enables lane x of ports A, B, and C
LN_x_EN = Low, disables lane x of ports A, B, and C</td><td>I^{2}C mode
No action needed</td></tr>
<tr><td>DIS_AGC_A
DIS_AGC_B
DIS_AGC_C</td><td>B1
C1
D1</td><td>Input (with 48-kΩ pulldown)
2.5-V/3.3-V CMOS</td><td>GPIO mode
Disables the AGC loop internal to the SN65LVCP114
DIS_AGC = High, disables the AGC loop
DIS_AGC = Low, enables the AGC loop</td><td>I^{2}C mode
No action needed</td></tr>
<tr><td>VOD_A
VOD_B
VOD_C</td><td>N2
M2
L2</td><td>Input, 2.5-V/3.3-V CMOS - 3-state</td><td>GPIO mode
HIGH: selects VOD output range: 1.2 V maximum and a gain of 2.2
LOW: selects VOD output range: 600 mV maximum and a gain of 1.1
If left floating, it defaults to 1.2 V maximum and a gain of 2.2.</td><td>I^{2}C mode
No action needed</td></tr>
<tr><td>Gain_A
Gain_B
Gain_C</td><td>E2
D2
E3</td><td>Input, 2.5-V/3.3-V CMOS - 3-state</td><td>GPIO mode
HIGH: Receiver gain = 1
LOW: Receiver gain = 0.5
If left floating, it defaults to 0.5</td><td>I^{2}C mode
No action needed</td></tr>
<tr><td>SDA</td><td>A2</td><td>Input / output, open-drain output</td><td>GPIO mode
No action needed</td><td>I^{2}C mode
I^{2}C data. Connect a 10-kΩ pullup resistor externally</td></tr>
<tr><td>SCL</td><td>B2</td><td>Input, open-drain input</td><td>GPIO mode
No action needed</td><td>I^{2}C mode
I^{2}C clock. Connect a 10-kΩ pullup resistor externally</td></tr>
</table>

PIN DESCRIPTIONS (continued)

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION	
SIGNAL	BALLS			
FST_SW	D13	Input (with 48-kΩ pullup) 2.5-V/3.3-V CMOS input	**GPIO mode** HIGH: Fast switching; the idle outputs are squelched (see tSM specification). LOW: Slow switching; the idle outputs are powered off (see tSM1 specification).	**I^2C mode** No action needed
I2C_SEL	D14	Input (with 48-kΩ pulldown) 2.5-V/3.3-V CMOS input	Configures the device in I^2C or GPIO mode of operation HIGH: Enables I^2C mode LOW: Enables GPIO mode	
POWER SUPPLY				
VCC	B4, B5, B7, B8, B10, B11, B13, E13, G2, G13, H2, H13, K2,N4, N5, N7, N10, N11, N13	Power, 2.5 V ±5% / 3.3 V ±5%	Power supply pins	
GROUND				
GND	A5, A8, A11, B3, B6, B9, B12, C4, C7, C10,D12, F2, F13,G1, G12, G1, G12, H3, H14,J2, J13, L3, M5,M8, M11, N3, N6, N8, N9, N12, P4, P7, P10	Ground	Ground pins	
GND CenterPad	E6, E7 , E8, E9, E10, F5, F6, F7, F8, F9, F10, G5, G6, G7,G8, G9, G10, H5, H6, H7, H8, H9, H10, J5, J6, J7, J8, J9, J10, K5, K6, K7,K8, K9, K10	Ground	These pins must be connected to the GND plane.	

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

				VALUE / UNIT
V_{CC}	Supply voltage range (2)			–0.3 V to 4 V
$V_{IN,DIFF}$	Differential voltage between xINx_P and xINx_N			±2.5 V
$V_{IN+,\ IN–}$	Voltage at xINx_P and xINx_N			–0.5 V to VCC + 0.5 V
V_{IO}	Voltage on control I/O pins			–0.3 V to VCC + 0.5 V
I_{IN+} $I_{IN–}$	Continuous current at high-speed differential data inputs (differential)			–25 mA to 25 mA
I_{OUT+} $I_{OUT–}$	Continuous current at high-speed differential data outputs			–25 mA to 25 mA
ESD		Human-body model (3)	All pins	2 kV
		Charged-device model (4)	All pins	500 V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

THERMAL INFORMATION

THERMAL METRIC[1]		SN65LVCP114 ZJA (167 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	38.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	7.55	
θ_{JB}	Junction-to-board thermal resistance[4]	17.8	
ψ_{JT}	Junction-to-top characterization parameter[5]	0.2	
ψ_{JB}	Junction-to-board characterization parameter[6]	17.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

SPECIFICATION		MIN	NOM	MAX	UNIT
	Operating data rate, dR			14.2	Gbps
	Supply voltage, V_{CC}, 2.5-V nominal supply	2.375	2.5	2.625	V
	Supply voltage, V_{CC}, 3.3-V nominal supply	3.135	3.3	3.465	V
	PSNR BG, bandgap circuitry PSNR, 10 Hz–10 GHz	20			dB
CONTROL INPUTS					
V_{IH}	High-level input voltage	0.8 × V_{CC}			
V_{IM}	Mid-level input voltage	V_{CC}/2 – 0.3		V_{CC}/2 + 0.3	V
V_{IL}	Low- level input voltage			0.2 × V_{CC}	V
T_C	Junction temperature[1]	–10		125	°C
	Maximum Board Temperature[1]			See Table 1	°C

(1) Use of θJB and φJB are recommended for thermal calculations. For more information about traditional and new thermal metrics, see IC Package Thermal Metrics application report, SPRA953.

ELECTRICAL CHARACTERISTICS (V_{CC} 2.5 V ±5%)

over operating conditions range. All parameters are referenced to package pins (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER CONSUMPTION						
PD_L	Device power dissipation, loopback mode	Ports A, B, and C in loopback mode with all 12 channels active. VOD = LOW		1800	2300	mW
PD_N	Device power dissipation, normal mode	Device configured in mux-demux mode with 8 channels active. VOD = LOW		1400	1800	mW
PD_{OFF}	Device power dissipation, lanes disabled	All 4 lanes disabled. See the I^2C section for device configuration.		50		mW
PD_{STB}	Device power dissipation, standby	All 12 channels active, VOD = LOW, FAST_SW = HIGH. See the I^2C section for device configuration.		1800	2300	mW

ELECTRICAL CHARACTERISTICS (V_{CC} 3.3 V ±5%)

over operating conditions range. All parameters are referenced to package pins (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER CONSUMPTION						
PD_L	Device power dissipation, loopback mode	Ports A, B, and C in loopback mode with all 12 channels active. VOD = LOW		2500	3150	mW
PD_N	Device power dissipation, normal mode	Device configured in mux-demux mode with 8 channels active. VOD = LOW		1800	2500	mW
PD_{OFF}	Device power dissipation, lanes disabled	All 4 lanes disabled. See the I^2C section for device configuration.		50		mW
PD_{STB}	Device power dissipation, standby	All 12 channels active, VOD = LOW, FAST_SW = HIGH. See I^2C section for device configuration.		2500	3150	mW

ELECTRICAL CHARACTERISTICS (V_{CC} 3.3 V ±5%, 2.5 V ±5%)

over operating conditions range. All parameters are referenced to package pins (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
CMOS DC SPECIFICATIONS						
I_{IH}	High-level input current	V_{IN} = 0.9 × V_{CC}			80	µA
I_{IL}	Low-level input current	V_{IN} = 0.1 × V_{CC}	-80			µA
CML INPUTS (AINP[3:0], AINN[3:0], BINP[3:0], BINN[3:0], CINP[3:0], CINN[3:0])						
r_{IN}	Differential input resistance	INx_P to INx_N		100		Ω
V_{INPP}	Input linear dynamic range	Gain = 0.5		1200		mVpp
V_{ICM}	Common-mode input voltage	Internally biased		V_{CC} – 0.3		V
SCD11	Input differential to common-mode conversion	100 MHz to 7.1GHz		–25		dB
SDD11	Differential input return loss	100 MHz to 7.1GHz		–10		dB
CML OUTPUTS (AOUTP[3:0], AOUTN[3:0], BOUTP[3:0], BOUTN[3:0], COUTP[3:0], COUTN[3:0])						
V_{OD}	Output linear dynamic range	R_L = 100 Ω, V_{OD} = High		1200		mV_{PP}
		R_L = 100 Ω, V_{OD} = Low		600		
V_{OS}	Output offset voltage	R_L = 100 Ω, 0 V applied at inputs			20	mV_{PP}
$V_{CM,RIP}$	Common-mode output ripple	K28.5 pattern at 14.2 Gbps, no interconnect loss, V_{OD} = HIGH		10	20	mV_{RMS}
$V_{OD,RIP}$	Differential path output ripple	K28.5 pattern at 14.2Gbps, no interconnect loss, V_{IN} = 1200 mVpp. Outputs squelched.			20	mV_{PP}
V_{OCM}	Output common mode voltage	See Figure 4		V_{CC} – 0.35		V
$V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			±10		mV
t_{PLH}	Low-to-high propagation delay	See Figure 5		200		ps
t_{PHL}	High-to-low propagation delay			200		ps
$t_{SK(O)}$	Inter-pair output skew (2)	All outputs terminated with 100 Ω. See Figure 7		50		ps

(1) All typical values are at 25°C and with 2.5-V and 3.3-V supply, unless otherwise noted.
(2) $t_{SK(O)}$ is the magnitude of the time difference between the channels within a Port. For more information, see SN65LVCP114 Guidelines for Skew Compensation, SLLA323.

ELECTRICAL CHARACTERISTICS (V_{CC} 3.3 V ±5%, 2.5 V ±5%) (continued)

over operating conditions range. All parameters are referenced to package pins (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{SK(PP)}$	Part-to-part skew(3)				100	ps
t_R	Rise time	Input signal with 30ps rise time, 20% to 80%. See Figure 6		31		ps
t_F	Fall time	Input signal with 30ps fall time, 20% to 80%. See Figure 6		31		ps
SDD22	Differential output return loss	100 MHz to 7.1GHz		–10		dB
SCC22	Common-mode output return loss	100 MHz to 7.1GHz		–5		dB
t_{SM}	Multiplexer switch time	Mux to valid output (idle outputs are squelched)		100		ns
t_{SM1}		Mux to valid output (idle outputs are turned off)		10		µs
Ch_{iso}	Channel-to-channel isolation(4)	Frequency at 5.1625 GHz		52.2		dB
		Frequency at 7.1GHz		43.5		
OUT_{NOISE}	Output referred noise	10 MHz to 7.1 GHz. No other noise source present. V_{OD} = LOW			1500	μV_{RMS}
		10 MHz to 7.1 GHz. No other noise source present. V_{OD} = HIGH			3000	
Vpre	Output pre-cursor pre-emphasis	Input signal with 3.75 pre-cursor and measured on the output signal. See Figure 8. Vpre = 20 log(V3/V2)		5		dB
Vpst	Output post-cursor pre-emphasis	Input signal with 12 dB post-cursor and measure it on the output signal. See Figure 8. Vpst = 20 log(V1/V2)		14		dB
r_{OT}	Single-ended output resistance	Single-ended on-chip terminations to VCC, outputs are ac-coupled		50		Ω
r_{OM}	Output termination mismatch at 1 MHz	$\Delta rom = 2 \times \frac{rp - rn}{rp + rn} \times 100$			5	%
EQUALIZATION						
EQ_{Gain}	At 7.1 GHz input signal	Equalization gain, EQ = MAX	10	15		dB
DJ1	TX residual deterministic jitter at 10.3125 Gbps	Tx launch amplitude = 0.6Vpp, EQ=1.3dB, VOD and GAIN are High. Test Channel = 0". See Figure 10.		0.08		UIp-p
DJ2	TX residual deterministic jitter at 14.2 Gbps	Tx launch Amplitude = 0.6 Vpp, EQ=1.3dB, VOD and GAIN are High. Test Channel = 0". See Figure 10.		0.06		UIp-p
DJ3	RX residual deterministic jitter at 10.3125 Gbps	Tx Launch Amplitude = 0.6 Vpp, test channel = 12" (9dB loss at 5GHz), EQ=13.9dB, VOD and GAIN are High. See Figure 9.		0.04		UIp-p
DJ4	RX residual deterministic Jitter at 14.2 Gbps	Tx Launch Amplitude = 0.6 Vpp, test channel = 8" (9dB loss at 7GHz), EQ=13.9dB, VOD=LOW and GAIN=HIGH. See Figure 9.		0.08		UIp-p

(3) $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) All noise sources added.

Table 1. RECOMMENDED MAXIMUM BOARD TEMPERATURE

LOOP_A	LOOP_B	LOOP_C	DIAG	Maximun Board Temperature [(1)]			
				V_{CC} = 2.5V		V_{CC} = 3.3V	
				V_{OD} = LOW	V_{OD} = HIGH	V_{OD} = LOW	V_{OD} = HIGH
LOW	LOW	LOW	LOW	85°C	85°C	85°C	75°C
LOW	LOW	LOW	HIGH	85°C	85°C	75°C	System Specific [(2)]
LOW	LOW	HIGH	LOW	85°C	85°C	85°C	75°C
LOW	LOW	HIGH	HIGH	85°C	85°C	85°C	75°C
LOW	HIGH	LOW	LOW	85°C	85°C	75°C	System Specific [(2)]
LOW	HIGH	LOW	HIGH	85°C	85°C	75°C	System Specific [(2)]
LOW	HIGH	HIGH	LOW	85°C	85°C	75°C	System Specific [(2)]
LOW	HIGH	HIGH	HIGH	85°C	85°C	75°C	System Specific [(2)]
HIGH	LOW	LOW	LOW	85°C	85°C	85°C	75°C
HIGH	LOW	LOW	HIGH	85°C	85°C	75°C	System Specific [(2)]
HIGH	LOW	HIGH	LOW	85°C	85°C	85°C	75°C
HIGH	LOW	HIGH	HIGH	85°C	85°C	75°C	System Specific [(2)]
HIGH	HIGH	LOW	LOW	85°C	85°C	75°C	System Specific [(2)]
HIGH	HIGH	LOW	HIGH	85°C	85°C	75°C	System Specific [(2)]
HIGH	HIGH	HIGH	LOW	85°C	85°C	75°C	System Specific [(2)]
HIGH	HIGH	HIGH	HIGH	85°C	85°C	75°C	System Specific [(2)]

(1) Maximum board temperature is allowed as long as the device maximum junction temperature is not exceeded.
(2) Texas Instruments recommends a system thermal and device use case power analysis to decide possible use of a heat sink.

PARAMETER MEASUREMENT INFORMATION

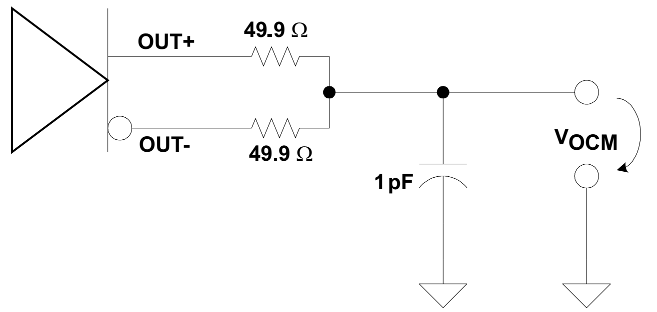

Figure 4. Common-Mode Output-Voltage Test Circuit

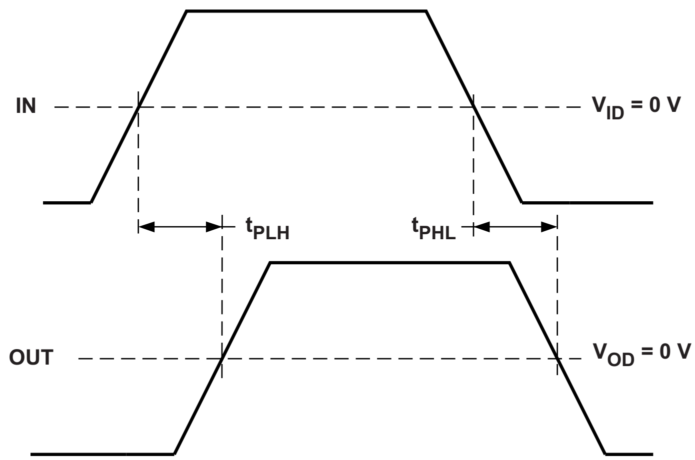

Figure 5. Propagation Delay, Input to Output

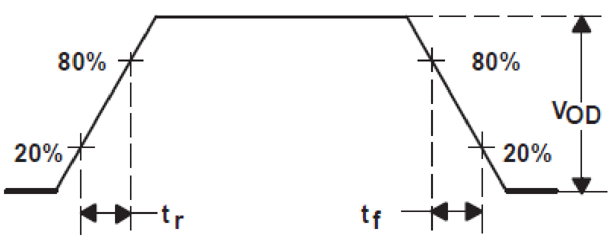

Figure 6. Output Rise and Fall Times

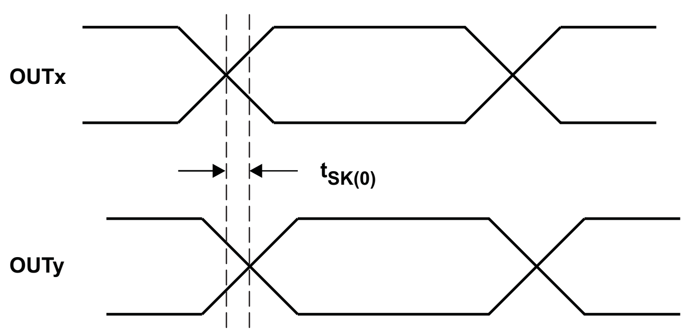

Figure 7. Output Inter-Pair Skew

PARAMETER MEASUREMENT INFORMATION (continued)

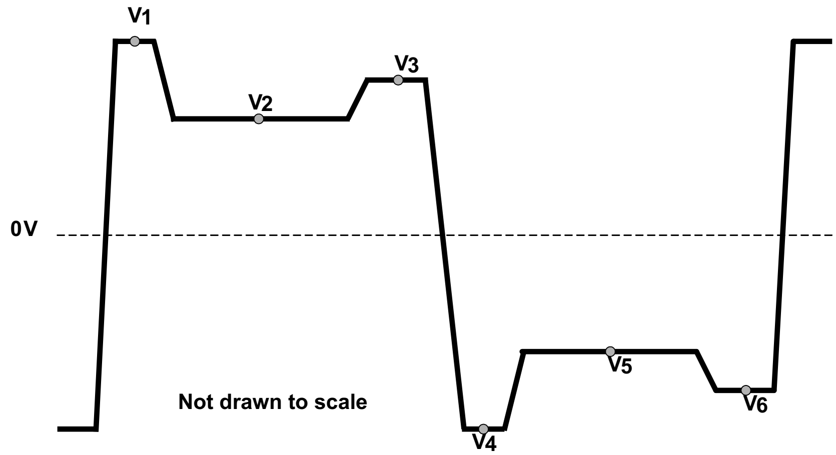

Figure 8. Vpre and Vpost [The Test Pattern is 1111111100000000 (Eight 1s, Eight 0s)]

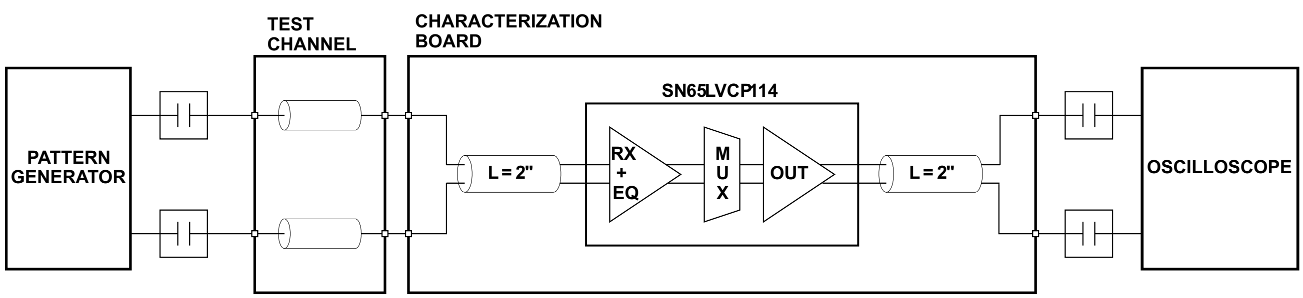

Figure 9. Receive-Side Performance Test Circuit

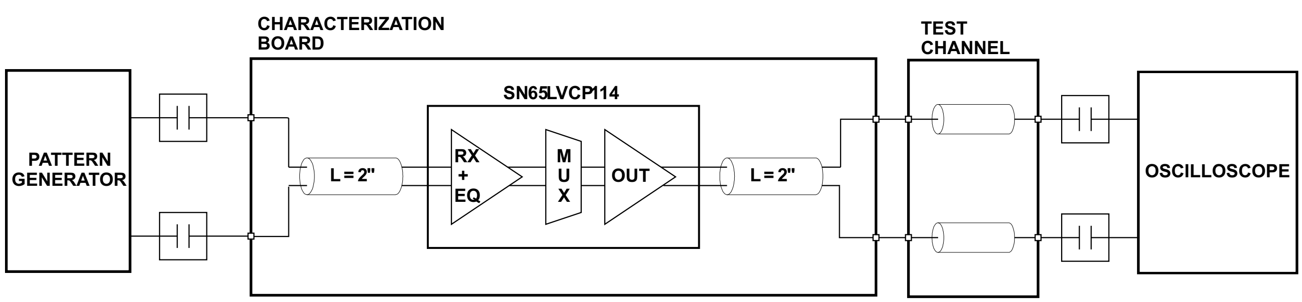

Figure 10. Transmit-Side Performance Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

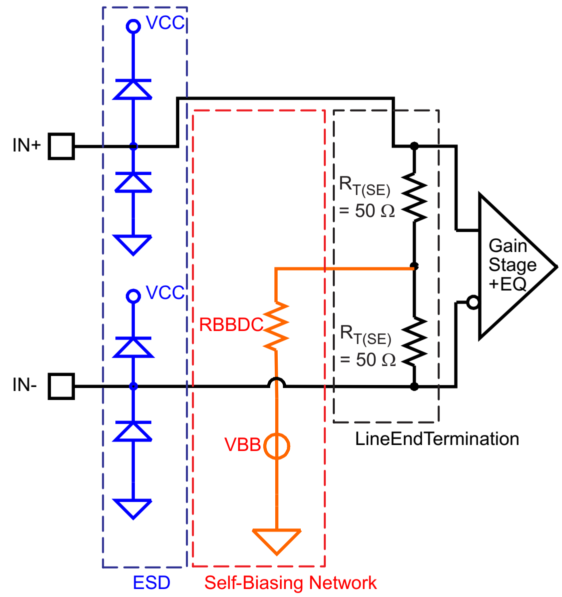

Figure 11. Equivalent Input Circuit Design

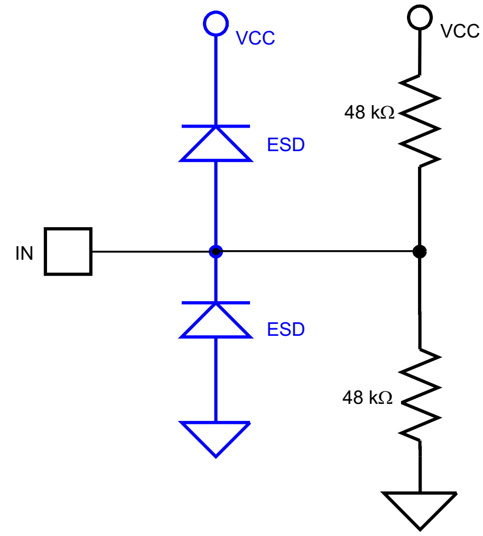

Figure 12. 3-Level Input Biasing Network

FUNCTIONAL DEFINITIONS

Table 2. Loopback, DIAG, and SEL Controls

Loop_A	Loop_B	Loop_C	DIAG	SEL[3:0]	Output Port A	Output Port B	Output Port C
0	0	0	0	0	In_Port_C[3:0]	idle	In_Port_A[3:0]
0	0	0	0	1	idle	In_Port_C[3:0]	In_Port_B[3:0]
0	0	0	1	0	In_Port_C[3:0]	In_Port_C[3:0]	In_Port_A[3:0]
0	0	0	1	1	In_Port_C[3:0]	In_Port_C[3:0]	In_Port_B[3:0]
0	0	1	0	0	In_Port_C[3:0]	Idle	In_Port_C[3:0]
0	0	1	0	1	Idle	In_Port_C[3:0]	In_Port_C[3:0]
0	0	1	1	0	In_Port_C[3:0]	In_Port_C[3:0]	In_Port_C[3:0]
0	0	1	1	1	In_Port_C[3:0]	In_Port_C[3:0]	In_Port_C[3:0]
0	1	0	0	0	In_Port_C[3:0]	In_Port_B[3:0]	In_Port_A[3:0]
0	1	0	0	1	Idle	In_Port_B[3:0]	In_Port_B[3:0]
0	1	0	1	0	In_Port_C[3:0]	In_Port_B[3:0]	In_Port_A[3:0]
0	1	0	1	1	In_Port_C[3:0]	In_Port_B[3:0]	In_Port_B[3:0]
0	1	1	0	0	In_Port_C[3:0]	In_Port_B[3:0]	In_Port_C[3:0]
0	1	1	0	1	Idle	In_Port_B[3:0]	In_Port_C[3:0]
0	1	1	1	0	In_Port_C[3:0]	In_Port_B[3:0]	In_Port_C[3:0]
0	1	1	1	1	In_Port_C[3:0]	In_Port_B[3:0]	In_Port_C[3:0]
1	0	0	0	0	In_Port_A[3:0]	Idle	In_Port_A[3:0]
1	0	0	0	1	In_Port_A[3:0]	In_Port_C[3:0]	In_Port_B[3:0]
1	0	0	1	0	In_Port_A[3:0]	In_Port_C[3:0]	In_Port_A[3:0]
1	0	0	1	1	In_Port_A[3:0]	In_Port_C[3:0]	In_Port_B[3:0]
1	0	1	0	0	In_Port_A[3:0]	Idle	In_Port_C[3:0]
1	0	1	0	1	In_Port_A[3:0]	In_Port_C[3:0]	In_Port_C[3:0]
1	0	1	1	0	In_Port_A[3:0]	In_Port_C[3:0]	In_Port_C[3:0]
1	0	1	1	1	In_Port_A[3:0]	In_Port_C[3:0]	In_Port_C[3:0]

PARAMETER MEASUREMENT INFORMATION (continued)

Table 2. Loopback, DIAG, and SEL Controls (continued)

Loop_A	Loop_B	Loop_C	DIAG	SEL[3:0]	Output Port A	Output Port B	Output Port C
1	1	0	0	0	In_Port_A[3:0]	In_Port_B[3:0]	In_Port_A[3:0]
1	1	0	0	1	In_Port_A[3:0]	In_Port_B[3:0]	In_Port_B[3:0]
1	1	0	1	0	In_Port_A[3:0]	In_Port_B[3:0]	In_Port_A[3:0]
1	1	0	1	1	In_Port_A[3:0]	In_Port_B[3:0]	In_Port_B[3:0]
1	1	1	0	0	In_Port_A[3:0]	In_Port_B[3:0]	In_Port_C[3:0]

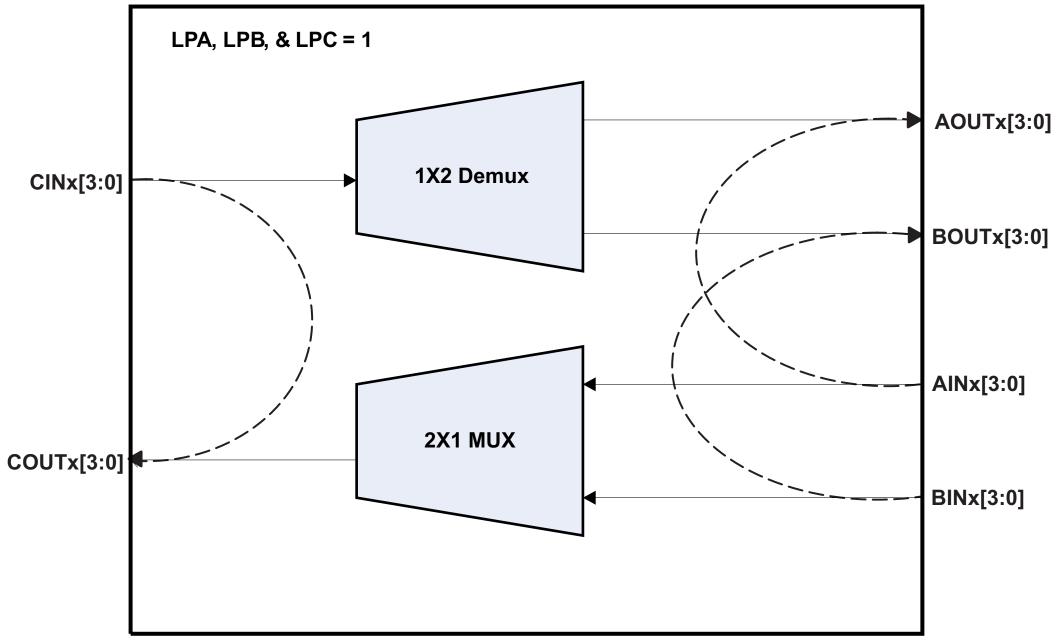

Figure 13. Loopback Mode

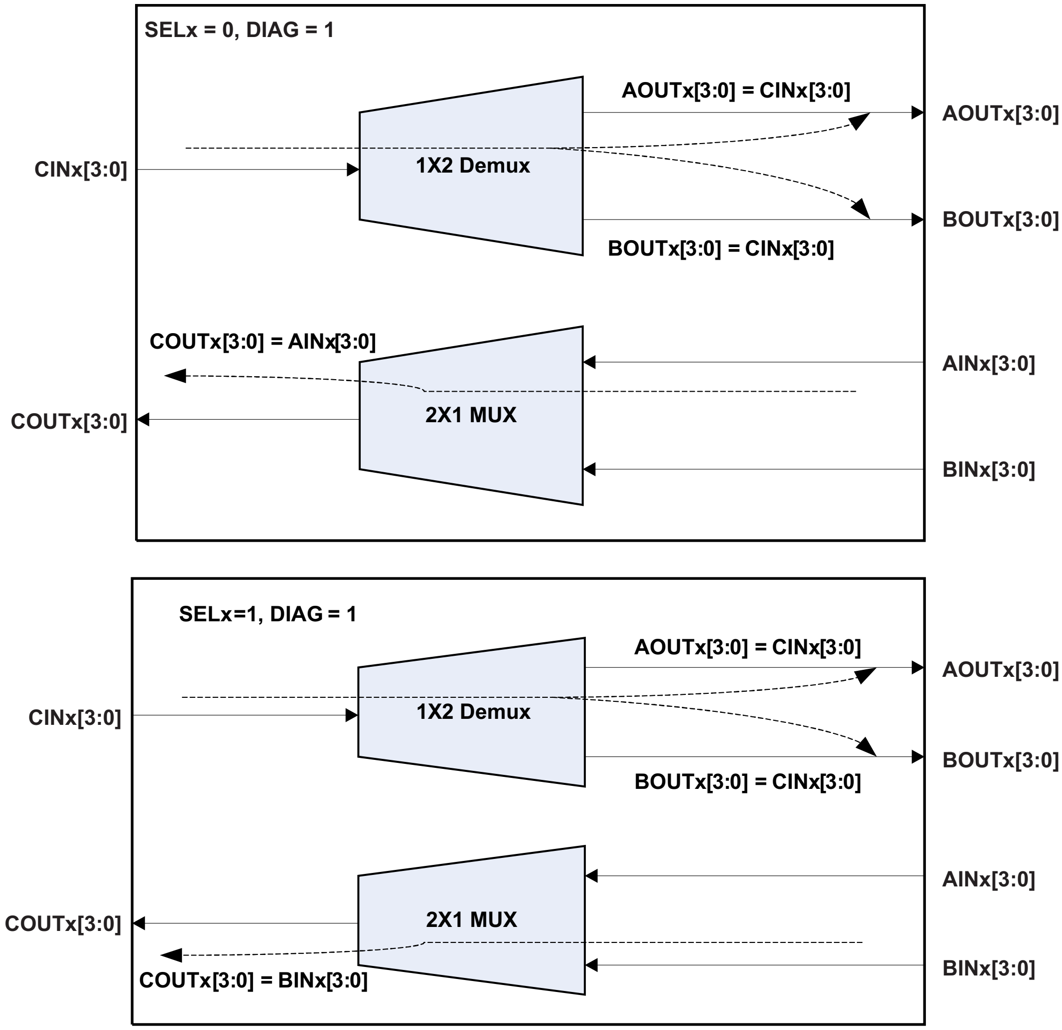

Figure 14. Diagnostic Mode

Table 3. Overall Gain Settings

Gain_x	Input Gain [dB]	VOD_x	VOD Gain [dB]	EQ[x]0	EQ[x]1	Total DC gain [dB]	Total EQ gain (7 GHz) [dB]
LOW	–6	LOW	1	LOW	LOW	–5	1.3
LOW	–6	LOW	1	LOW	HiZ	–5	2
LOW	–6	LOW	1	LOW	HIGH	–5	3.6
LOW	–6	LOW	1	HiZ	LOW	–8	5
LOW	–6	LOW	1	HiZ	HiZ	–8	6.5
LOW	–6	LOW	1	HiZ	HIGH	–8	8.3
LOW	–6	LOW	1	HIGH	LOW	–11	10
LOW	–6	LOW	1	HIGH	HiZ	–11	11.9
LOW	–6	LOW	1	HIGH	HIGH	–11	13.9
LOW	–6	HIGH	6.8	LOW	LOW	0.8	1.3
LOW	–6	HIGH	6.8	LOW	HiZ	0.8	2
LOW	–6	HIGH	6.8	LOW	HIGH	0.8	3.6
LOW	–6	HIGH	6.8	HiZ	LOW	–2.2	5
LOW	–6	HIGH	6.8	HiZ	HiZ	–2.2	6.5
LOW	–6	HIGH	6.8	HiZ	HIGH	–2.2	8.3
LOW	–6	HIGH	6.8	HIGH	LOW	–5.2	10
LOW	–6	HIGH	6.8	HIGH	HiZ	–5.2	11.9
LOW	–6	HIGH	6.8	HIGH	HIGH	–5.2	13.9
HIGH	0	LOW	1	LOW	LOW	1	1.3
HIGH	0	LOW	1	LOW	HiZ	1	2
HIGH	0	LOW	1	LOW	HIGH	1	3.6
HIGH	0	LOW	1	HiZ	LOW	–2	5
HIGH	0	LOW	1	HiZ	HiZ	–2	6.5
HIGH	0	LOW	1	HiZ	HIGH	–2	8.3
HIGH	0	LOW	1	HIGH	LOW	–5	10
HIGH	0	LOW	1	HIGH	HiZ	–5	11.9
HIGH	0	LOW	1	HIGH	HIGH	–5	13.9
HIGH	0	HIGH	6.8	LOW	LOW	6.8	1.3
HIGH	0	HIGH	6.8	LOW	HiZ	6.8	2
HIGH	0	HIGH	6.8	LOW	HIGH	6.8	3.6
HIGH	0	HIGH	6.8	HiZ	LOW	3.8	5
HIGH	0	HIGH	6.8	HiZ	HiZ	3.8	6.5
HIGH	0	HIGH	6.8	HiZ	HIGH	3.8	8.3
HIGH	0	HIGH	6.8	HIGH	LOW	0.8	10
HIGH	0	HIGH	6.8	HIGH	HiZ	0.8	11.9
HIGH	0	HIGH	6.8	HIGH	HIGH	0.8	13.9

TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 2.5 V and T_A = 25°C, no interconnect line at the output, and with default device settings (unless otherwise noted).

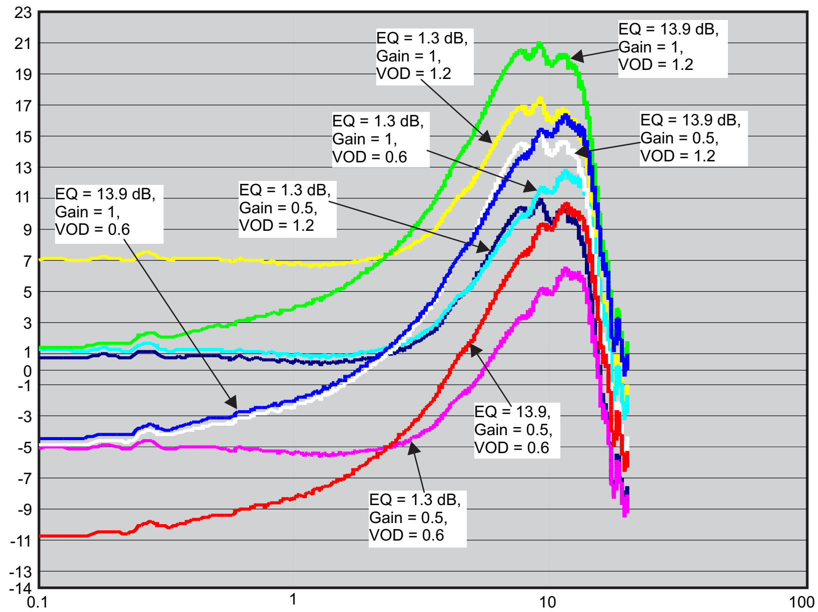

Figure 15. Typical EQ Gain Profile Curve

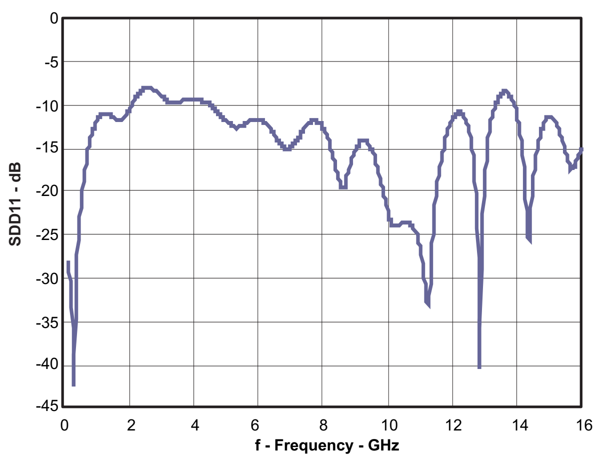

Figure 16. Differential Input Return Loss

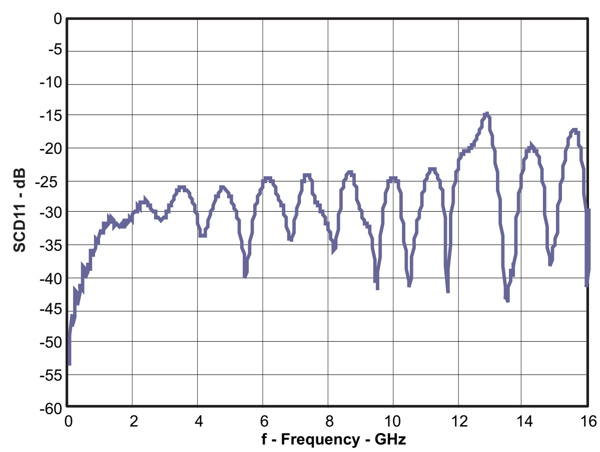

Figure 17. Differential to Common-Mode Conversion

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 2.5 V and T_A = 25°C, no interconnect line at the output, and with default device settings (unless otherwise noted).

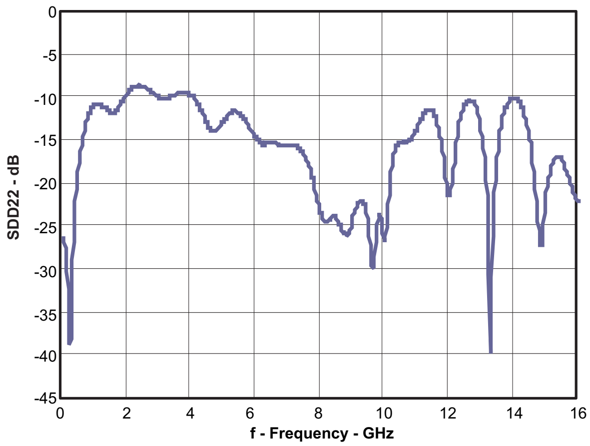

Figure 18. Differential Output Return Loss

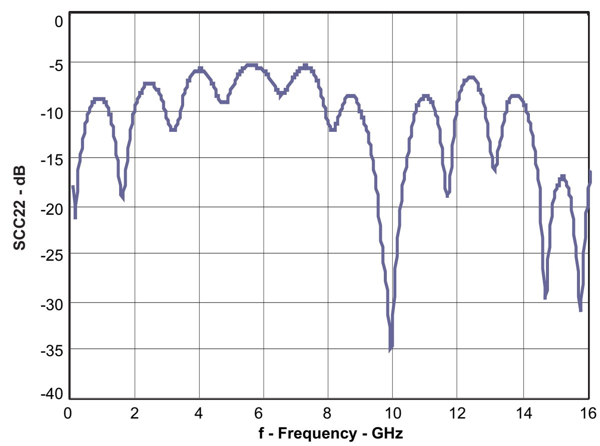

Figure 19. Common-Mode Output Return Loss

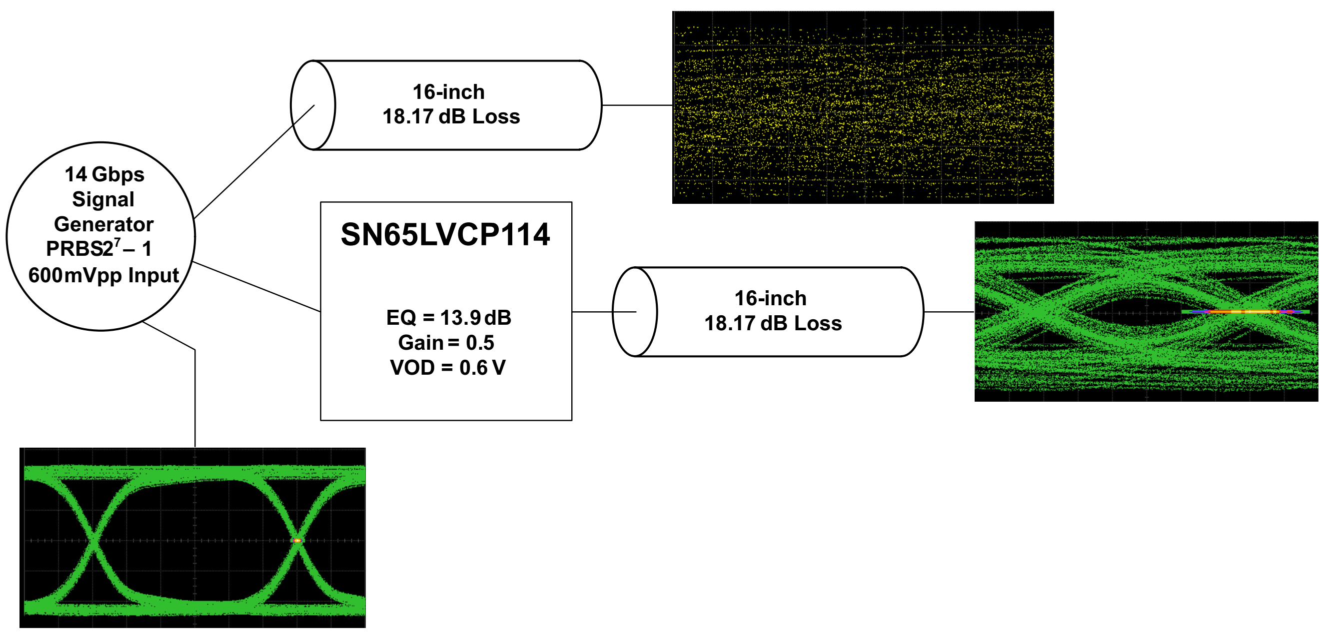

Figure 20. Transmit-Side Typical Application

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 2.5 V and T_A = 25°C, no interconnect line at the output, and with default device settings (unless otherwise noted).

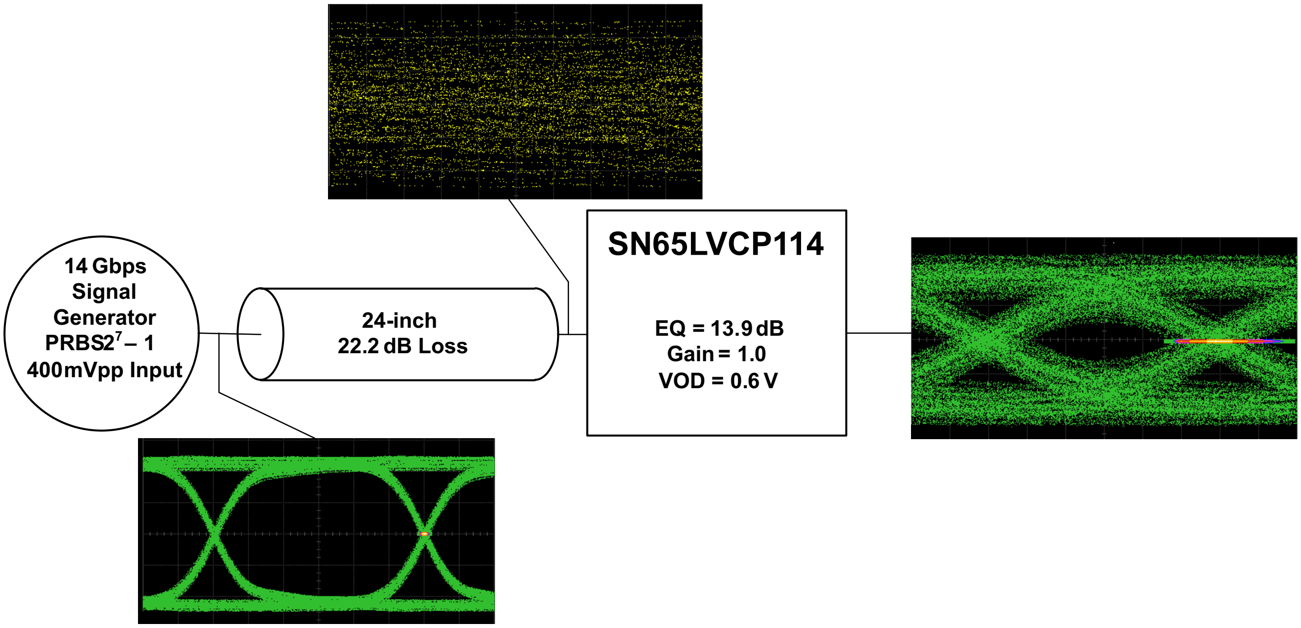

Figure 21. Receive-Side Typical Application

APPLICATION INFORMATION

TWO-WIRE SERIAL INTERFACE AND CONTROL LOGIC

The SN65LVCP114 uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCL, are driven, respectively, by the serial data and serial clock from a microprocessor, for example. The SDA and SCL pins require external 10-kΩ pullups to V_{CC}.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out the control signals. The SN65LVCP114 is a slave device only, which means that it cannot initiate a transmission itself; it always relies on the availability of the SCL signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7-bit slave address (0000ADD[2:0]) followed by an 8th bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ. The ADD[2:0] address bits change with the status of the ADD2, ADD1, and ADD0 device pins, respectively. If the pins are left floating or pulled down, the 7-bit slave address is 0000000.
3. 8-bit register address
4. 8-bit register data word
5. STOP command

Regarding timing, the SN65LVCP114 is I^2C compatible. The typical timing is shown in Figure 22, and a complete data transfer is shown in Figure 23. Parameters for Figure 22 are defined in Table 4.

Bus Idle: Both SDA and SCL lines remain HIGH

Start data transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still must communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line, and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver does not acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

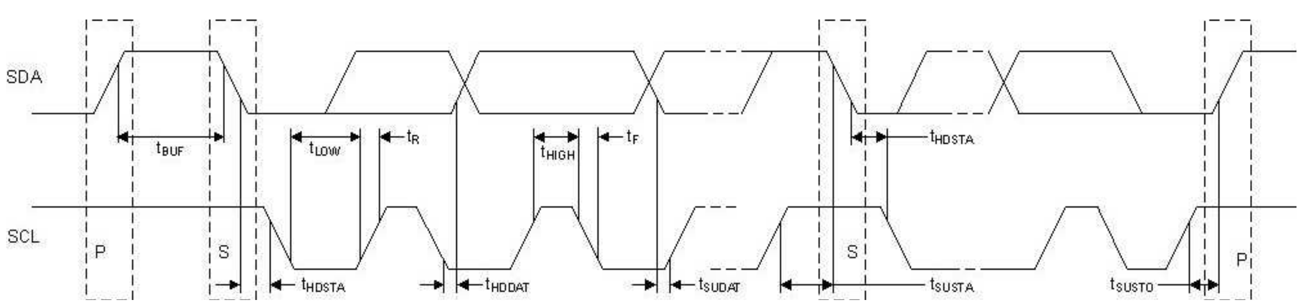

Figure 22. Two-Wire Serial Interface Timing Diagram

Table 4. Two-Wire Serial Interface Timing Diagram Definitions

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency		400	kHz
t_{BUF}	Bus free time between START and STOP conditions	1.3		μs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated.	0.6		μs
t_{LOW}	Low period of the SCL clock	1.3		μs
t_{HIGH}	High period of the SCL clock	0.6		μs
t_{SUSTA}	Setup time for a repeated START condition	0.6		μs
t_{HDDAT}	Data hold time	0		μs
t_{SUDAT}	Data setup time	100		ns
t_R	Rise time of both SDA and SCL signals		300	ns
t_F	Fall time of both SDA and SCL signals		300	ns
t_{SUSTO}	Setup time for STOP condition	0.6		μs

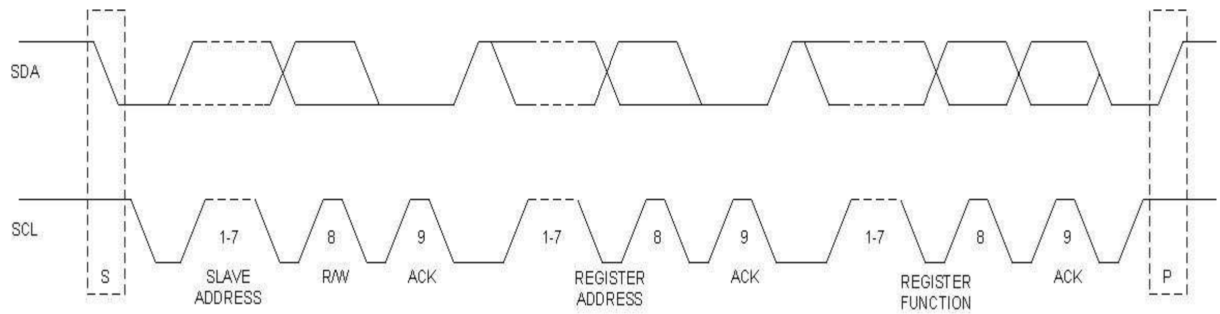

Figure 23. Two-wire Serial Interface Data Transfer

SN65LVCP114 Register Mapping Information

Register 0x00 (General Device Settings) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SW_GPIO	PWRDOWN						RSVD

Register 0x01 (Device Control Settings) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DIAG	LOOP[C]	LOOP[B]	LOOP[A]	SEL[3]	SEL[2]	SEL[1]	SEL[0]

Register 0x02 (Port A Control Settings) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
OUT_DIS_0	OUT_DIS_1	OUT_DIS_2	OUT_DIS_3	FAST_SW	RSVD		DIS_AGC

Register 0x03 (Port A Input Settings) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
INOFF	RSVD	RSVD	RSVD	EQ3	EQ2	EQ1	EQ0

Register 0x04 (Port A Output Settings) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		VOD1	VOD0			GAIN1	GAIN0

Register 0x06 (Port B Control Settings) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
OUT_DIS_0	OUT_DIS_1	OUT_DIS_2	OUT_DIS_3	FAST_SW	RSVD		DIS_AGC

Register 0x07 (Port B Input Settings) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
INOFF	RSVD	RSVD	RSVD	EQ3	EQ2	EQ1	EQ0

Register 0x08 (Port B Output Settings) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		VOD1	VOD0			GAIN1	GAIN0

Register 0x0A (Port C Control Settings) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
OUT_DIS_0	OUT_DIS_1	OUT_DIS_2	OUT_DIS_3	FAST_SW	RSVD		DIS_AGC

Register 0x0B (Port C Input Settings) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
INOFF	RSVD	RSVD	RSVD	EQ3	EQ2	EQ1	EQ0

Register 0x0C (Port C Output Settings) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		VOD1	VOD0			GAIN1	GAIN0

Register 0x0D (Reserved Settings) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Register 0x0F (Reserved Settings) Read Only							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Register 0x10 (Polarity Control Settings for Port A and B) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
POL_B[3]	POL_B[2]	POL_B[1]	POL_B[0]	POL_A[3]	POL_A[2]	POL_A[1]	POL_A[0]

Register 0x11 (Polarity Control Settings for Port C) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
				POL_C[3]	POL_C[2]	POL_C[1]	POL_C[0]

Register 0x12 (Lane Enable) R/W							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
				LN_EN[3]	LN_EN[2]	LN_EN[1]	LN_EN[0]

Table 5. SN65LVCP114 Register Descriptions

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x00	7	SW_GPIO	Switching logic is controlled by GPIO or I^{2}C: 1 = GPIO control 0 = I^{2}C control	00000000
	6	PWRDOWN	Power down the device: 0 = Normal operation 1 = Power down	
	5			
	4			
	3			
	2			
	1			
	0	RSVD	For TI use only	
0x01	7	DIAG	Enables Diag Mode: 0 = Disable 1 = Enable	00000000
	6	LOOP[C]	Enables port C loopback: 0 = Disable 1 = Enable	
	5	LOOP[B]	Enables port B loopback: 0 = Disable 1 = Enable	
	4	LOOP[A]	Enables port A loopback: 0 = Disable 1 = Enable	
	3	SEL[3]	Lane 3, port A/port B switch control: 0 = Port A selected 1 = Port B selected	
	2	SEL[2]	Lane 2, port A/port B switch control: 0 = Port A selected 1 = Port B selected	
	1	SEL[1]	Lane 1, port A/port B switch control: 0 = Port A selected 1 = Port B selected	
	0	SEL[0]	Lane 0, port A/port B switch control: 0 = Port A selected 1 = Port B selected	

Table 5. SN65LVCP114 Register Descriptions (continued)

<table>
<tr><th>REGISTER</th><th>BIT</th><th>SYMBOL</th><th>FUNCTION</th><th>DEFAULT</th></tr>
<tr><td rowspan="8">0x02
0x06
0x0A</td><td>7</td><td>OUT_DIS0</td><td>Disables output lane 0:
0 = Enable
1 = Disable</td><td rowspan="8">00001100</td></tr>
<tr><td>6</td><td>OUT_DIS1</td><td>Disables output lane 1:
0 = Enable
1 = Disable</td></tr>
<tr><td>5</td><td>OUT_DIS2</td><td>Disables output lane 2:
0 = Enable
1 = Disable</td></tr>
<tr><td>4</td><td>OUT_DIS3</td><td>Disables output lane 3:
0 = Enable
1 = Disable</td></tr>
<tr><td>3</td><td>FAST_SW</td><td>Fast switch:
0 = Idle outputs are disabled (save power)
1 = Idle outputs are squelched (fast switch time)</td></tr>
<tr><td>2</td><td>RSVD</td><td>For TI use only</td></tr>
<tr><td>1</td><td></td><td></td></tr>
<tr><td>0</td><td>DIS_AGC</td><td>AGC loop:
0 = Enable
1 = Disable</td></tr>
<tr><td rowspan="8">0x03
0x07
0x0B</td><td>7</td><td>IN_OFF</td><td>Power down input stages:
0 = Normal
1 = Power down</td><td rowspan="8">00000000</td></tr>
<tr><td>6</td><td>RSVD</td><td>For TI use only</td></tr>
<tr><td>5</td><td>RSVD</td><td>For TI use only</td></tr>
<tr><td>4</td><td>RSVD</td><td>For TI use only</td></tr>
<tr><td>3</td><td>EQ3</td><td rowspan="4"><table><tr><th>EQ3</th><th>EQ2</th><th>EQ1</th><th>EQ0</th><th>Peaking in dB</th></tr><tr><td>0</td><td>x</td><td>x</td><td>x</td><td>1.3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>2</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>3.6</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>6.5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>8.3</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>10</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>11.9</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>13.9</td></tr></table></td></tr>
<tr><td>2</td><td>EQ2</td></tr>
<tr><td>1</td><td>EQ1</td></tr>
<tr><td>0</td><td>EQ0</td></tr>
<tr><td rowspan="8">0x04
0x08
0x0C</td><td>7</td><td></td><td></td><td rowspan="8">00000000</td></tr>
<tr><td>6</td><td></td><td></td></tr>
<tr><td>5</td><td>VOD1</td><td rowspan="2">VOD control [VOD1:VOD0]:
00 = 1200 mV maximum
01 = 600 mV maximum
10 = 1200 mV maximum
11 = 1200 mV maximum</td></tr>
<tr><td>4</td><td>VOD0</td></tr>
<tr><td>3</td><td></td><td></td></tr>
<tr><td>2</td><td></td><td></td></tr>
<tr><td>1</td><td>GAIN1</td><td rowspan="2">GAIN control [GAIN1:GAIN0]:
00 = 0.5
01 = 1
10 = 0.5
11 = 1</td></tr>
<tr><td>0</td><td>GAIN0</td></tr>
</table>

Table 5. SN65LVCP114 Register Descriptions (continued)

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x05 0x09 0x0E	7			00000000
	6			
	5			
	4			
	3			
	2			
	1			
	0			
0x0D	7	RSVD	For TI use only	00000000
	6	RSVD	For TI use only	
	5	RSVD	For TI use only	
	4	RSVD	For TI use only	
	3	RSVD	For TI use only	
	2	RSVD	For TI use only	
	1	RSVD	For TI use only	
	0	RSVD	For TI use only	
0x0F	7	RSVD	For TI use only	00010001
	6	RSVD	For TI use only	
	5	RSVD	For TI use only	
	4	RSVD	For TI use only	
	3	RSVD	For TI use only	
	2	RSVD	For TI use only	
	1	RSVD	For TI use only	
	0	RSVD	For TI use only	
0x10	7	POL_B[3]	Polarity switch of output lane 3 of port B: 0 = Normal 1 = Switched	00000000
	6	POL_B[2]	Polarity switch of output lane 2 of port B: 0 = Normal 1 = Switched	
	5	POL_B[1]	Polarity switch of output lane 1 of port B: 0 = Normal 1 = Switched	
	4	POL_B[0]	Polarity switch of output lane 0 of port B 0 = Normal 1 = Switched	
	3	POL_A[3]	Polarity switch of output lane 3 of port A: 0 = Normal 1 = Switched	
	2	POL_A[2]	Polarity switch of output lane 2 of port A: 0 = Normal 1 = Switched	
	1	POL_A[1]	Polarity switch of output lane 1 of port A: 0 = Normal 1 = Switched	
	0	POL_A[0]	Polarity switch of output lane 0 of port A: 0 = Normal 1 = Switched	

Table 5. SN65LVCP114 Register Descriptions (continued)

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x11	7			00000000
	6			
	5			
	4			
	3	POL_C[3]	Polarity switch of output lane 3 of port C: 0 = Normal 1 = Switched	
	2	POL_C[2]	Polarity switch of output lane 2 of port C: 0 = Normal 1 = Switched	
	1	POL_C[1]	Polarity switch of output lane 1 of port C: 0 = Normal 1 = Switched	
	0	POL_C[0]	Polarity switch of output lane 0 of port C: 0 = Normal 1 = Switched	
0x12	7			00001111
	6			
	5			
	4			
	3	LN_EN_3	Lane 3 of ports A, B, and C: 0 = Disable 1 = Enable	
	2	LN_EN_2	Lane 2 of ports A, B, and C: 0 = Disable 1 = Enable	
	1	LN_EN_1	Lane 1 of ports A, B, and C: 0 = Disable 1 = Enable	
	0	LN_EN_0	Lane 0 of ports A, B, and C: 0 = Disable 1 = Enable	

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
SN65LVCP114ZJA	ACTIVE	NFBGA	ZJA	167	189	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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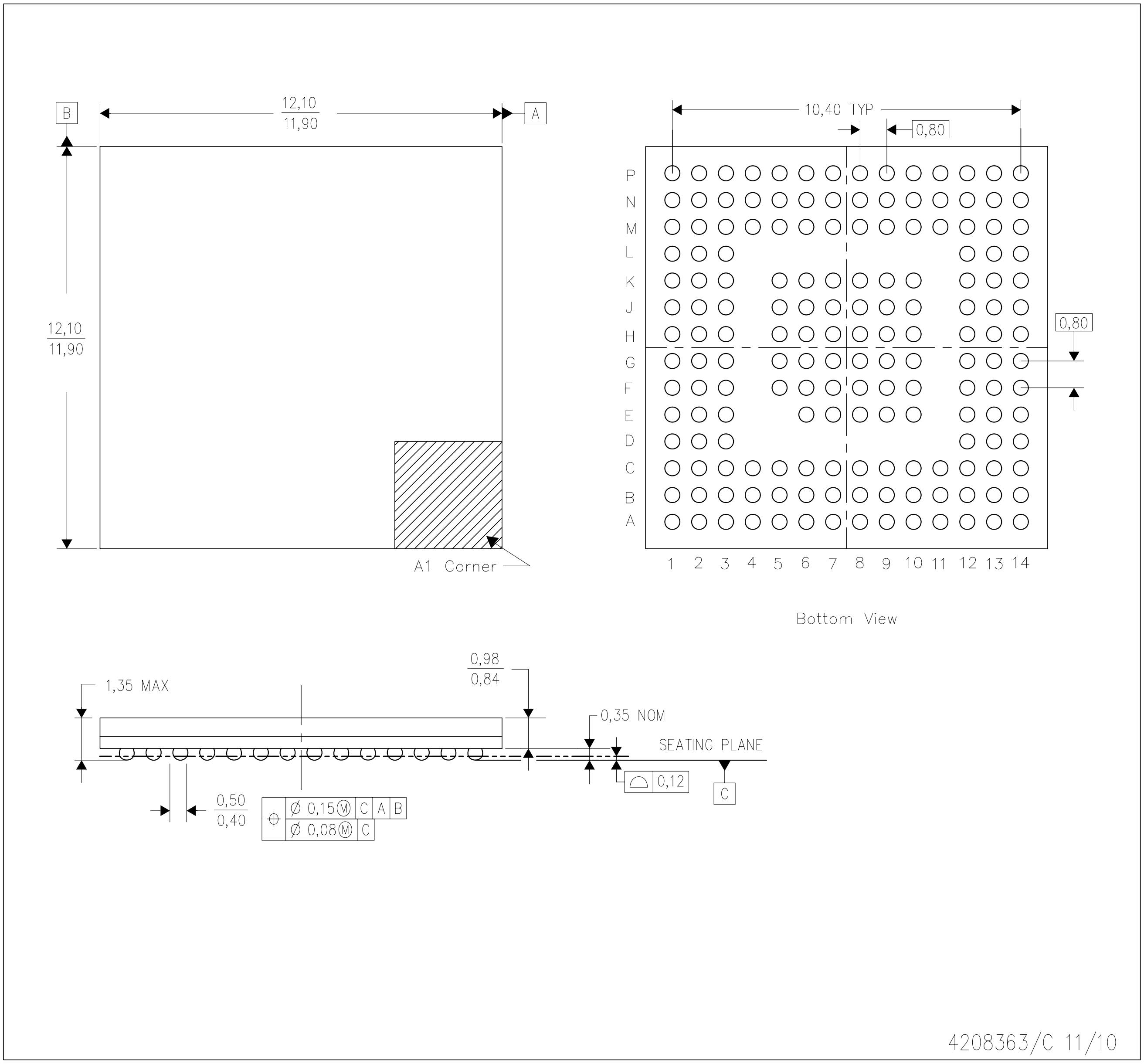
ZJA (S-PBGA-N167) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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