



# FDS8447

## Single N-Channel PowerTrench® MOSFET

40V, 12.8A, 10.5mΩ

### Features

- Max  $r_{DS(on)}$  = 10.5mΩ at  $V_{GS} = 10V$ ,  $I_D = 12.8A$
- Max  $r_{DS(on)}$  = 12.3mΩ at  $V_{GS} = 4.5V$ ,  $I_D = 11.4A$
- Low gate charge
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability
- RoHS compliant

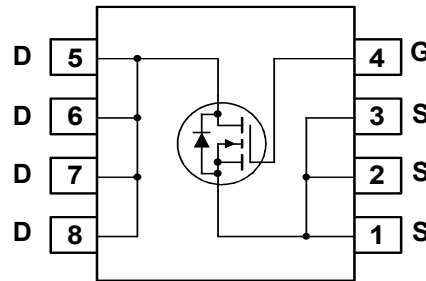
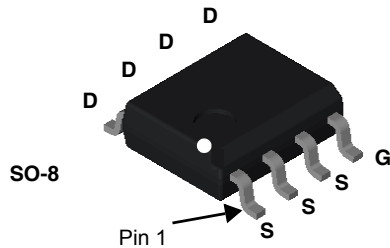


### General Description

This single N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Applications

- DC - DC conversion



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	40	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Note 1a)	12.8	A
	-Pulsed	50	
$E_{AS}$	Drain-Source Avalanche Energy (Note 3)	150	mJ
$P_D$	Power Dissipation for Single Operation (Note 1a)	2.5	W
	(Note 1b)	1	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance-Single operation, Junction to Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	25	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS8447	FDS8447	13"	12mm	2500 units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		34		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{V}, V_{GS} = 0\text{V}$ $T_J = 55^\circ\text{C}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

**On Characteristics (Note 2)**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-5		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 12.8\text{A}$		9	10.5	m $\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 11.4\text{A}$		10	12.3	
		$V_{GS} = 10\text{V}, I_D = 12.8\text{A}, T_J = 125^\circ\text{C}$		13	15	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 12.8\text{A}$		75.3		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$		2000	2600	pF
$C_{oss}$	Output Capacitance			250	350	pF
$C_{rss}$	Reverse Transfer Capacitance			150	250	pF
$R_g$	Gate Resistance		$f = 1\text{MHz}$	1.3		$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{V}, I_D = 12.8\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 4.5\Omega$		11	20	ns
$t_r$	Rise Time			14	25	ns
$t_{d(off)}$	Turn-Off Delay Time			27	42	ns
$t_f$	Fall Time			7	14	ns
$Q_g$	Total Gate Charge at $V_{GS} = 10\text{V}$	$V_{DS} = 20\text{V}, I_D = 12.8\text{A},$		35	49	nC
$Q_g$	Total Gate Charge at $V_{GS} = 5\text{V}$			19	27	nC
$Q_{gs}$	Gate to Source Gate Charge			6		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			7		nC

**Drain-Source Diode Characteristics and Maximum Ratings**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 12.8\text{A}$ (note 2)		0.84	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 12.8\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$		19	29	ns
$Q_{rr}$	Reverse Recovery Charge			9.5	19	nC

**Notes:**

1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a)  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper

Scale 1:1 on letter size paper



b)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

2: Pulse Test: Pulse Width < 300 us, Duty Cycle < 2.0%.

3: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{mH}$ ,  $I_{AS} = 10\text{A}$ ,  $V_{DD} = 40\text{V}$ ,  $V_{GS} = 10\text{V}$ .

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

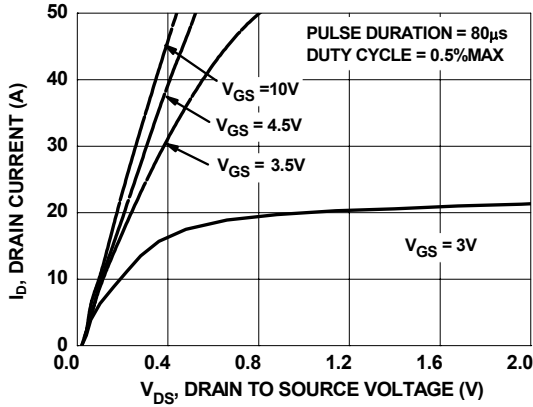


Figure 1. On Region Characteristics

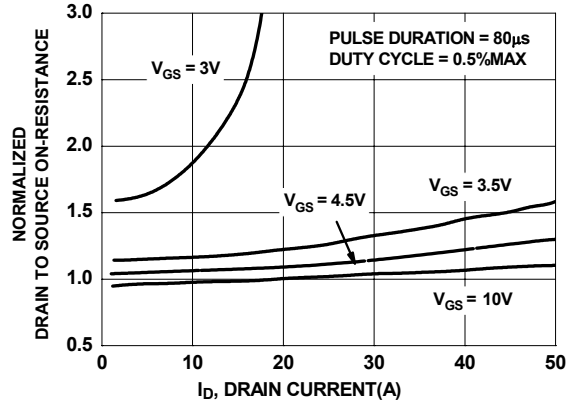


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

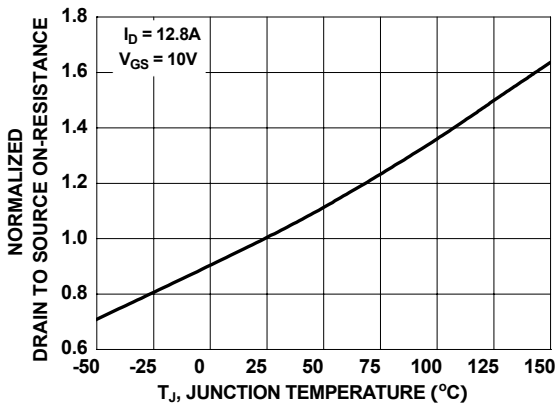


Figure 3. Normalized On Resistance vs Junction Temperature

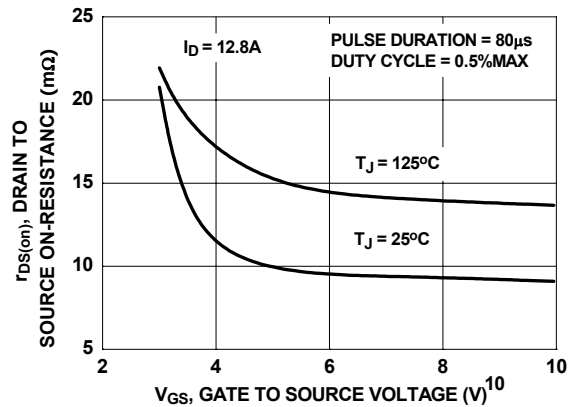


Figure 4. On-Resistance vs Gate to Source Voltage

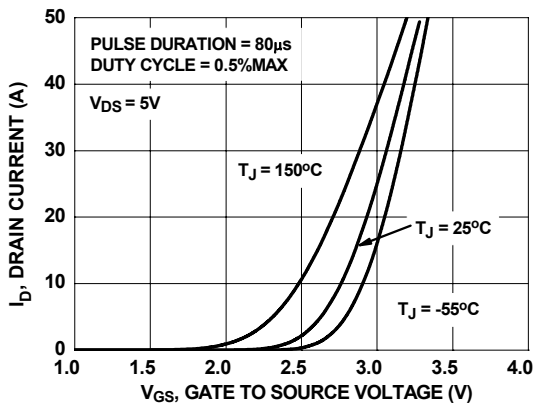


Figure 5. Transfer Characteristics

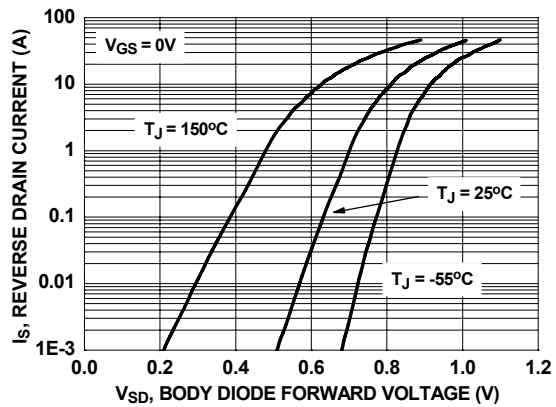


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

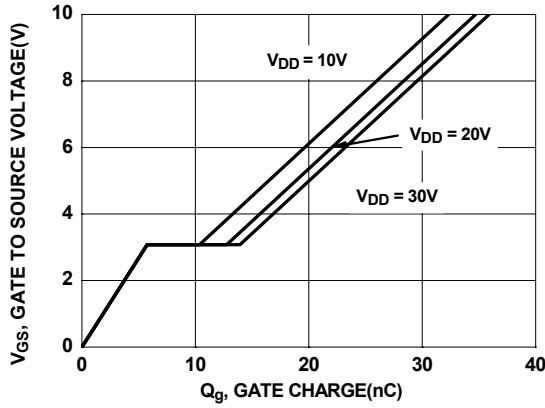


Figure 7. Gate Charge Characteristics

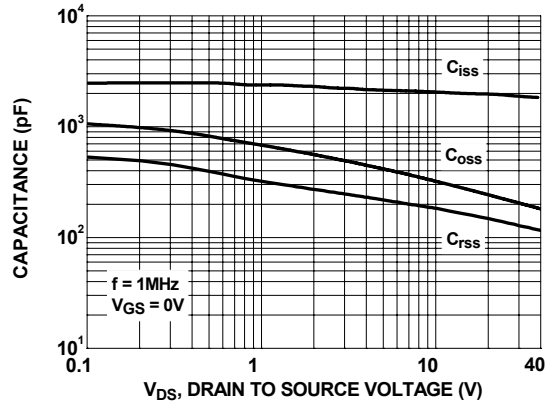


Figure 8. Capacitance vs Drain to Source Voltage

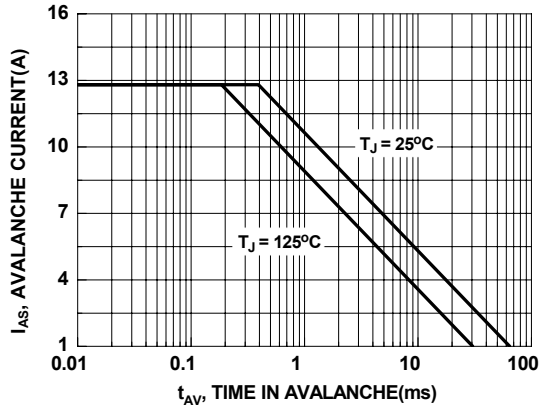


Figure 9. Unclamped Inductive Switching Capability

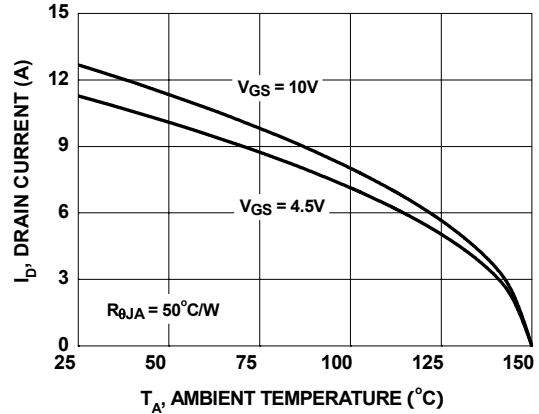


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

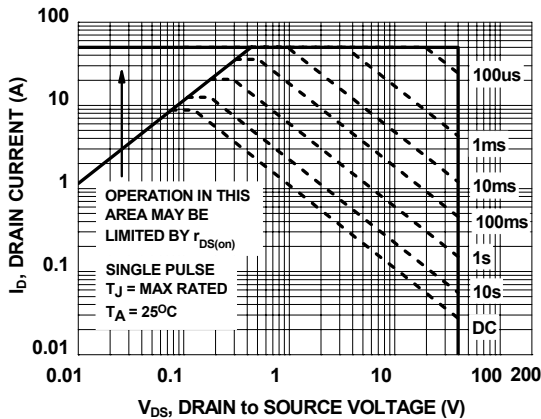


Figure 11. Forward Bias Safe Operating Area

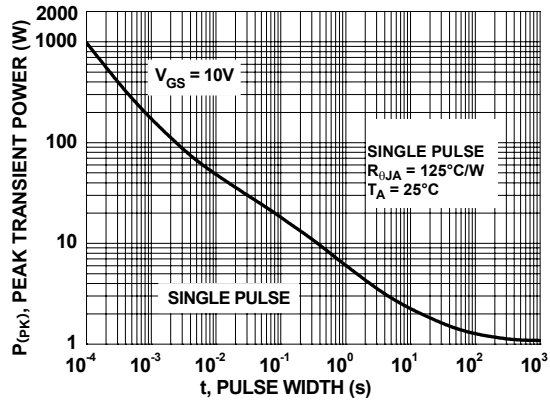
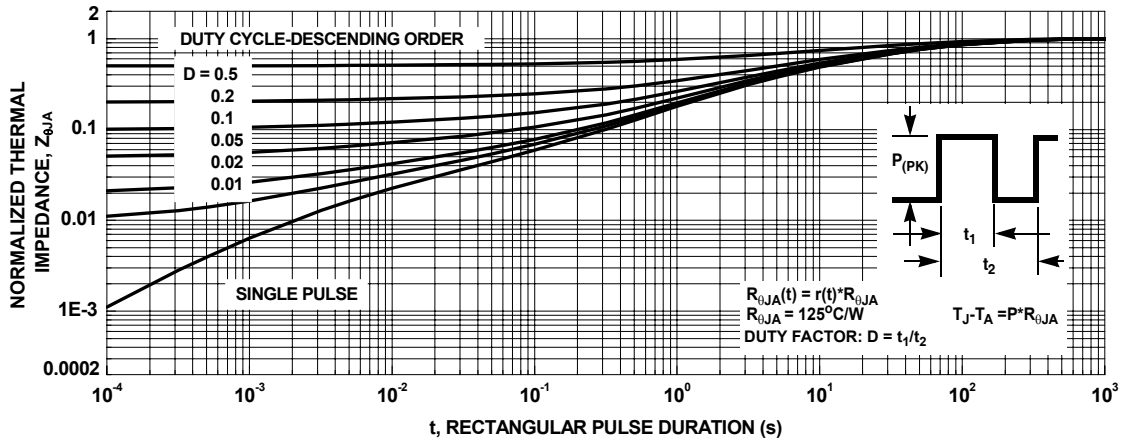


Figure 12. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Transient Thermal Response Curve**

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