



BT149G

SCR

13 March 2014

Product data sheet

1. General description

Planar passivated Silicon Controlled Rectifier with sensitive gate in a SOT54 (TO-92) plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic ICs and other low power gate trigger circuits.

2. Features and benefits

- Enhanced voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate
- Direct triggering from low power drivers and logic ICs

3. Applications

- General purpose switching and phase control

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
V_{RRM}	repetitive peak reverse voltage		-	-	600	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	-	8	A
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83\text{ }^{\circ}\text{C}$; Fig. 1	-	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 83\text{ }^{\circ}\text{C}$; Fig. 2 ; Fig. 3	-	-	0.8	A
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	50	200	μA

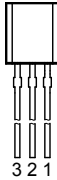


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 TO-92 (SOT54)	 sym037
2	G	gate		
3	A	anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT149G	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
V_{RRM}	repetitive peak reverse voltage		-	600	V
$I_{\text{T(AV)}}$	average on-state current	half sine wave; $T_{\text{lead}} \leq 83^\circ\text{C}$; Fig. 1	-	0.5	A
$I_{\text{T(RMS)}}$	RMS on-state current	half sine wave; $T_{\text{lead}} \leq 83^\circ\text{C}$; Fig. 2 ; Fig. 3	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{\text{j(init)}} = 25^\circ\text{C}$; $t_{\text{p}} = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	8	A
		half sine wave; $T_{\text{j(init)}} = 25^\circ\text{C}$; $t_{\text{p}} = 8.3\text{ ms}$	-	9	A
I^2t	I^2t for fusing	$t_{\text{p}} = 10\text{ ms}$; SIN	-	0.32	A^2s
di_{T}/dt	rate of rise of on-state current	$I_{\text{T}} = 2\text{ A}$; $I_{\text{G}} = 10\text{ mA}$; $di_{\text{G}}/dt = 100\text{ mA}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	1	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	2	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	$^\circ\text{C}$
T_{j}	junction temperature		-	125	$^\circ\text{C}$

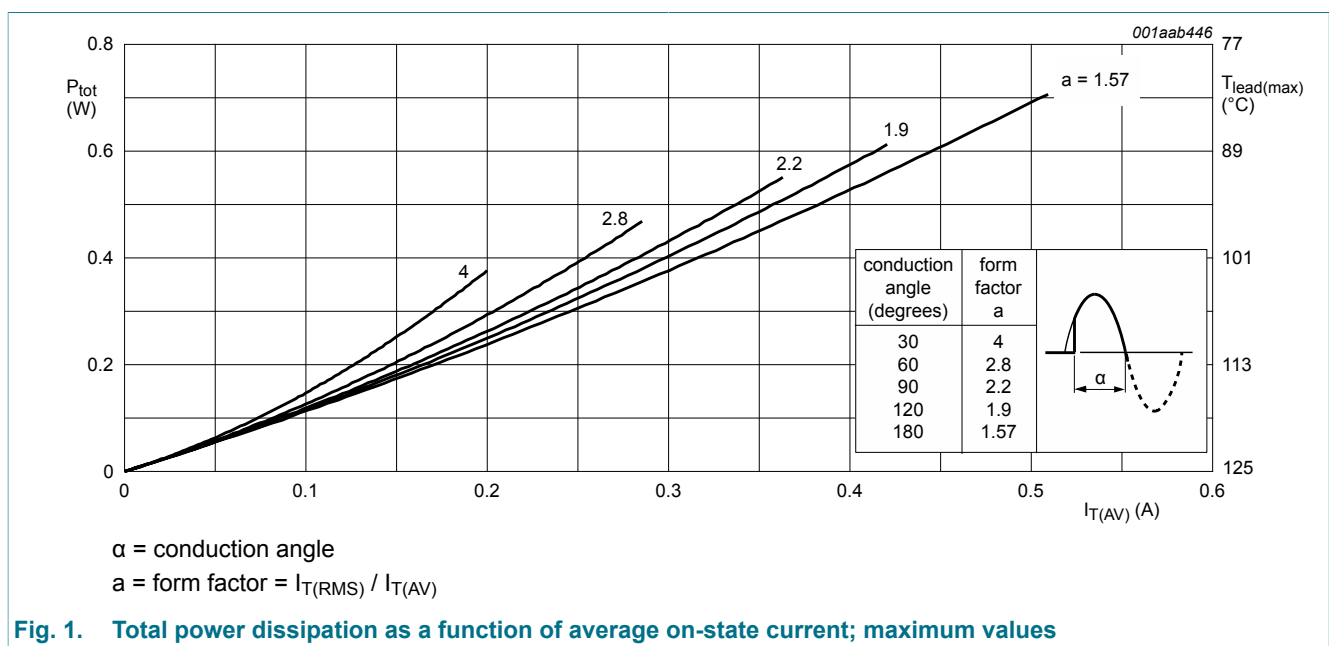


Fig. 1. Total power dissipation as a function of average on-state current; maximum values

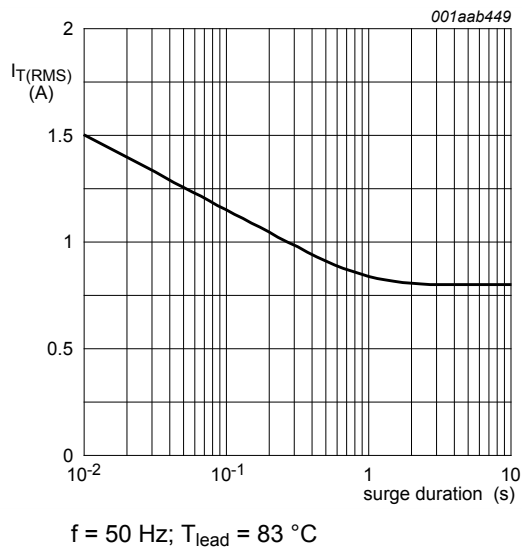


Fig. 2. RMS on-state current as a function of surge duration for sinusoidal currents

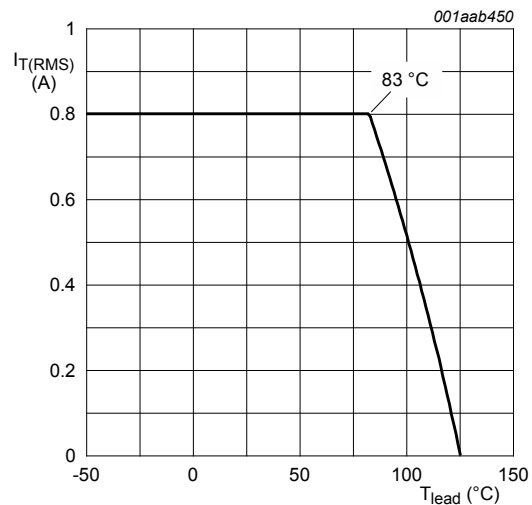


Fig. 3. RMS on-state current as a function of lead temperature; maximum values

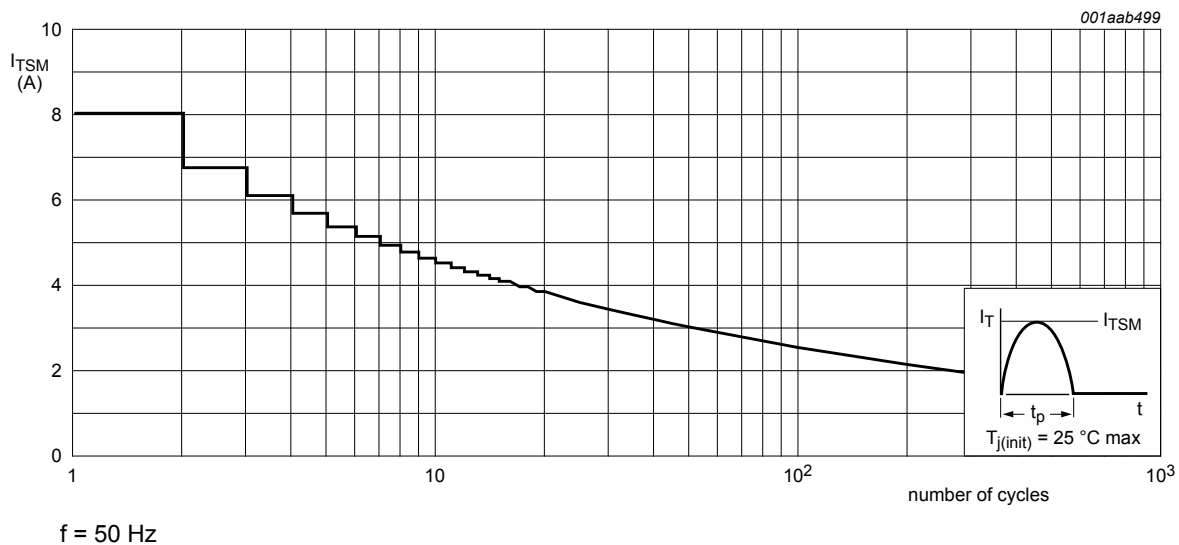
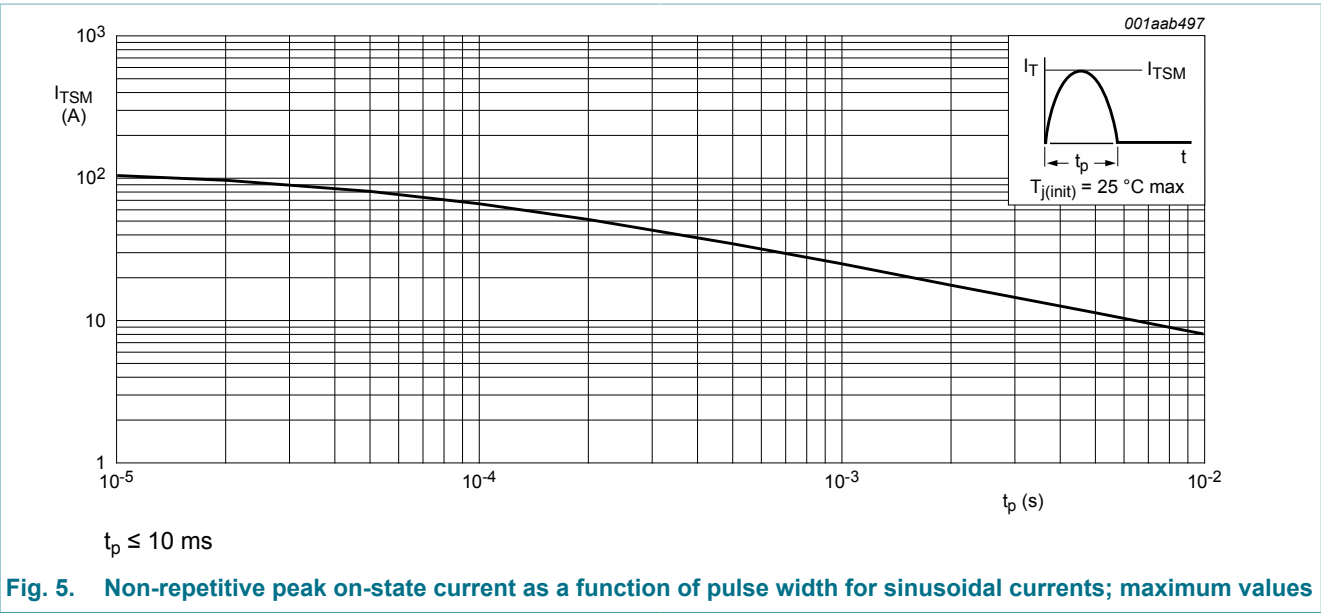


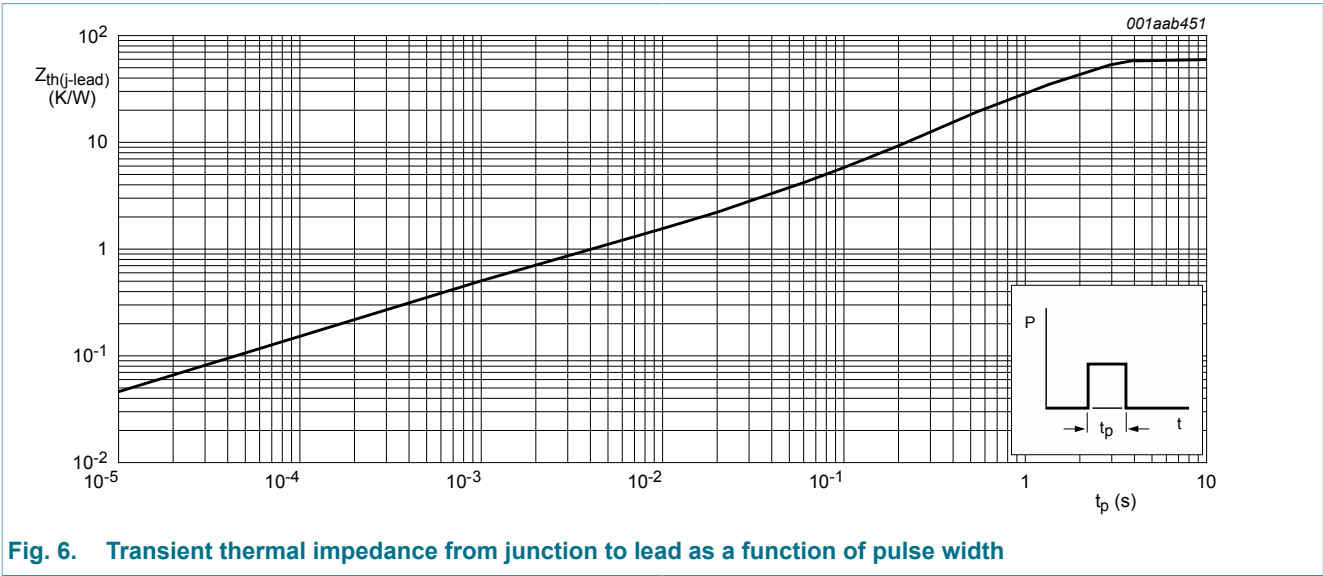
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

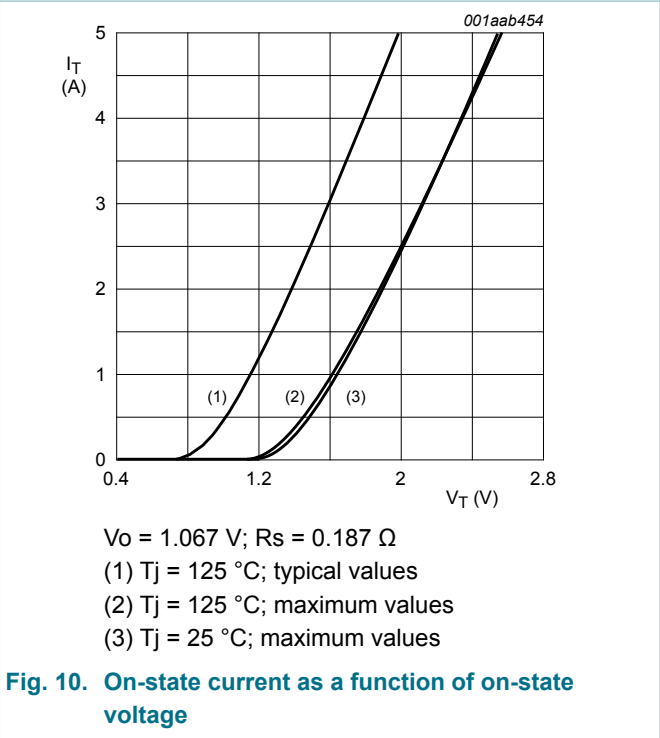
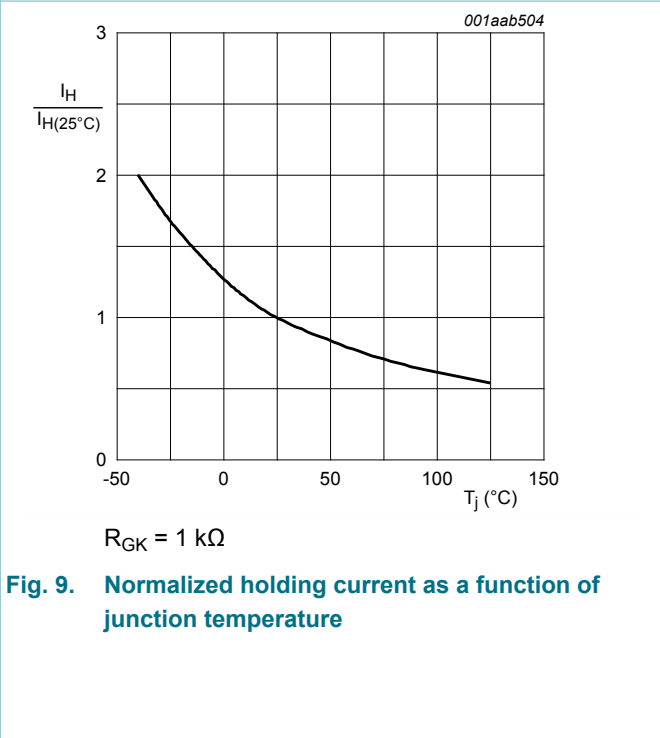
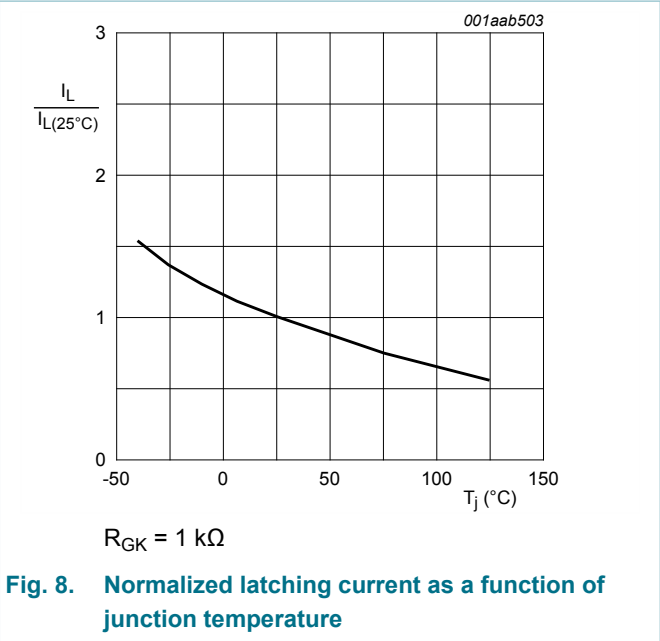
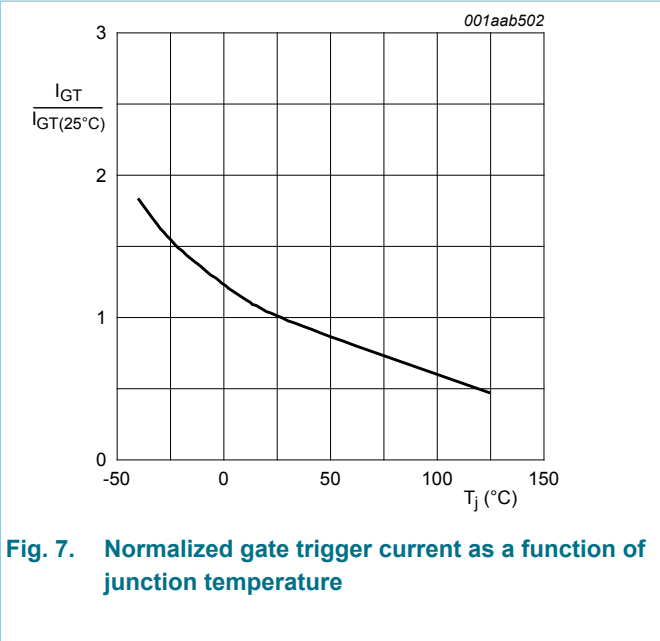
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	Fig. 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W

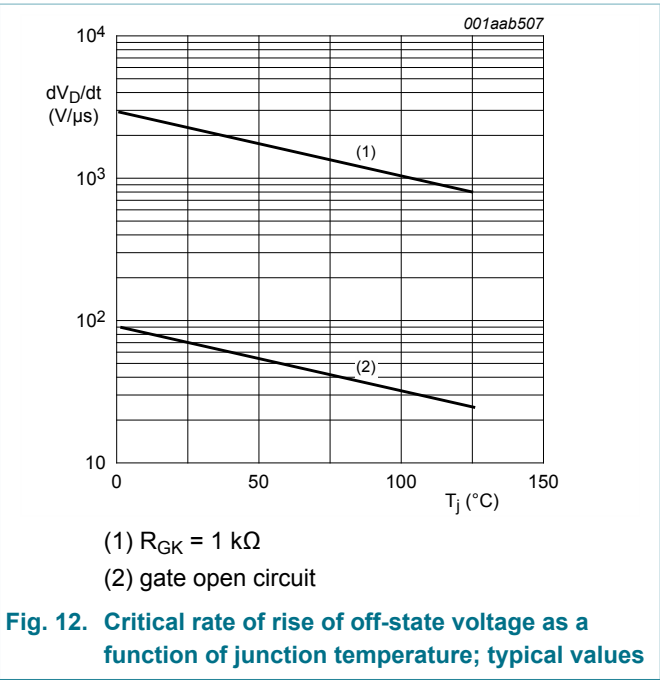
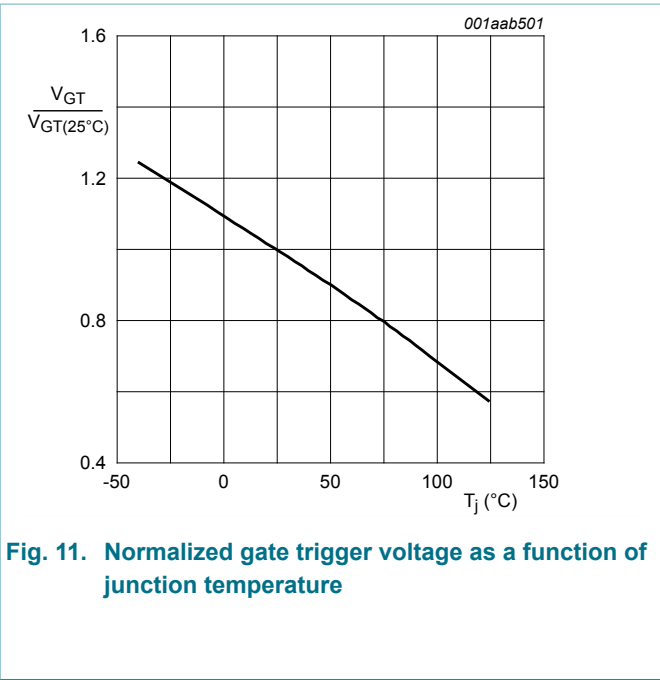


9. Characteristics

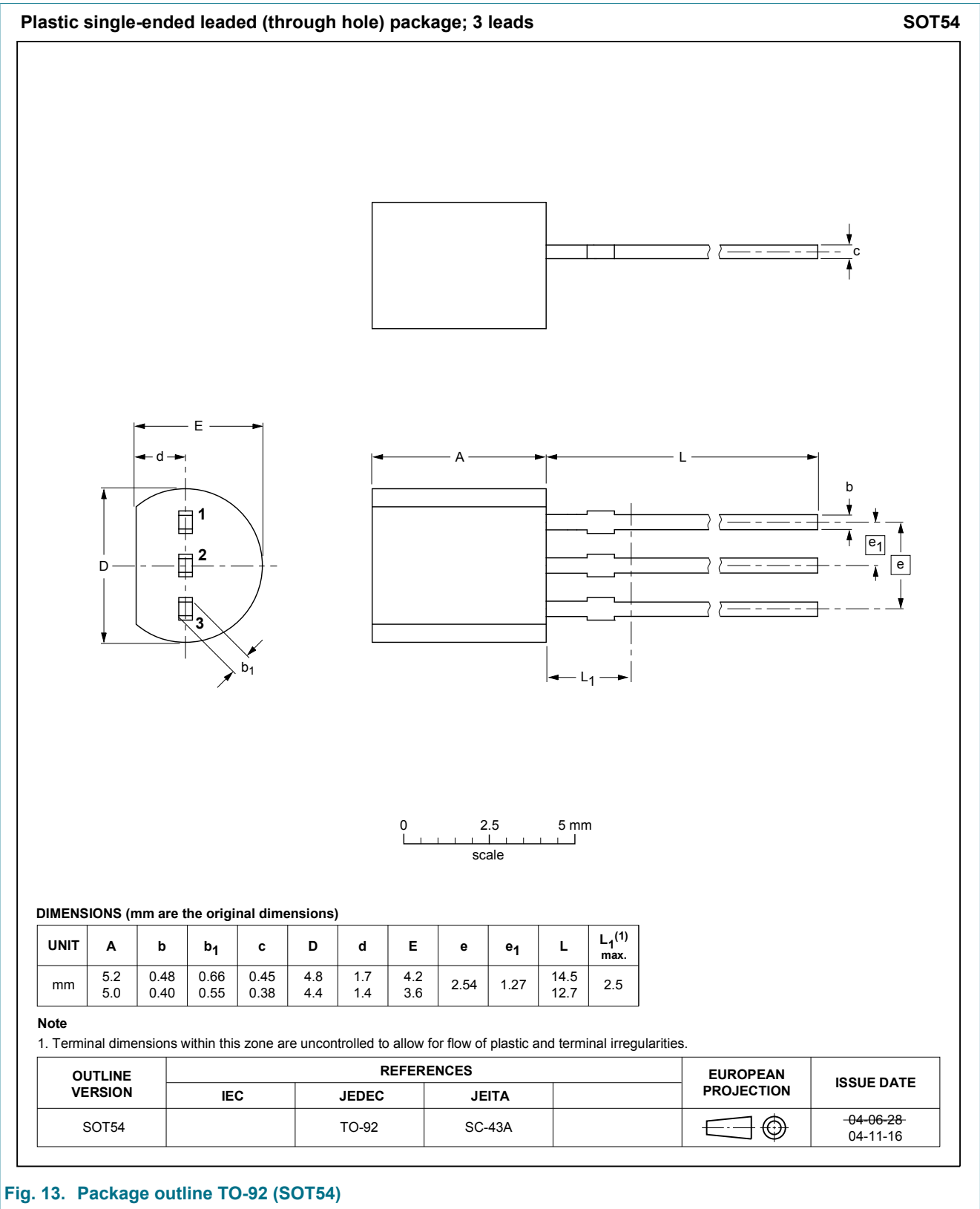
Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ °C}$; Fig. 7		-	50	200	μA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.5\text{ mA}$; $R_{GK} = 1\text{ k}\Omega$; $T_j = 25\text{ °C}$; Fig. 8		-	2	6	mA
I_H	holding current	$V_D = 12\text{ V}$; $R_{GK} = 1\text{ k}\Omega$; $T_j = 25\text{ °C}$; Fig. 9		-	2	5	mA
V_T	on-state voltage	$I_T = 1.2\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10		-	1.25	1.7	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ °C}$; Fig. 11		-	0.5	0.8	V
		$V_D = 600\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 125\text{ °C}$; Fig. 11		0.2	0.3	-	V
I_D	off-state current	$V_D = 600\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$		-	0.05	0.1	mA
I_R	reverse current	$V_R = 600\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$		-	0.05	0.1	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 12		500	800	-	$\text{V}/\mu\text{s}$
		$V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 12		-	2	-	$\text{V}/\mu\text{s}$
t_{gt}	gate-controlled turn-on time	$I_{TM} = 2\text{ A}$; $V_D = 600\text{ V}$; $I_G = 10\text{ mA}$; $dI_G/dt = 0.1\text{ A}/\mu\text{s}$; $T_j = 25\text{ °C}$		-	2	-	μs
t_q	commutated turn-off time	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; $I_{TM} = 1.6\text{ A}$; $V_R = 35\text{ V}$; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$; $dV_D/dt = 2\text{ V}/\mu\text{s}$; $R_{GK} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM})		-	100	-	μs





10. Package outline



11. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692
Email amall@ameya360.com
QQ 800077892
Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333
Email mkt@ameya360.com