FAIRCHILD
SEMICONDUCTOR®

October 2013

FDP060AN08A0 / FDB060AN08A0

## N-Channel PowerTrench® MOSFET
75 V, 80 A, 6 mΩ

Features

- $R_{DS(on)}$ = 4.8 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 80 A
- $Q_{G(tot)}$ = 73 nC (Typ.) @ V_{GS} = 10 V
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)

Formerly developmental type 82680

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies

TO-220

D²-PAK
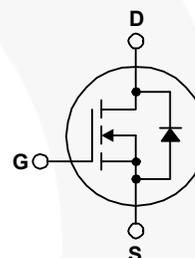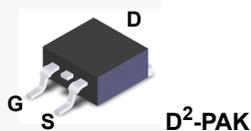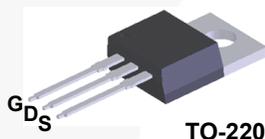
MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	FDP060AN08A0 FDB060AN08A0	Unit
V_{DSS}	Drain to Source Voltage	75	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current		
	Continuous (T_C < 127°C, V_{GS} = 10V)	80	A
	Continuous (T_{amb} = 25°C, V_{GS} = 10V, with $R_{\theta JA}$ = 43°C/W)	16	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	350	mJ
P_D	Power dissipation	255	W
	Derate above 25°C	1.7	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case, Max. TO-220, D²-PAK	0.58	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, Max. TO-220, D²-PAK (Note 2)	62	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, Max. D²-PAK, 1in² copper pad area	43	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB060AN08A0	FDB060AN08A0	D²-PAK	330 mm	24 mm	800 units
FDP060AN08A0	FDP060AN08A0	TO-220	Tube	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Off Characteristics							
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V		75	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60V		-	-	1	µA
		V_{GS} = 0V	T_C = 150°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V		-	-	±100	nA
On Characteristics							
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA		2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 80A, V_{GS} = 10V		-	0.0048	0.006	Ω
		I_D = 40A, V_{GS} = 6V		-	0.0066	0.010	
		I_D = 80A, V_{GS} = 10V, T_J = 175°C		-	0.010	0.013	
Dynamic Characteristics							
C_{ISS}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	5150	-	pF
C_{OSS}	Output Capacitance			-	800	-	pF
C_{RSS}	Reverse Transfer Capacitance			-	230	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V			73	95	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 2V	V_{DD} = 40V	-	10	13	nC
Q_{gs}	Gate to Source Gate Charge		I_D = 80A	-	29	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		I_g = 1.0mA	-	19	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	16	-	nC
Switching Characteristics $(V_{GS}$ = 10V)							
t_{ON}	Turn-On Time	V_{DD} = 40V, I_D = 80A, V_{GS} = 10V, R_{GS} = 3.9Ω		-	-	147	ns
$t_{d(ON)}$	Turn-On Delay Time			-	19	-	ns
t_r	Rise Time			-	79	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time			-	37	-	ns
t_f	Fall Time			-	38	-	ns
t_{OFF}	Turn-Off Time			-	-	113	ns
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 80A		-	-	1.25	V
		I_{SD} = 40A		-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 75A, dI_{SD}/dt = 100A/µs		-	-	37	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 75A, dI_{SD}/dt = 100A/µs		-	-	38	nC

Notes:
1: Starting T_J = 25°C, L = 109µH, I_{AS} = 80A.
2: Pulse width = 100s

Typical Characteristics T_C = 25°C unless otherwise noted
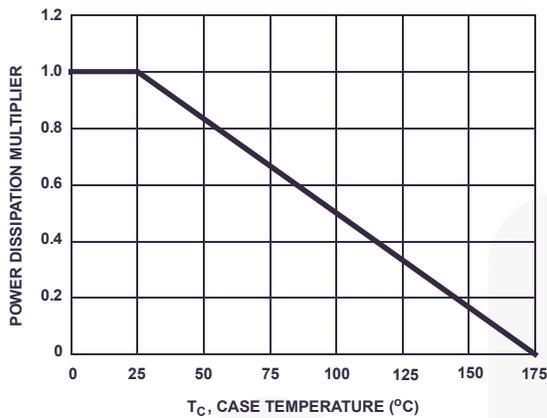
Figure 1. Normalized Power Dissipation vs Ambient Temperature
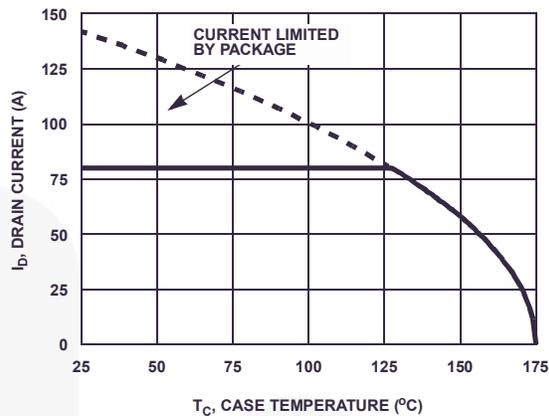
Figure 2. Maximum Continuous Drain Current vs Case Temperature

NOTES:
DUTY FACTOR: D = t_1/t_2
PEAK T_J = P_{DM} x $Z_{\theta JC}$ x $R_{\theta JC}$ + T_C
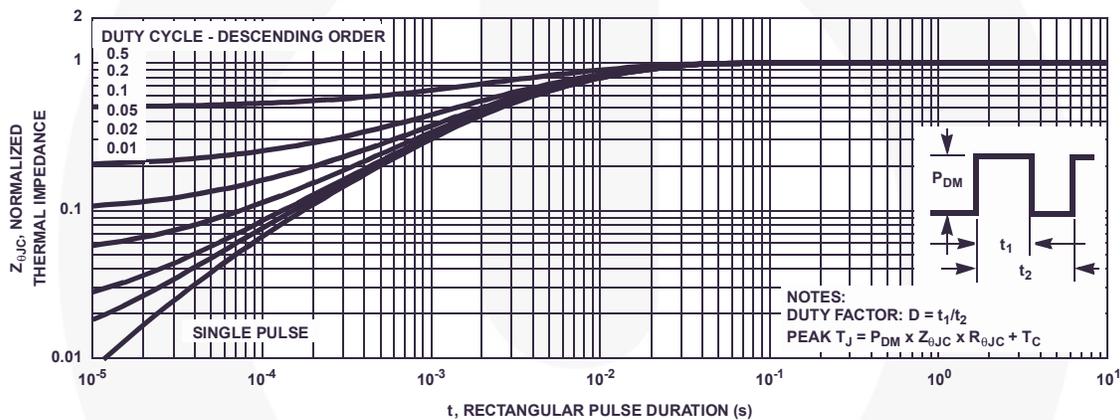
Figure 3. Normalized Maximum Transient Thermal Impedance

T_C = 25°C
FOR TEMPERATURES
ABOVE 25°C DERATE PEAK
CURRENT AS FOLLOWS:

$$I = I_{25} \sqrt{\frac{175 - T_C}{150}}$$
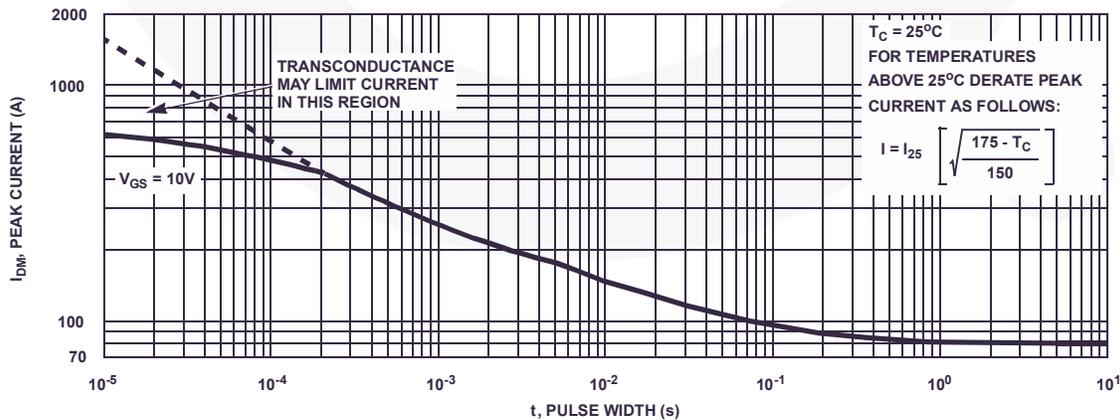
Figure 4. Peak Current Capability

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Typical Characteristics T_C = 25°C unless otherwise noted
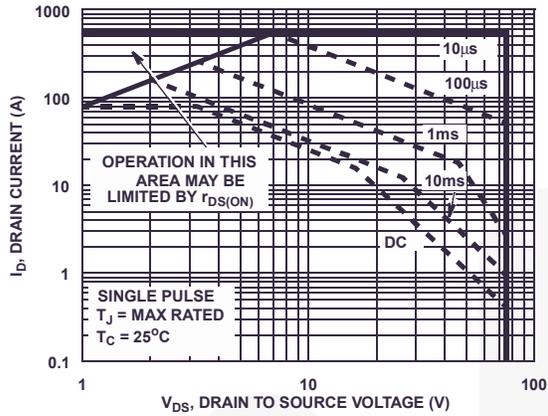
Figure 5. Forward Bias Safe Operating Area
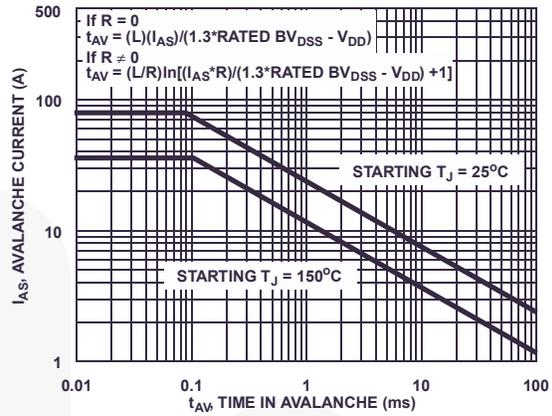
NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

In Figure 6:

If R = 0
$$t_{AV} = (L)(I_{AS})/(1.3*RATED\ BV_{DSS} - V_{DD})$$
If R ≠ 0
$$t_{AV} = (L/R)ln[(I_{AS}*R)/(1.3*RATED\ BV_{DSS} - V_{DD}) +1]$$
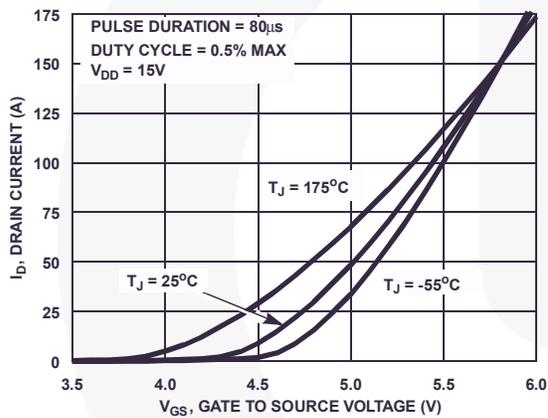
Figure 7. Transfer Characteristics
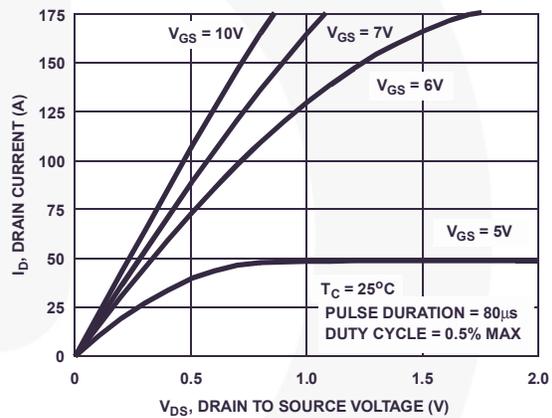
Figure 8. Saturation Characteristics
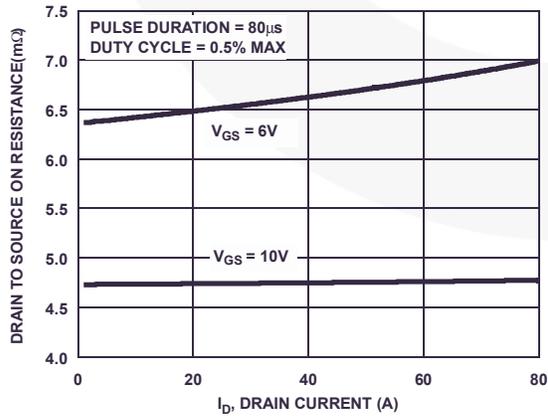
Figure 9. Drain to Source On Resistance vs Drain Current
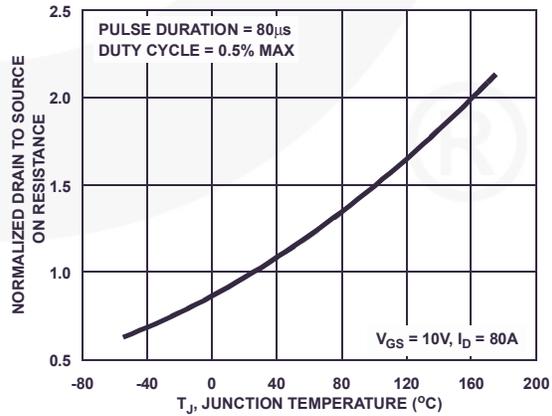
Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics T_C = 25°C unless otherwise noted
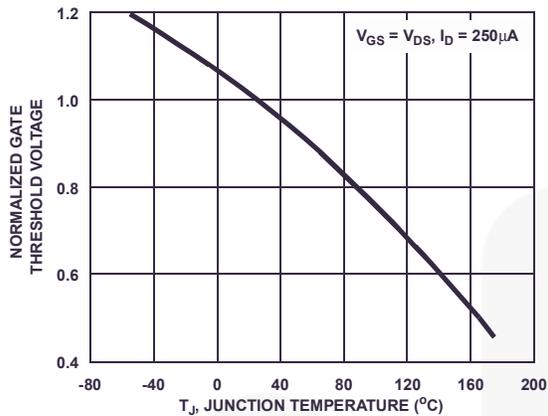
Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

$V_{GS} = V_{DS}, I_D = 250\mu A$

NORMALIZED GATE THRESHOLD VOLTAGE

T_J, JUNCTION TEMPERATURE (°C)
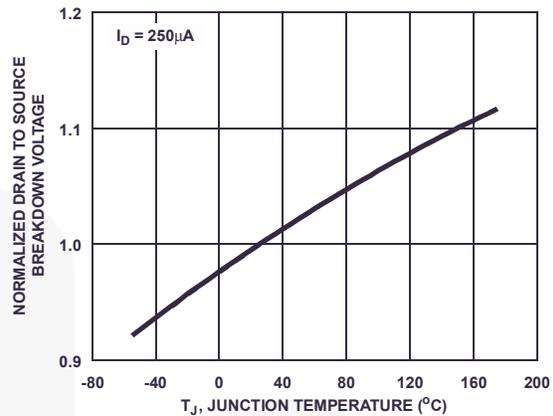
Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

$I_D = 250\mu A$

NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE

T_J, JUNCTION TEMPERATURE (°C)
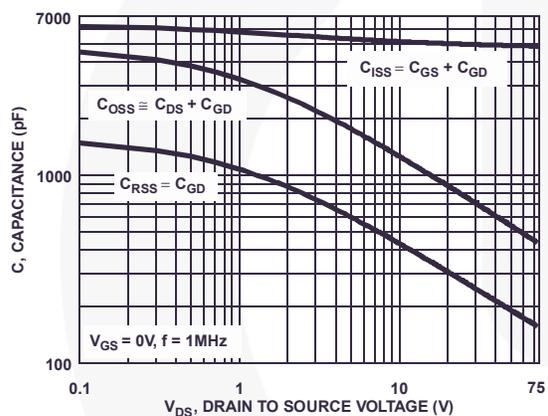
Figure 13. Capacitance vs Drain to Source Voltage

$C_{ISS} = C_{GS} + C_{GD}$

$C_{OSS} \cong C_{DS} + C_{GD}$

$C_{RSS} = C_{GD}$

$V_{GS} = 0V, f = 1MHz$

C, CAPACITANCE (pF)

V_{DS}, DRAIN TO SOURCE VOLTAGE (V)
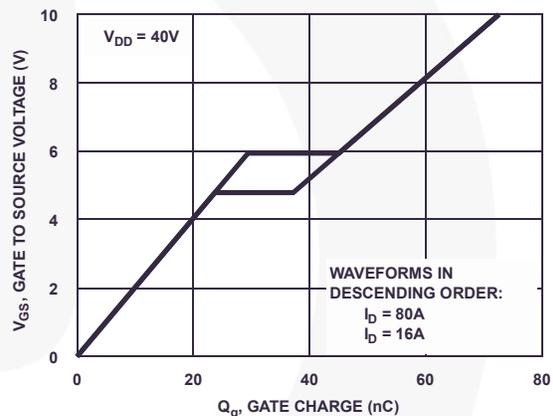
Figure 14. Gate Charge Waveforms for Constant Gate Current

$V_{DD} = 40V$

WAVEFORMS IN DESCENDING ORDER:
$I_D = 80A$
$I_D = 16A$

V_{GS}, GATE TO SOURCE VOLTAGE (V)

Q_g, GATE CHARGE (nC)

Test Circuits and Waveforms
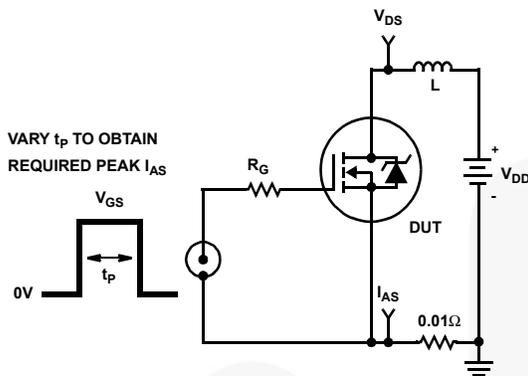
Figure 15. Unclamped Energy Test Circuit
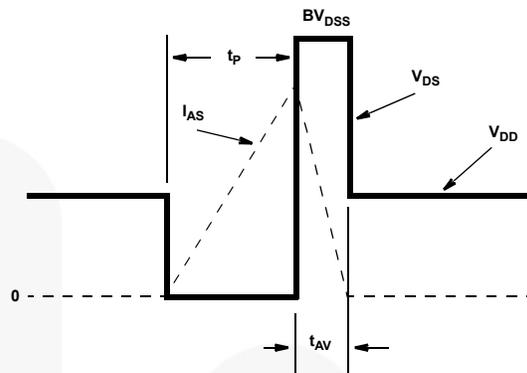
Figure 16. Unclamped Energy Waveforms
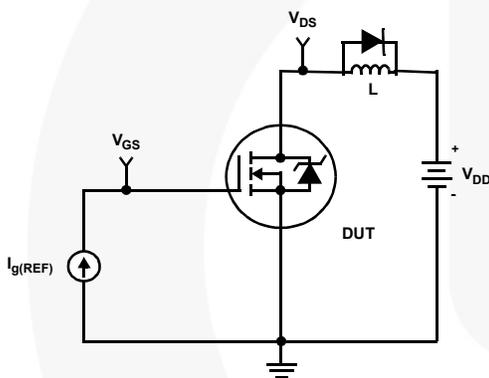
Figure 17. Gate Charge Test Circuit
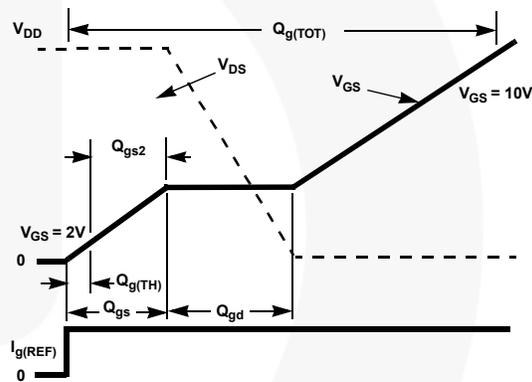
Figure 18. Gate Charge Waveforms
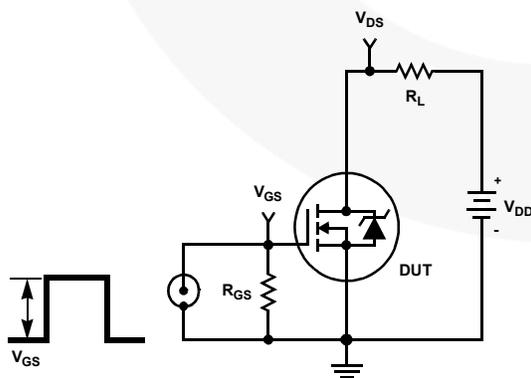
Figure 19. Switching Time Test Circuit
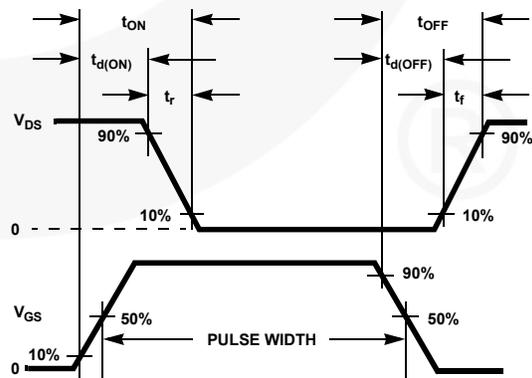
Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A ($^{\circ}$C), and thermal resistance $R_{\theta JA}$ ($^{\circ}$C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.

2. The number of copper layers and the thickness of the board.

3. The use of external heat sinks.

4. The use of thermal vias.

5. Air flow and board orientation.

6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{(0.262 + Area)} \qquad \text{(EQ. 2)}$$
Area in Inches Squared

$$R_{\theta JA} = 26.51 + \frac{128}{(1.69 + Area)} \qquad \text{(EQ. 3)}$$
Area in Centimeters Squared

$R_{\theta JA} = 26.51 + 19.84/(0.262 + Area)$ EQ.2

$R_{\theta JA} = 26.51 + 128/(1.69 + Area)$ EQ.3
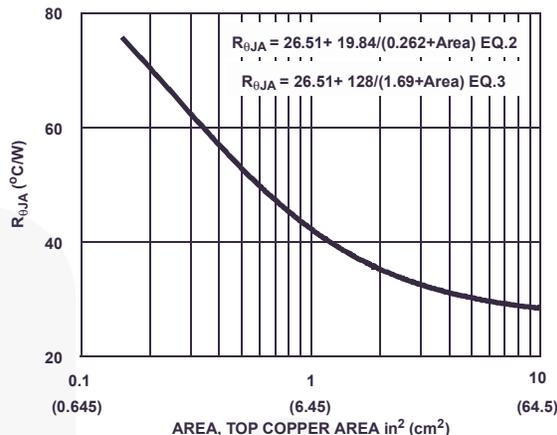
Figure 21. Thermal Resistance vs Mounting Pad Area

PSPICE Electrical Model

.SUBCKT FDP060AN08A0 2 1 3 ; rev October 2002
Ca 12 8 2.5e-9
Cb 15 14 2.1e-9
Cin 6 8 4.7e-9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 82.1
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 5.3e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 5e-9

RLgate 1 9 53
RLdrain 2 5 10
RLsource 3 7 50

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 9e-4
Rgate 9 20 1.4
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 3e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*350),5))}

.MODEL DbodyMOD D (IS=2E-11 N=1.04 RS=1.76e-3 TRS1=2.7e-3 TRS2=1e-6
+ CJO=3.2e-9 M=5.6e-1 TT=3e-10 XTI=3.9)
.MODEL DbreakMOD D (RS=3e-1 TRS1=1e-3 TRS2=-8.9e-6)
.MODEL DplcapMOD D (CJO=1.56e-9 IS=1e-30 N=10 M=0.53)

.MODEL MmedMOD NMOS (VTO=3.6 KP=6 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.4)
.MODEL MstroMOD NMOS (VTO=4.22 KP=220 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MweakMOD NMOS (VTO=3 KP=0.03 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=14 RS=0.1)

.MODEL RbreakMOD RES (TC1=9.4e-4 TC2=-9e-7)
.MODEL RdrainMOD RES (TC1=2.2e-2 TC2=6e-5)
.MODEL RSLCMOD RES (TC1=2e-3 TC2=1e-5)
.MODEL RsourceMOD RES (TC1=1e-3 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=-6e-3 TC2=-1.6e-5)
.MODEL RvtempMOD RES (TC1=-2.4e-3 TC2=1e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-8 VOFF=-5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5 VOFF=-8)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-3.5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.5 VOFF=-4)
.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.
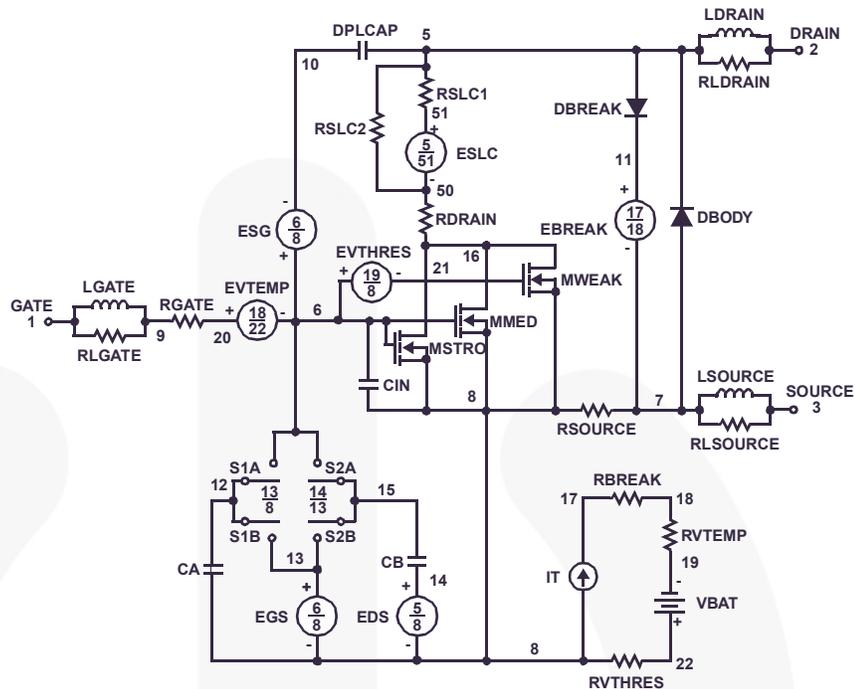
SABER Electrical Model

rev October 2002
template FDP060AN08A0 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod = (isl=2e-11,nl=1.04,rs=1.76e-3,trs1=2.7e-3,trs2=1e-6,cjo=3.2e-9,m=5.6e-1,tt=3e-10,xti=3.9)
dp..model dbreakmod = (rs=3e-1,trs1=1e-3,trs2=-8.9e-6)
dp..model dplcapmod = (cjo=1.56e-9,isl=10e-30,nl=10,m=0.53)
m..model mmedmod = (type=_n,vto=3.6,kp=6,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=4.22,kp=220,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=3,kp=0.03,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-8,voff=-5)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-5,voff=-8)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-4,voff=-3.5)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-3.5,voff=-4)
c.ca n12 n8 = 2.5e-9
c.cb n15 n14 = 2.1e-9
c.cin n6 n8 = 4.7e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 82.1
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 5.3e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 5e-9

res.rlgate n1 n9 = 53
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 50

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=9.4e-4,tc2=-9e-7
res.rdrain n50 n16 = 9e-4, tc1=2.2e-2,tc2=6e-5
res.rgate n9 n20 = 1.4
res.rslc1 n5 n51 = 1e-6, tc1=2e-3,tc2=1e-5
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 3e-3, tc1=1e-3,tc2=1e-6
res.rvthres n22 n8 = 1, tc1=-6e-3,tc2=-1.6e-5
res.rvtemp n18 n19 = 1, tc1=-2.4e-3,tc2=1e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/350))** 5))
}
}
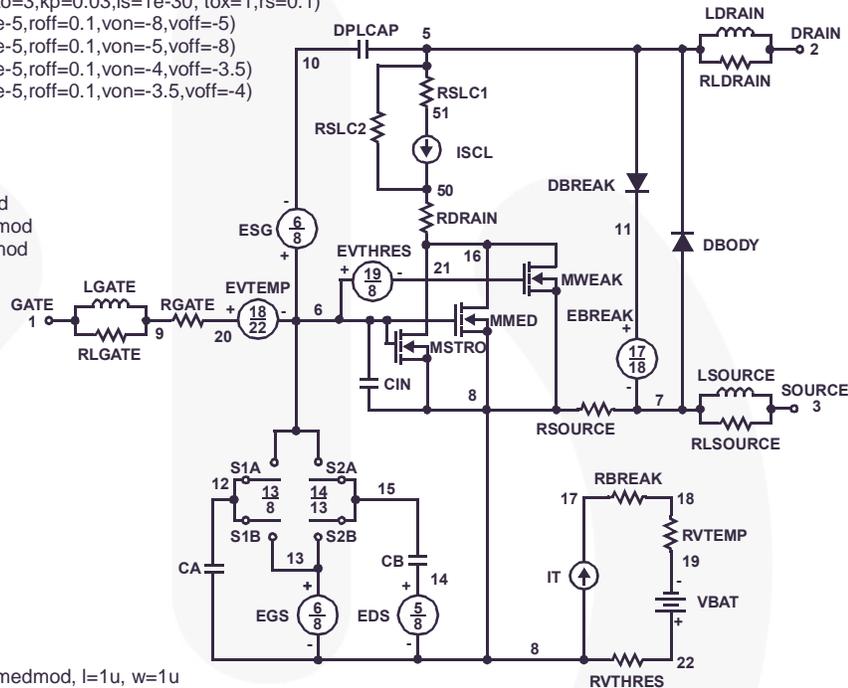
SPICE Thermal Model

REV 23 October 2002

FDP060AN08A0T

CTHERM1 TH 6 9.6e-3
CTHERM2 6 5 9.7e-3
CTHERM3 5 4 9.8e-3
CTHERM4 4 3 1e-2
CTHERM5 3 2 3e-2
CTHERM6 2 TL 9e-2

RTHERM1 TH 6 3.2e-3
RTHERM2 6 5 8.1e-3
RTHERM3 5 4 2.3e-2
RTHERM4 4 3 1.2e-1
RTHERM5 3 2 1.5e-1
RTHERM6 2 TL 1.6e-1

SABER Thermal Model

SABER thermal model FDP060AN08A0T
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 =9.6e-3
ctherm.ctherm2 6 5 =9.7e-3
ctherm.ctherm3 5 4 =9.8e-3
ctherm.ctherm4 4 3 =1e-2
ctherm.ctherm5 3 2 =3e-2
ctherm.ctherm6 2 tl =9e-2

rtherm.rtherm1 th 6 =3.2e-3
rtherm.rtherm2 6 5 =8.1e-3
rtherm.rtherm3 5 4 =2.3e-2
rtherm.rtherm4 4 3 =1.2e-1
rtherm.rtherm5 3 2 =1.5e-1
rtherm.rtherm6 2 tl =1.6e-1
}

th ○ JUNCTION

RTHERM1   CTHERM1
6
RTHERM2   CTHERM2
5
RTHERM3   CTHERM3
4
RTHERM4   CTHERM4
3
RTHERM5   CTHERM5
2
RTHERM6   CTHERM6

tl ○ CASE

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Mechanical Dimensions

TO-220 3L

Figure 22. TO-220, Molded, 3Lead, Jedec Variation AB

NOTES: UNLESS OTHERWISE SPECIFIED
A) REFERENCE JEDEC, TO-220, ISSUE K,
VARIATION AB, DATED APRIL, 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER
ANSI Y14.5 - 1973
D) LOCATION OF THE PIN HOLE MAY VARY
(LOWER LEFT CORNER, LOWER CENTER
AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE,
F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.14 - 1.40
G) DRAWING FILE NAME: TO220B03REV6

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Dimension in Millimeters

Mechanical Dimensions

TO-263 2L (D²PAK)

NOTES: UNLESS OTHERWISE SPECIFIED
A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) REFERENCE JEDEC, TO-263, VARIATION AB.
C) DIMENSIONING AND TOLERANCING PER
   ANSI Y14.5M – 1994.
D) LOCATION OF THE PIN HOLE MAY VARY
   (LOWER LEFT CORNER, LOWER CENTER
   AND CENTER OF THE PACKAGE).
E) LANDPATTERN RECOMMENDATION PER IPC
   TO254P1524X482-3N
F) FILENAME: TO263A02REV6

LAND PATTERN RECOMMENDATION
UNLESS NOTED, ALL DIMS TYPICAL

DETAIL A, ROTATED 90°
SCALE: 2X

Figure 23. 2LD, TO263, Surface Mount

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Dimension in Millimeters

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