COMPLEMENTARY PAIR ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

Features

- Low On-Resistance
- Low Gate Threshold Voltage $V_{GS(th)}$ <1V
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Complementary Pair MOSFET
- Ultra-Small Surface Mount Package
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **ESD Protected Gate**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

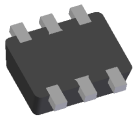
Mechanical Data

- Case: SOT-563
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminal Connections: See Diagram
- Terminals: Finish – Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.006 grams (approximate)

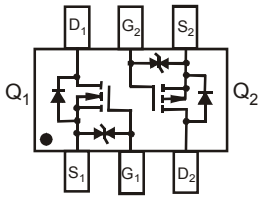
ESD protected

SOT-563

TOP VIEW



BOTTOM VIEW



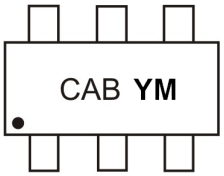
TOP VIEW
Internal Schematic

Ordering Information (Note 4)

Part Number	Case	Packaging
DMC2004VK-7	SOT-563	3000/Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.

Marking Information



CAB = Product Type Marking Code
YM = Date Code Marking
Y = Year ex: U = 2007
M = Month ex: 9 = September

Date Code Key

Year	2007	2008	2009	2010	2011	2012
Code	U	V	W	X	Y	Z

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings N-CHANNEL – Q_1 (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	±8	V
Drain Current (Note 5)	T_A = +25°C T_A = +85°C	I_D	670 480	mA

Maximum Ratings P-CHANNEL – Q_2 (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±8	V
Drain Current (Note 5)	T_A = +25°C T_A = +85°C	I_D	-530 -380	mA

Thermal Characteristics

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)		P_D	0.45	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	281	°C/W
	t<10s		210	°C/W
Total Power Dissipation (Note 6)		P_D	1	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	129	°C/W
	t<10s		97	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics N-CHANNEL – Q_1 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	V_{GS} = 0V, I_D = 10μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1.0	μA	V_{DS} = 16V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	± 1.0	μA	V_{GS} = ±4.5V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	0.5	—	1.0	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	— — —	0.4 0.5 0.7	0.55 0.70 0.90	Ω	V_{GS} = 4.5V, I_D = 540mA V_{GS} = 2.5V, I_D = 500mA V_{GS} = 1.8V, I_D = 350mA
Forward Transfer Admittance (Note 8)	$\|Y_{fs}\|$	200	—	—	mS	V_{DS} =10V, I_D = 0.2A
Diode Forward Voltage	V_{SD}	0.5	—	1.2	V	V_{GS} = 0V, I_S = 115mA
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	—	—	150	pF	V_{DS} = 16V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	—	25	pF	
Reverse Transfer Capacitance	C_{rss}	—	—	20	pF	

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

Electrical Characteristics P-CHANNEL – Q_2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1.0	µA	V_{DS} = -20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	± 1.0	µA	V_{GS} = ±4.5V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.5	—	-1.0	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	—	0.7 1.1 1.7	0.9 1.4 2.0	Ω	V_{GS} = -4.5V, I_D = -430mA V_{GS} = -2.5V, I_D = -300mA V_{GS} = -1.8V, I_D = -150mA
Forward Transfer Admittance	$\|Y_{fs}\|$	200	—	—	mS	V_{DS} =10V, I_D = 0.2A
Diode Forward Voltage	V_{SD}	-0.5	—	-1.2	V	V_{GS} = 0V, I_S = -115mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	—	175	pF	V_{DS} = -16V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	—	30	pF	
Reverse Transfer Capacitance	C_{rss}	—	—	20	pF	

Q_1, N-CHANNEL

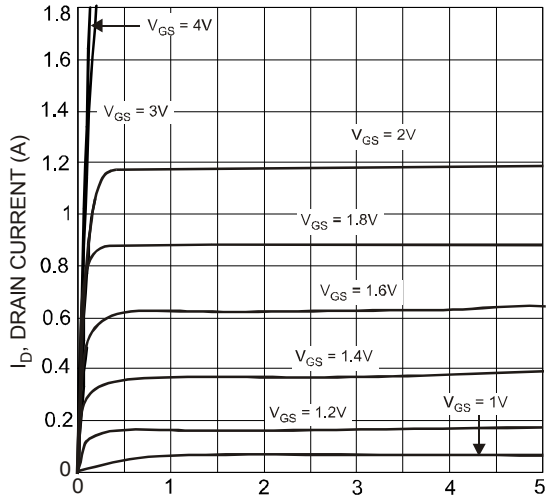


Fig. 1 Typical Output Characteristics

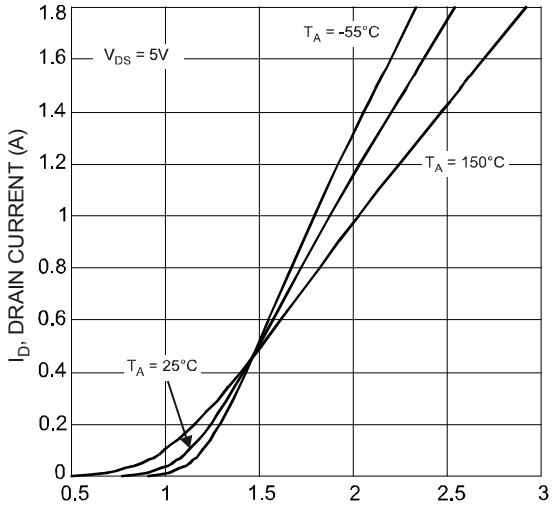


Fig. 2 Typical Transfer Characteristics

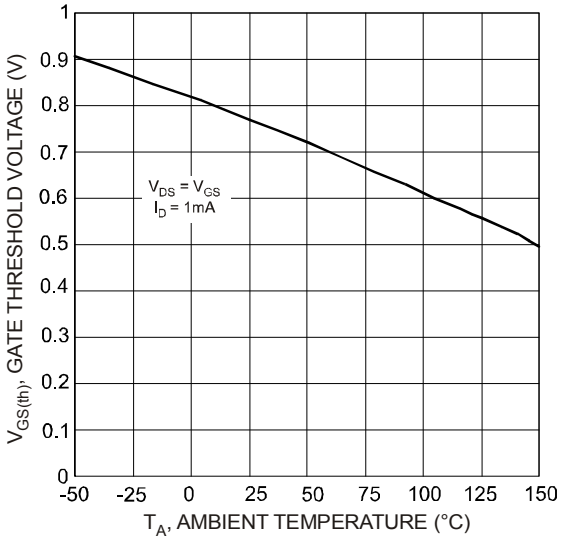


Fig. 3 Gate Threshold Voltage vs. Ambient Temperature

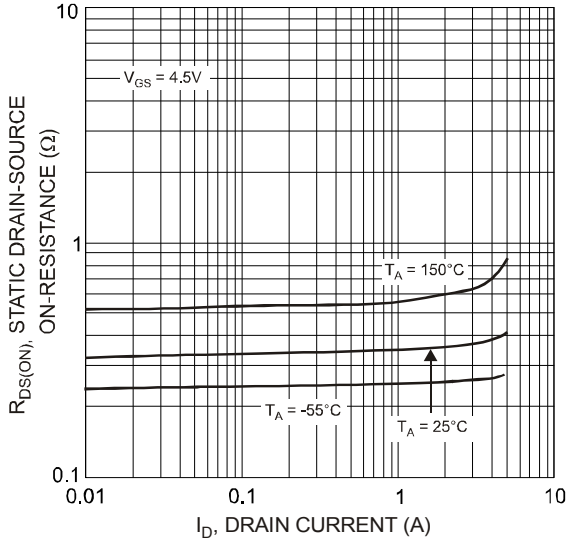


Fig. 4 Static Drain-Source On-Resistance vs. Drain Current

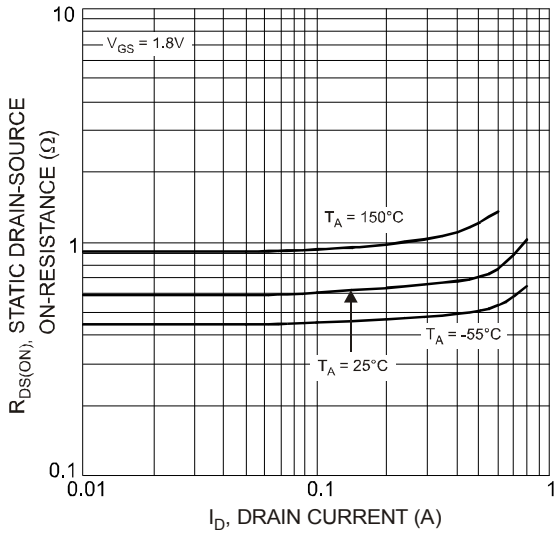


Fig. 5 Static Drain-Source On-Resistance vs. Drain Current

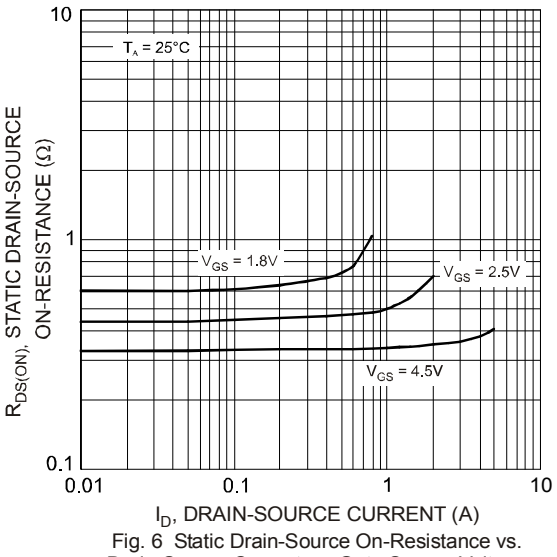


Fig. 6 Static Drain-Source On-Resistance vs. Drain-Source Current vs. Gate Source Voltage

Q_1, N-CHANNEL (cont.)

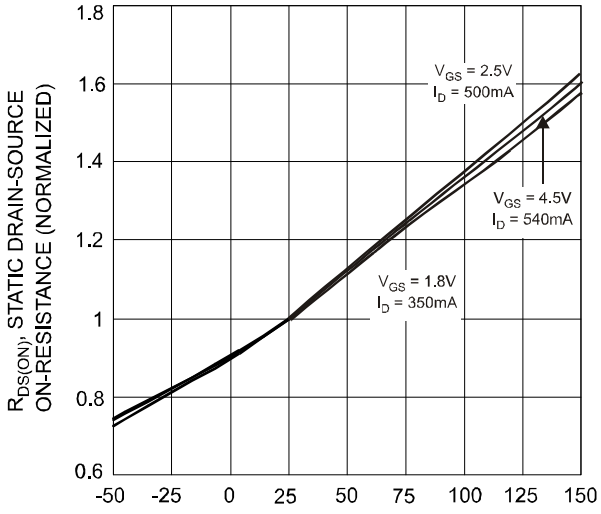


Fig. 7 Static Drain-Source On-State Resistance vs. Ambient Temperature

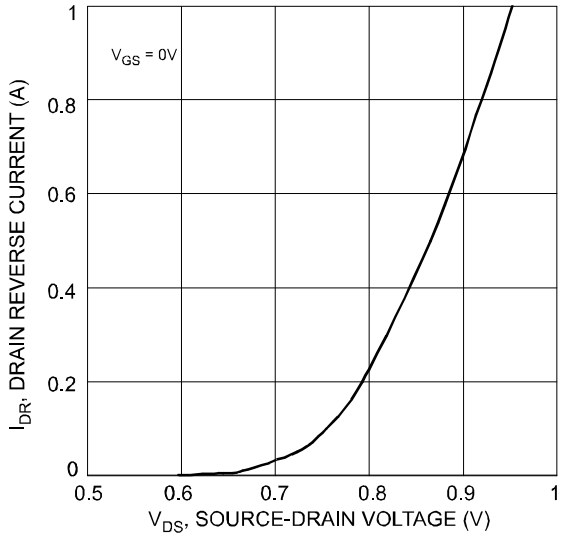


Fig. 8 Drain Reverse Current vs. Source-Drain Voltage

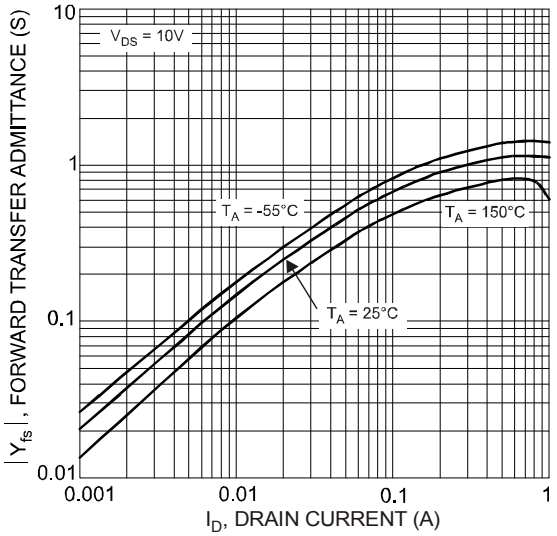


Fig. 9 Forward Transfer Admittance vs. Drain Current

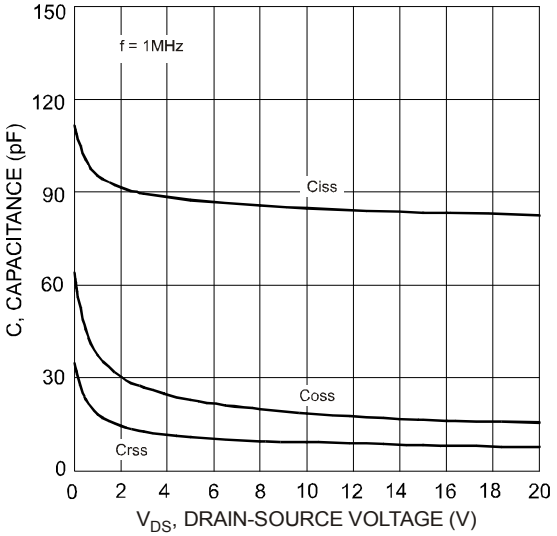


Fig. 10 Typical Capacitance

Q_2, P-CHANNEL

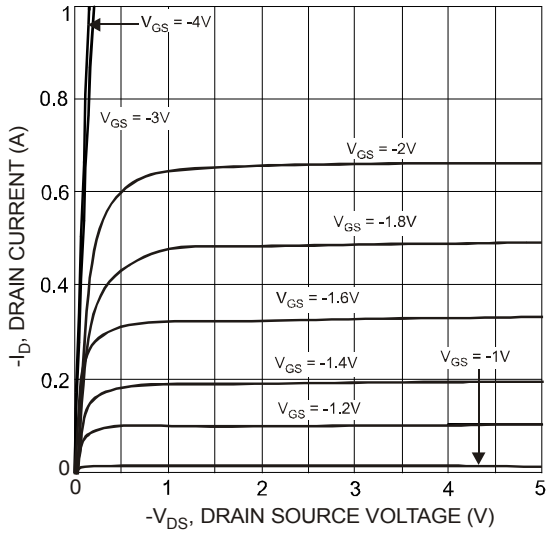


Fig. 11 Typical Output Characteristics

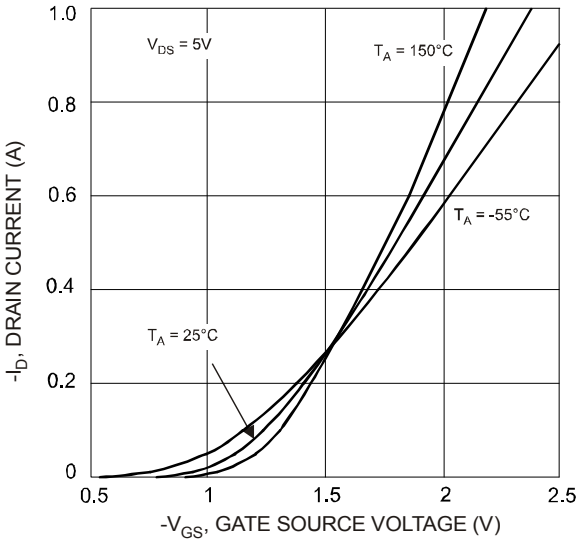


Fig. 12 Typical Transfer Characteristics

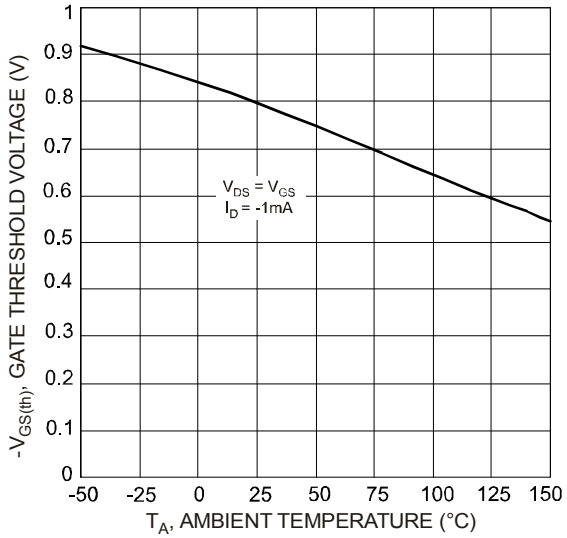


Fig. 13 Gate Threshold Voltage vs. Ambient Temperature

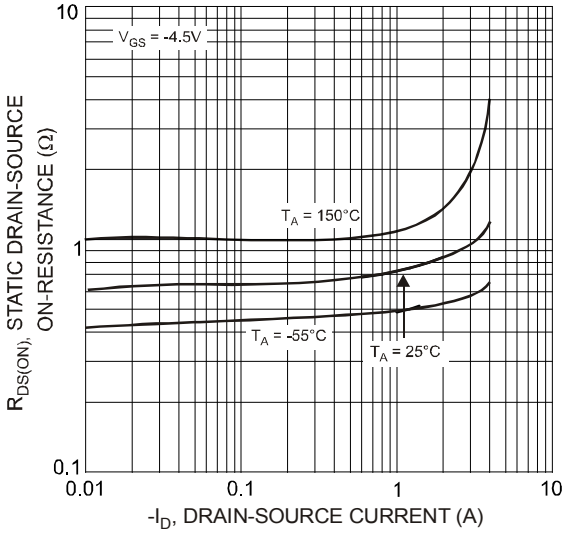


Fig. 14 Static Drain-Source On-Resistance vs. Drain Current

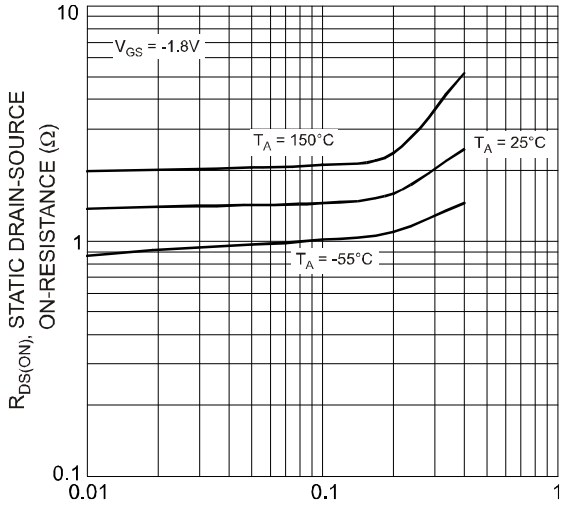


Fig. 15 Static Drain-Source On-Resistance vs. Drain Current

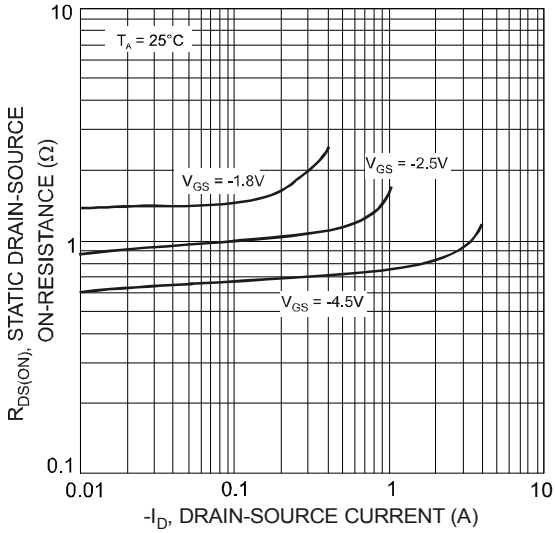


Fig. 16 Static Drain-Source On-Resistance vs. Drain-Source Current vs. Gate Source Voltage

Q_2, P-CHANNEL (cont.)

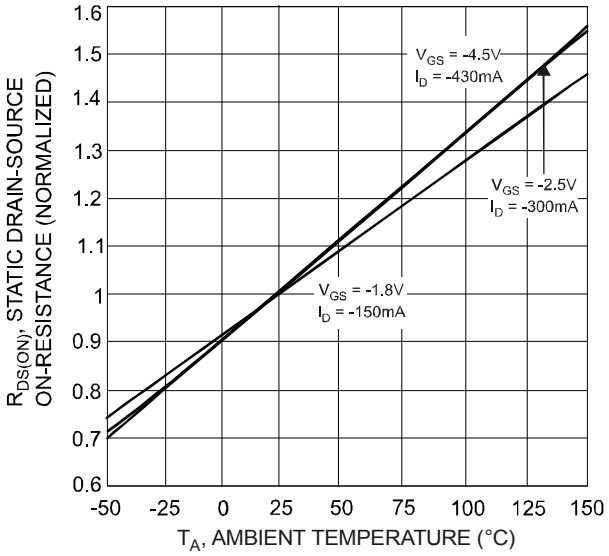


Fig. 17 Static Drain-Source On-State Resistance vs. Ambient Temperature

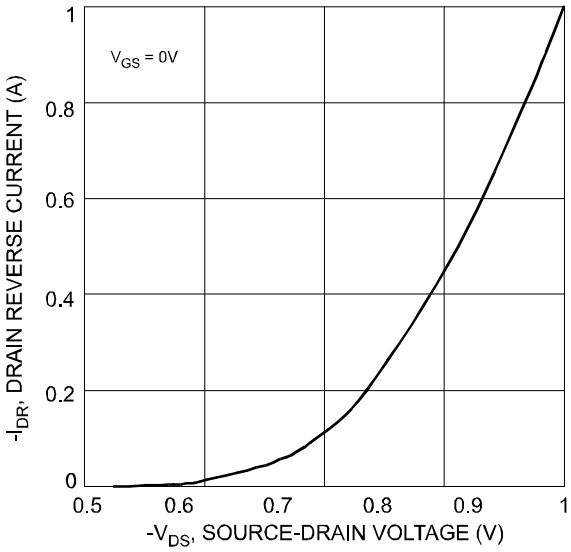


Fig. 18 Drain Reverse Current vs. Source-Drain Voltage

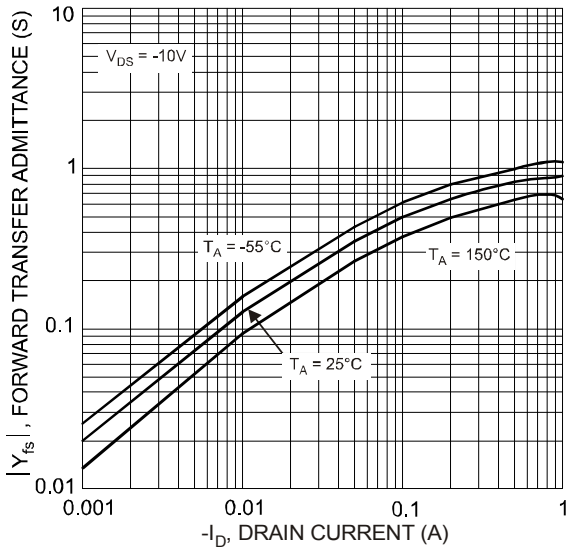


Fig. 19 Forward Transfer Admittance vs. Drain Current

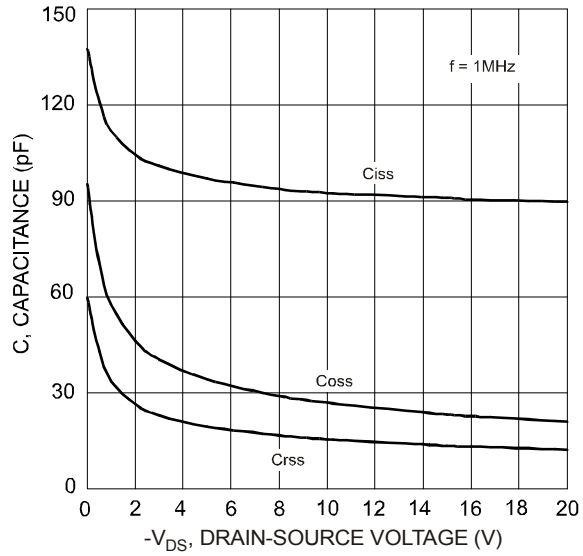
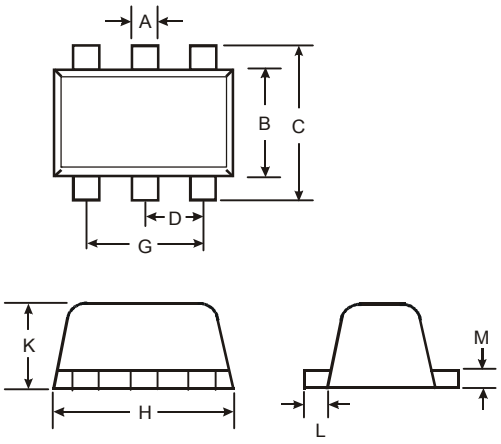


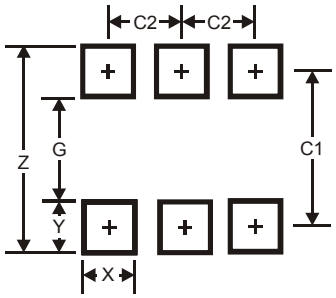
Fig. 20 Typical Capacitance

Package Outline Dimensions



SOT563			
Dim	Min	Max	Typ
A	0.15	0.30	0.20
B	1.10	1.25	1.20
C	1.55	1.70	1.60
D	-	-	0.50
G	0.90	1.10	1.00
H	1.50	1.70	1.60
K	0.55	0.60	0.60
L	0.10	0.30	0.20
M	0.10	0.18	0.11
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
Z	2.2
G	1.2
X	0.375
Y	0.5
C1	1.7
C2	0.5

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