

## Features

- Thin small outline package (TSOP I) configurable as 2 M × 16 or as 4 M × 8 static RAM (SRAM)
- Very high speed
  - 55 ns
- Wide voltage range
  - 2.2 V to 3.7 V
- Ultra low standby power
  - Typical standby current: 3 μA
  - Maximum standby current: 25 μA
- Ultra low active power
  - Typical active current: 4.5 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  Features
- Automatic power down when deselected
- Complementary Metal Oxide Semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 48-pin TSOP I package and 48-ball FBGA package

## Functional Description

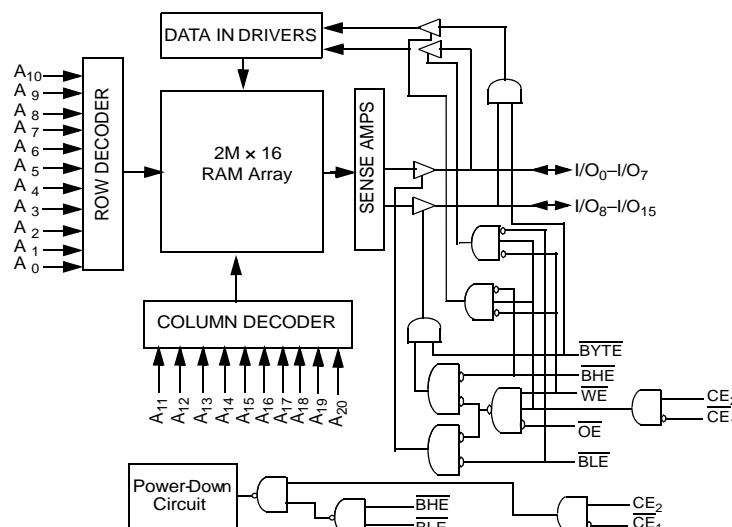
The CY62177EV30 is a high performance CMOS static RAM organized as 2 M words by 16 bits and 4 M words by 8 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 99 percent when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW or both BHE and BLE are HIGH). The input and output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high impedance state when: deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a write operation ( $CE_1$  LOW,  $CE_2$  HIGH and WE LOW).

To write to the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>20</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written to the location specified on the address pins (A<sub>0</sub> through A<sub>20</sub>). To read from the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O<sub>8</sub> to I/O<sub>15</sub>. See the [Truth Table on page 11](#) for a complete description of read and write modes.

Pin #13 of the 48 TSOP I package is an DNU pin that must be left floating at all times to ensure proper application.

For a complete list of related resources, [click here](#).

## Logic Block Diagram



## Contents

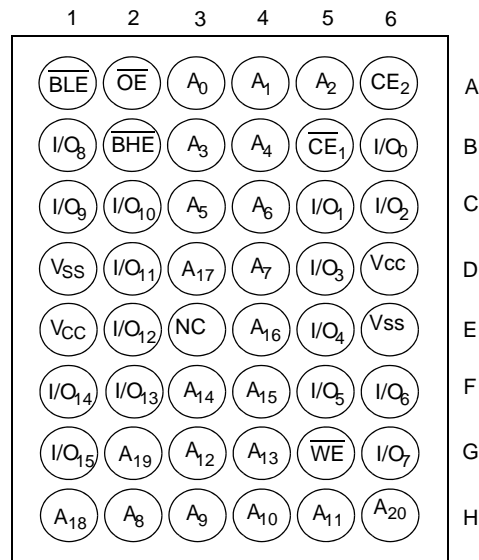
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## Pin Configurations

Figure 1. 48-pin TSOP I pinout (Front View) [1, 2]



Figure 2. 48-ball FBGA pinout (Top View)



## Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
	f = 1 MHz		f = f <sub>Max</sub>							
	Min	Typ <sup>[3]</sup>	Max		Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max
CY62177EV30LL	2.2	3.0	3.7	55	4.5	5.5	35	45	3	25

### Notes

1. DNU Pin# 13 needs to be left floating to ensure proper application.

2. The  $\overline{\text{BYTE}}$  pin in the 48-pin TSOP I package has to be tied to V<sub>CC</sub> to use the device as a 2 M x 16 SRAM.

The 48-pin TSOP I package can also be used as a 4 M x 8 SRAM by tying the  $\overline{\text{BYTE}}$  signal to V<sub>SS</sub>. In the 4 M x 8 configuration, Pin 45 is A21, while  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$ , and I/O<sub>8</sub> to I/O<sub>14</sub> pins are not used.

3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .....	-65 °C to +150 °C
Ambient temperature with power applied .....	-55 °C to +125 °C
Supply voltage to ground potential <sup>[4, 5]</sup> .....	-0.3 V to $V_{CC(max)}$ + 0.3 V
DC voltage applied to outputs in High Z state <sup>[4, 5]</sup> .....	-0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage <sup>[4, 5]</sup> .....	-0.3 V to $V_{CC(max)}$ + 0.3 V
Output current into outputs (LOW) .....	20 mA
Static discharge voltage (per MIL-STD-883, method 3015) .....	> 2001 V
Latch up current .....	> 200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[6]</sup>
CY62177EV30LL	Industrial	-40 °C to +85 °C	2.2 V to 3.7 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		55 ns			Unit
				Min	Typ <sup>[7]</sup>	Max	
V <sub>OH</sub>	Output HIGH voltage	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> = 2.20 V	2.0	-	-	V
		I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 2.70 V	2.4	-	-	V
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 0.1 mA	V <sub>CC</sub> = 2.20 V	-	-	0.4	V
		I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = 2.70 V	-	-	0.4	V
V <sub>IH</sub>	Input HIGH voltage	V <sub>CC</sub> = 2.2 V to 2.7 V		1.8	-	V <sub>CC</sub> + 0.3	V
		V <sub>CC</sub> = 2.7 V to 3.7 V		2.2	-	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW voltage	V <sub>CC</sub> = 2.2 V to 2.7 V		-0.3	-	0.6	V
		V <sub>CC</sub> = 2.7 V to 3.7 V		-0.3	-	0.7 <sup>[8]</sup>	V
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1	-	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1	-	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	f = f <sub>Max</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = V <sub>CC(max)</sub> I <sub>OUT</sub> = 0 mA CMOS levels	-	35	45	mA
		f = 1 MHz		-	4.5	5.5	mA
I <sub>SB2</sub> <sup>[9, 10]</sup>	Automatic CE power down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $\overline{CE}_2 \leq 0.2 \text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$ , f = 0, V <sub>CC</sub> = 3.7 V		-	3	25	μA

### Notes

- V<sub>IL(min)</sub> = -2.0 V for pulse durations less than 20 ns.
- V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75 V for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC</sub> (min) and 200 μs wait time after V<sub>CC</sub> stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
- Under DC conditions the device meets a V<sub>IL</sub> of 0.8 V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.7 V.
- The  $\overline{BYTE}$  pin in the 48-pin TSOP I package has to be tied to V<sub>CC</sub> to use the device as a 2 M × 16 SRAM.  
The 48-pin TSOP I package can also be used as a 4 M × 8 SRAM by tying the  $\overline{BYTE}$  signal to V<sub>SS</sub>. In the 4 M × 8 configuration, Pin 45 is A21, while  $\overline{BHE}$ ,  $\overline{BLE}$ , and I/O<sub>8</sub> to I/O<sub>14</sub> pins are not used.
- Chip enables ( $\overline{CE}_1$  and  $\overline{CE}_2$ ),  $\overline{BYTE}$ , and Byte Enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) need to be tied to CMOS levels to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

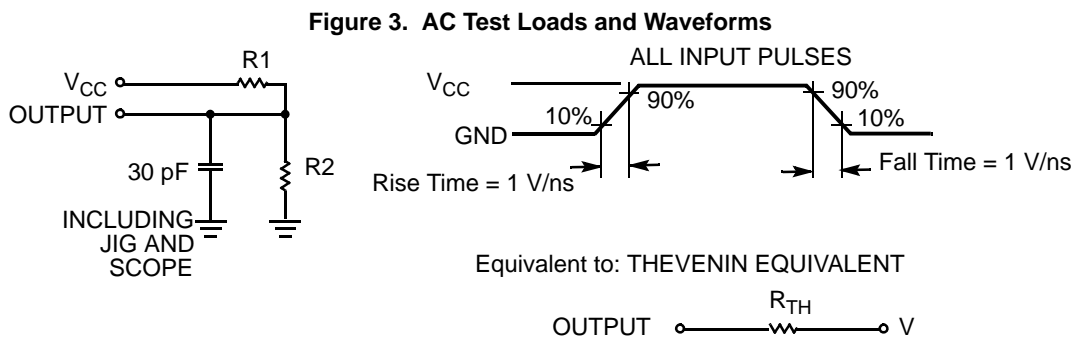
### Capacitance

Parameter <sup>[11]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	15	pF
C <sub>OUT</sub>	Output capacitance		15	pF

### Thermal Resistance

Parameter <sup>[11]</sup>	Description	Test Conditions	FBGA	TSOP I	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board	38.10	44.66	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		7.54	12.12	°C/W

### AC Test Loads and Waveforms



Parameter	2.5 V	3.3 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

**Note**

11. Tested initially and after any design or process changes that may affect these parameters.

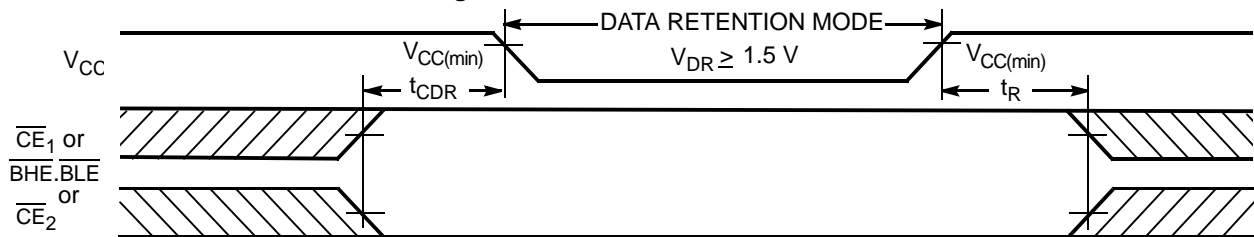
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[12]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.5	–	–	V
$I_{CCDR}$ <sup>[13]</sup>	Data retention current	$V_{CC} = 1.5\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ , or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	17	$\mu\text{A}$
$t_{CDR}$ <sup>[14]</sup>	Chip deselect to data retention time		0	–	–	ns
$t_R$ <sup>[15]</sup>	Operation recovery time		55	–	–	ns

## Data Retention Waveform

Figure 4. Data Retention Waveform<sup>[16]</sup>



### Notes

12. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .
13. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ),  $\overline{BYTE}$ , Address Pin  $A_{20}$  and Byte Enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) need to be tied to CMOS levels to meet the  $I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.
14. Tested initially and after any design or process changes that may affect these parameters.
15. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .
16.  $\overline{BHE}.\overline{BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Chip is deselected by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Over the Operating Range

Parameter [17, 18]	Description	55 ns		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read cycle time	55	–	ns
$t_{AA}$	Address to data valid	–	55	ns
$t_{OHA}$	Data hold from address change	6	–	ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to data valid	–	55	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to LOW Z [19]	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z [19, 20]	–	18	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Low Z [19]	10	–	ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to High Z [19, 20]	–	18	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to power up	0	–	ns
$t_{PD}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to power down	–	55	ns
$t_{DBE}$	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	55	ns
$t_{LZBE}$	$\overline{BLE}/\overline{BHE}$ LOW to Low Z [19]	10	–	ns
$t_{HZBE}$	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z [19, 20]	–	18	ns
<b>Write Cycle [21, 22]</b>				
$t_{WC}$	Write cycle time	55	–	ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to write end	40	–	ns
$t_{AW}$	Address setup to write end	40	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	40	–	ns
$t_{BW}$	$\overline{BLE}/\overline{BHE}$ LOW to write end	40	–	ns
$t_{SD}$	Data setup to write end	25	–	ns
$t_{HD}$	Data hold from Write End	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z [19, 20]	–	20	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z [19]	10	–	ns

### Notes

17. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
18. Test conditions for all parameters other than tristate parameters assume signal transition time of 1 V/ns, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in Figure 3 on page 5.
19. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
20.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
21. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
22. The minimum write pulse width for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be sum of  $t_{SD}$  and  $t_{HZWE}$ .



Switching Waveforms (continued)

Figure 7. Write Cycle 1 ( $\overline{WE}$  Controlled) [26, 27, 28, 29]

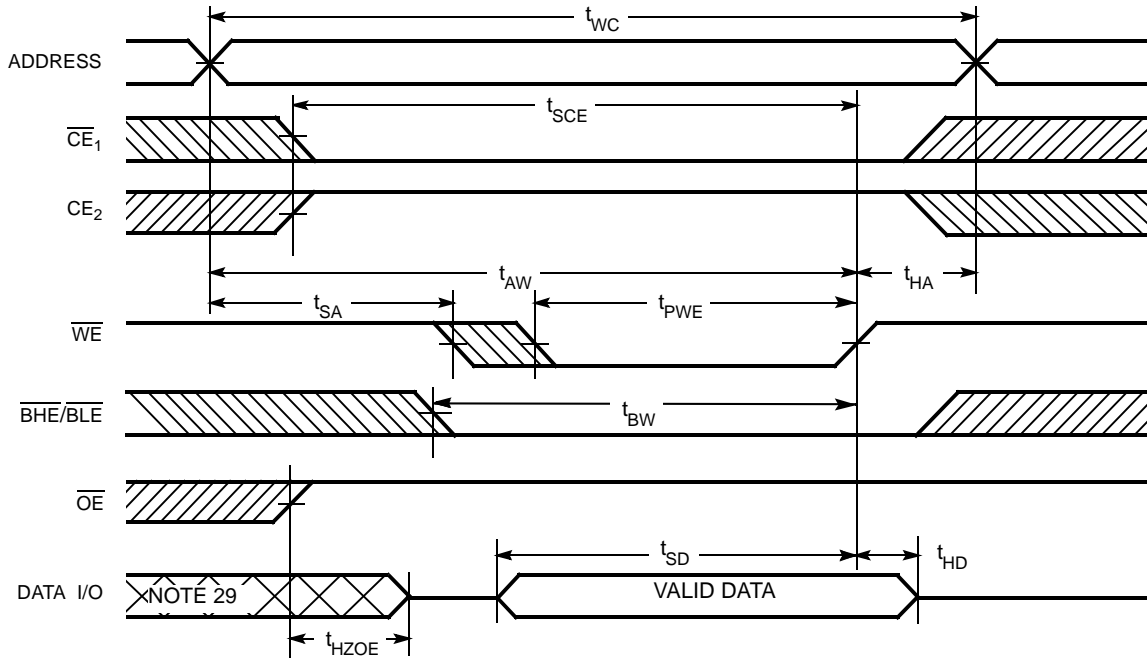
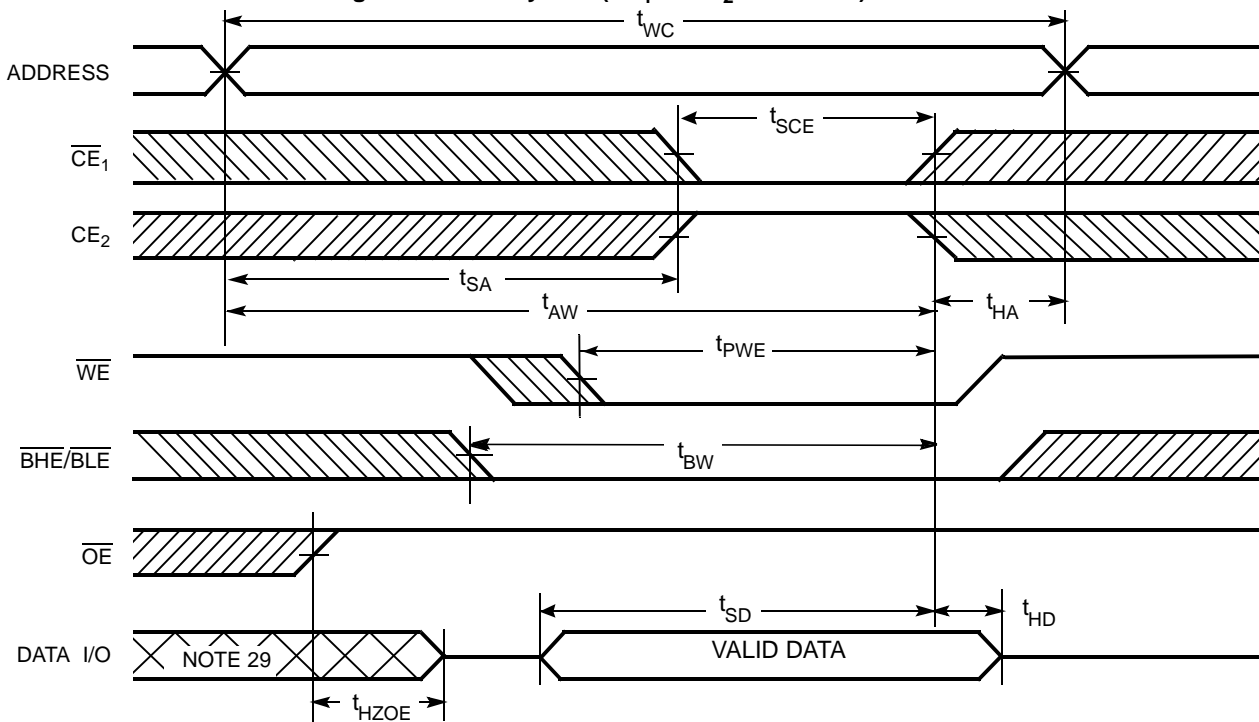


Figure 8. Write Cycle 2 ( $\overline{CE}_1$  or  $\overline{CE}_2$  Controlled) [26, 27, 28, 29]



Notes

- 26. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $\overline{CE}_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 27. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 28. If  $\overline{CE}_1$  goes HIGH and  $\overline{CE}_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 29. During this period the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 9. Write Cycle 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [30]

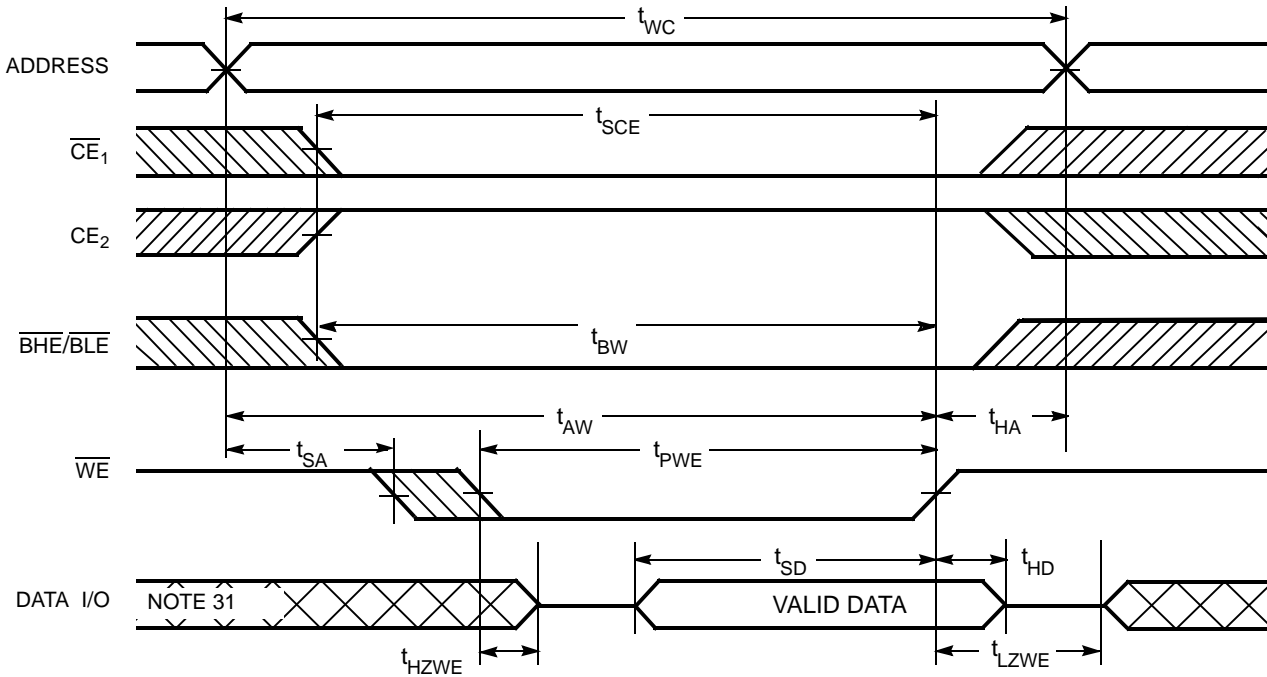
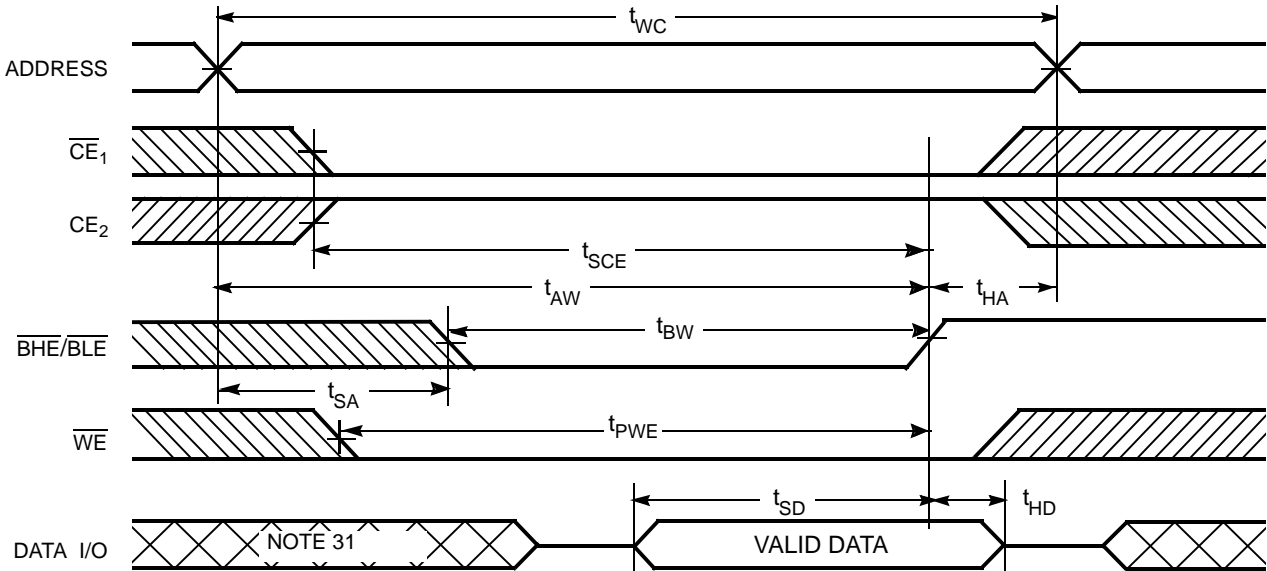


Figure 10. Write Cycle 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW) [30, 32]



Notes

- 30. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 31. During this period the I/Os are in output state and input signals should not be applied.
- 32. The minimum write pulse width for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) should be sum of  $t_{SD}$  and  $t_{HZWE}$ .

**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Input/Output	Mode	Power
H	X <sup>[33]</sup>	X	X	X <sup>[33]</sup>	X <sup>[33]</sup>	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
X <sup>[33]</sup>	L	X	X	X <sup>[33]</sup>	X <sup>[33]</sup>	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
X <sup>[33]</sup>	X <sup>[33]</sup>	X	X	H	H	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	High Z ( $I/O_8$ – $I/O_{15}$ ); Data Out ( $I/O_0$ – $I/O_7$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); High Z ( $I/O_0$ – $I/O_7$ )	Read	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	High Z ( $I/O_8$ – $I/O_{15}$ ); Data In ( $I/O_0$ – $I/O_7$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); High Z ( $I/O_0$ – $I/O_7$ )	Write	Active ( $I_{CC}$ )
L	H	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )

**Note**

33. The 'X' (Don't care) state for the chip enables and byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

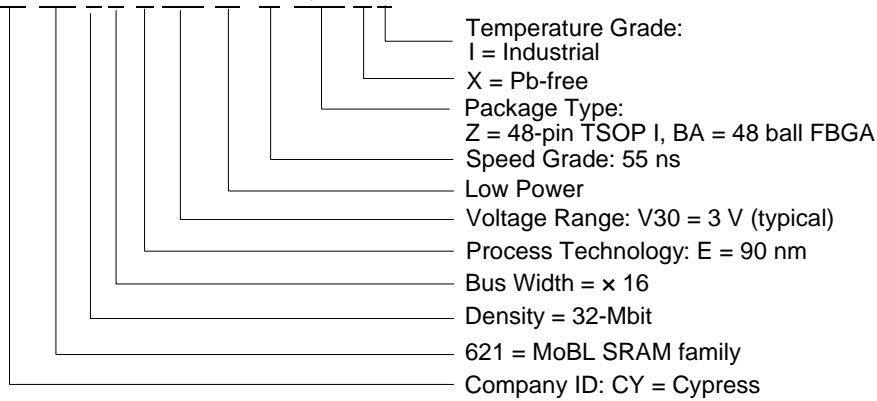
### Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62177EV30LL-55ZXI	51-85183	48-pin TSOP I (12 x 18.4 x 1 mm) Pb-free	Industrial
55	CY62177EV30LL-55BAXI	51-85191	48 ball FBGA (8 x 9.5 x 1.2 mm) Pb-free	Industrial

Contact your local Cypress sales representative for availability of these parts.

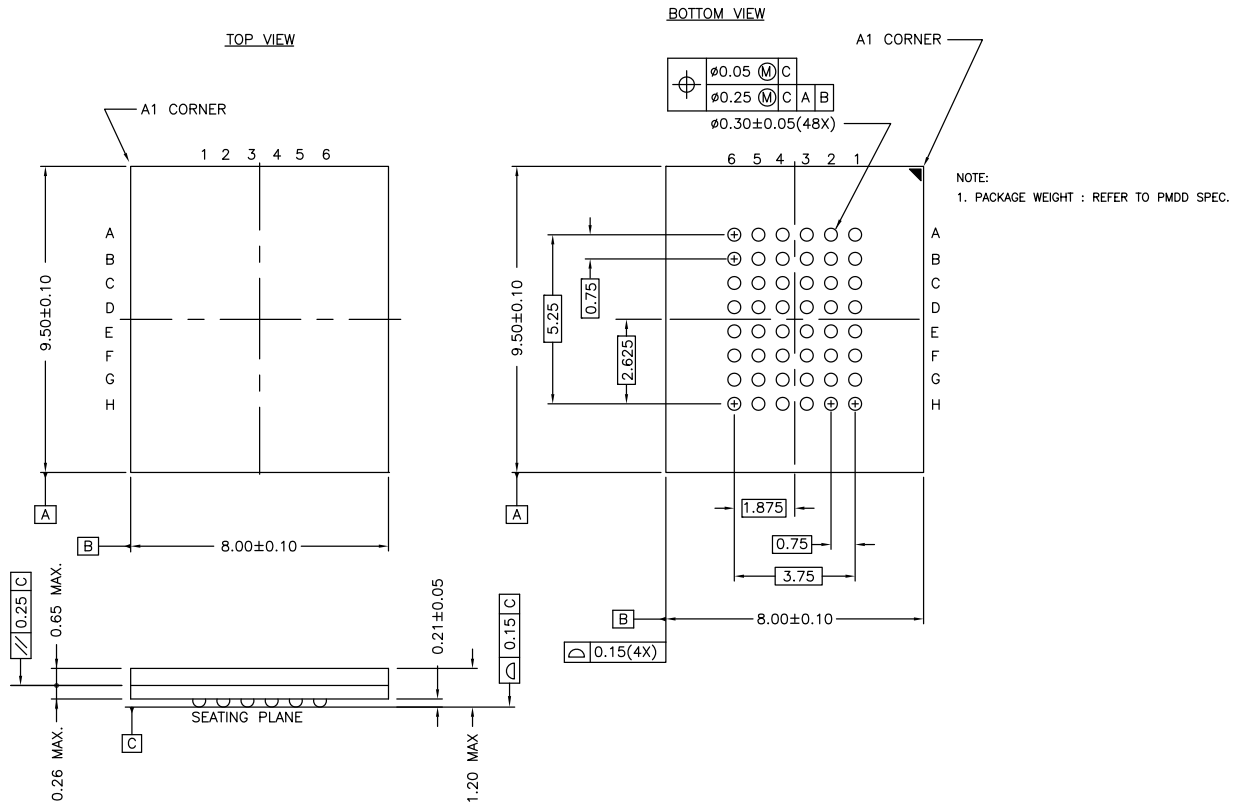
### Ordering Code Definitions

CY 621 7 7 E V30 LL -55 Z,BA X I



### Package Diagram

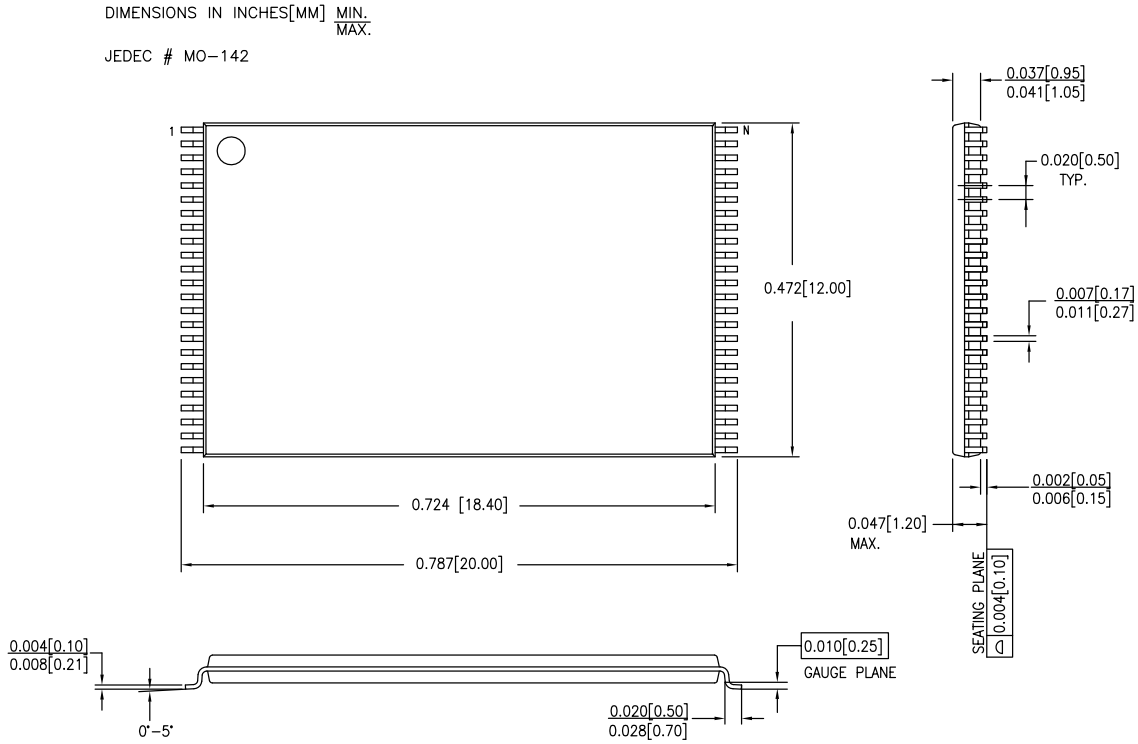
Figure 11. 48-ball FBGA (8 × 9.5 × 1.2 mm) BA48J Package Outline, 51-85191



51-85191 °C

Package Diagram (continued)

Figure 12. 48-pin TSOP I (12 x 18.4 x 1 mm) Z48A Package Outline, 51-85183



51-85183 \*C

## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

**Document History Page**

Document Title: CY62177EV30 MoBL <sup>®</sup> , 32-Mbit (2 M × 16 / 4 M × 8) Static RAM Document Number: 001-09880				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	498562	NXR	See ECN	New data sheet.
*A	2544845	VKN / PYRS	07/29/08	Removed 45 ns speed bin Added 70 ns speed bin Added 48-Pin TSOPI package Added footnote# 4 related to TSOPI package Added footnote# 9 related to I <sub>SB2</sub> and I <sub>CCDR</sub> Updated Ordering information table
*B	2589750	VKN / PYRS	10/15/08	Changed pin functions of pin# 10 from NC to A20 and pin# 13 from A20 to DNU in 48-Pin TSOPI package
*C	2668432	VKN / PYRS	03/03/09	Replaced 70 ns speed with 55 ns Extended the V <sub>CC</sub> range to 3.7 V Changed I <sub>CC (max)</sub> spec from 2.8 mA to 4.5 mA at f = 1 MHz Changed I <sub>CC (max)</sub> spec from 30 mA to 45 mA at f = f <sub>(max)</sub> Removed I <sub>SB1</sub> spec Changed I <sub>SB2 (max)</sub> spec from 17 μA to 25 μA Modified footnote #10
*D	2779867	VKN	10/06/09	Converted from Preliminary to Final Changed I <sub>CC (max)</sub> spec from 4.5 mA to 5.5 mA at f = 1 MHz Changed I <sub>CC (typ)</sub> spec from 2.2 mA to 4.5 mA at f = 1 MHz Changed I <sub>CC (typ)</sub> spec from 28 mA to 35 mA at f = f <sub>(max)</sub> Added V <sub>IL</sub> spec for TSOP I package and footnote# 10 Changed C <sub>OUT</sub> spec from 10 pF to 15 pF Included thermal specs Changed t <sub>OHA</sub> spec from 10ns to 6ns
*E	2899662	AJU	03/26/10	Removed inactive parts from Ordering Information. Updated Package Diagram
*F	2927528	VKN	05/04/2010	Included $\overline{\text{BHE}}$ , $\overline{\text{BLE}}$ in footnote #11 Added footnote #25 related to chip enable Added <a href="#">Contents</a> and <a href="#">Acronyms</a> Updated links in <a href="#">Sales, Solutions, and Legal Information</a>
*G	3177000	AJU	02/18/2011	Updated <a href="#">Features</a> (Removed FBGA package related information). Updated <a href="#">Pin Configurations</a> (Removed FBGA package related information). Corrected NC to DNU in footnote #2 Updated <a href="#">Electrical Characteristics</a> (Included $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ in I <sub>SB2</sub> test conditions to reflect Byte power down feature). Updated <a href="#">Thermal Resistance</a> (Removed FBGA package related information). Updated <a href="#">Data Retention Characteristics</a> (Included $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ in I <sub>CCDR</sub> test conditions to reflect Byte power down feature). Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Removed FBGA package related information in all instances in the document. Updated in new template.
*H	3295175	RAME	06/29/2011	Updated <a href="#">Package Diagram</a> . Updated Table of Contents. Removed reference to AN1064 SRAM system guidelines.
*I	3461953	TAVA	12/22/2011	Added <a href="#">Figure 2</a> and <a href="#">Figure 11</a> . Updated <a href="#">Ordering Information</a> and <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Thermal Resistance</a> Table.

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*J	4100342	VINI	08/21/2013	<p>Updated <a href="#">Switching Characteristics</a>: Added Note 17 and referred the same note in "Parameter" column.</p> <p>Updated <a href="#">Package Diagram</a>: spec 51-85191 – Changed revision from *B to *C.</p> <p>Updated in new template.</p> <p>Completing Sunset Review.</p>
*K	4111710	NILE	09/12/2013	<p>Updated <a href="#">Electrical Characteristics</a>: Updated Note 10.</p> <p>Updated <a href="#">Data Retention Characteristics</a>: Updated Note 13.</p>
*L	4355423	MEMJ	04/29/2014	<p>Updated <a href="#">Electrical Characteristics</a>: Updated Note 10 (Issue is fixed so pin A<sub>20</sub> can be left floating in standby).</p> <p>Updated <a href="#">Switching Characteristics</a>: Added Note 22 and referred the same note in Write Cycle (for t<sub>PWE</sub> parameter in WE Controlled, OE LOW condition).</p> <p>Updated <a href="#">Switching Waveforms</a>: Added Note 32 and referred the same note in <a href="#">Figure 10</a> (for t<sub>PWE</sub> parameter in WE Controlled, OE LOW condition).</p>
*M	4567826	VINI	11/12/2014	<p>Updated <a href="#">Features</a>: Included 48-ball FBGA package related information.</p> <p>Updated <a href="#">Functional Description</a>: Added "For a complete list of related resources, <a href="#">click here.</a>" at the end.</p> <p>Updated <a href="#">Maximum Ratings</a>: Referred Notes 4, 5 in "Supply voltage to ground potential".</p> <p>Completing Sunset Review.</p>

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