

## 74LCX02

# Low Voltage Quad 2-Input NOR Gate with 5V Tolerant Inputs

### Features

- 5V tolerant inputs
- 2.3V–3.6V  $V_{CC}$  specifications provided
- 5.2ns  $t_{PD}$  max. ( $V_{CC} = 3.3V$ ), 10 $\mu$ A  $I_{CC}$  max.
- Power down high impedance inputs and outputs
- $\pm 24mA$  output drive ( $V_{CC} = 3.0V$ )
- Implements proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds 500mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

### General Description


The LCX02 contains four 2-input NOR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX02 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

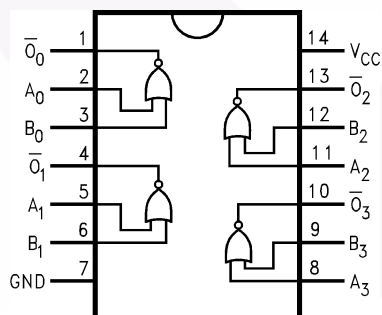
### Ordering Information

Order Number	Package Number	Package Description
74LCX02M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX02SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX02MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

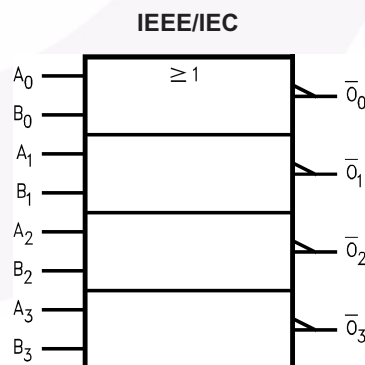
### Connection Diagram



### Pin Description

Pin Names	Description
$A_n, B_n$	Inputs
$\bar{O}_n$	Outputs

### Logic Symbol



## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	−0.5V to +7.0V
$V_I$	DC Input Voltage	−0.5V to +7.0V
$V_O$	DC Output Voltage, Output in HIGH or LOW State <sup>(1)</sup>	−0.5V to $V_{CC} + 0.5V$
$I_{IK}$	DC Input Diode Current, $V_I < GND$	−50mA
$I_{OK}$	DC Output Diode Current $V_O < GND$	−50mA
	$V_O > V_{CC}$	+50mA
$I_O$	DC Output Source/Sink Current	±50mA
$I_{CC}$	DC Supply Current per Supply Pin	±100mA
$I_{GND}$	DC Ground Current per Ground Pin	±100mA
$T_{STG}$	Storage Temperature	−65°C to +150°C

**Note:**

1.  $I_O$  Absolute Maximum Rating must be observed.

## Recommended Operating Conditions<sup>(2)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
$V_{CC}$	Supply Voltage Operating	2.0	3.6	V
	Data Retention	1.5	3.6	
$V_I$	Input Voltage	0	5.5	V
$V_O$	Output Voltage, HIGH or LOW State	0	$V_{CC}$	V
$I_{OH} / I_{OL}$	Output Current $V_{CC} = 3.0V-3.6V$		±24	mA
	$V_{CC} = 2.7V-3.0V$		±12	
	$V_{CC} = 2.3V-2.7V$		±8	
$T_A$	Free-Air Operating Temperature	−40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V

**Note:**

2. Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Max.	
V <sub>IH</sub>	HIGH Level Input Voltage	2.3–2.7		1.7		V
		2.7–3.6		2.0		
V <sub>IL</sub>	LOW Level Input Voltage	2.3–2.7			0.7	V
		2.7–3.6			0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	2.3–3.6	I <sub>OH</sub> = -100μA	V <sub>CC</sub> - 0.2		V
		2.3	I <sub>OH</sub> = -8mA	1.8		
		2.7	I <sub>OH</sub> = -12mA	2.2		
		3.0	I <sub>OH</sub> = -18mA	2.4		
			I <sub>OH</sub> = -24mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.3–3.6	I <sub>OL</sub> = 100μA		0.2	V
		2.3	I <sub>OL</sub> = 8mA		0.6	
		2.7	I <sub>OL</sub> = 12mA		0.4	
		3.0	I <sub>OL</sub> = 16mA		0.4	
			I <sub>OL</sub> = 24mA		0.55	
I <sub>I</sub>	Input Leakage Current	2.3–3.6	0 ≤ V <sub>I</sub> ≤ 5.5V		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	0	V <sub>I</sub> or V <sub>O</sub> = 5.5V		10	μA
I <sub>CC</sub>	Quiescent Supply Current	2.3–3.6	V <sub>I</sub> = V <sub>CC</sub> or GND		10	μA
			3.6V ≤ V <sub>I</sub> ≤ 5.5V		±10	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.3–3.6	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		500	μA

**AC Electrical Characteristics**

Symbol	Parameter	T <sub>A</sub> = −40°C to +85°C, R <sub>L</sub> = 500Ω						Units
		V <sub>CC</sub> = 3.3V ± 0.3V, C <sub>L</sub> = 50pF		V <sub>CC</sub> = 2.7V, C <sub>L</sub> = 50pF		V <sub>CC</sub> = 2.5V ± 0.2V, C <sub>L</sub> = 30pF		
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	1.5	5.2	1.5	6.0	1.5	6.2	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew <sup>(3)</sup>		1.0					ns

**Note:**

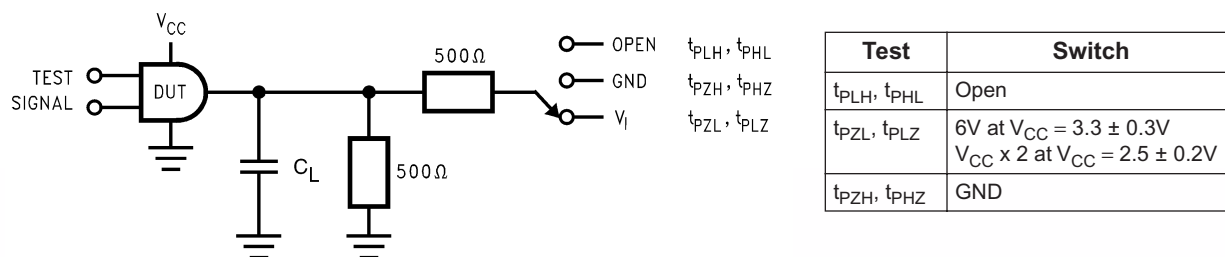
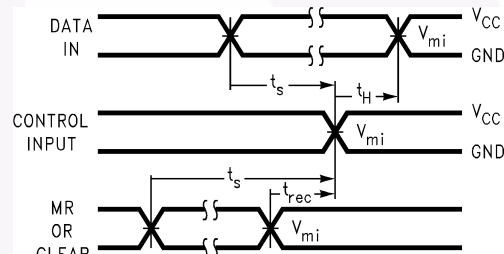
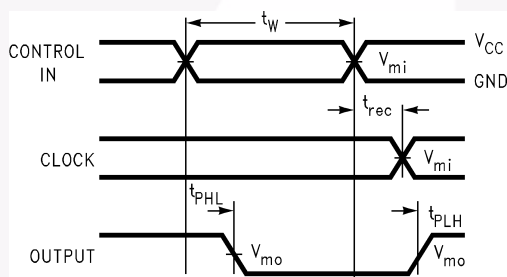
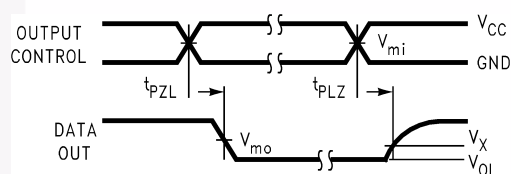
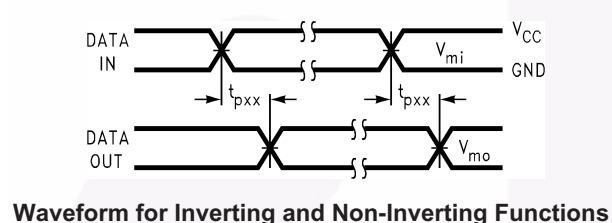
3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

**Dynamic Switching Characteristics**

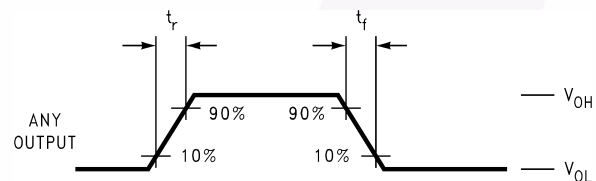
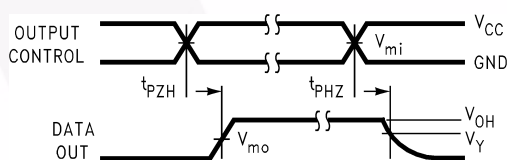
Symbol	Parameter	$V_{CC}$ (V)	Conditions	$T_A = 25^\circ\text{C}$	Unit
				Typical	
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$	3.3	$C_L = 50\text{pF}$ , $V_{IH} = 3.3\text{V}$ , $V_{IL} = 0\text{V}$	0.8	V
		2.5	$C_L = 30\text{pF}$ , $V_{IH} = 2.5\text{V}$ , $V_{IL} = 0\text{V}$	0.6	
$V_{OLV}$	Quiet Output Dynamic Valley $V_{OL}$	3.3	$C_L = 50\text{pF}$ , $V_{IH} = 3.3\text{V}$ , $V_{IL} = 0\text{V}$	-0.8	V
		2.5	$C_L = 30\text{pF}$ , $V_{IH} = 2.5\text{V}$ , $V_{IL} = 0\text{V}$	-0.6	

**Capacitance**

Symbol	Parameter	Conditions	Typical	Units
$C_{IN}$	Input Capacitance	$V_{CC} = \text{Open}$ , $V_I = 0\text{V}$ or $V_{CC}$	7	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 3.3\text{V}$ , $V_I = 0\text{V}$ or $V_{CC}$	8	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CC} = 3.3\text{V}$ , $V_I = 0\text{V}$ or $V_{CC}$ , $f = 10\text{MHz}$	25	pF

**AC Loading and Waveforms** (Generic for LCX Family)Figure 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms

Setup Time, Hold Time and Recovery Time for Logic



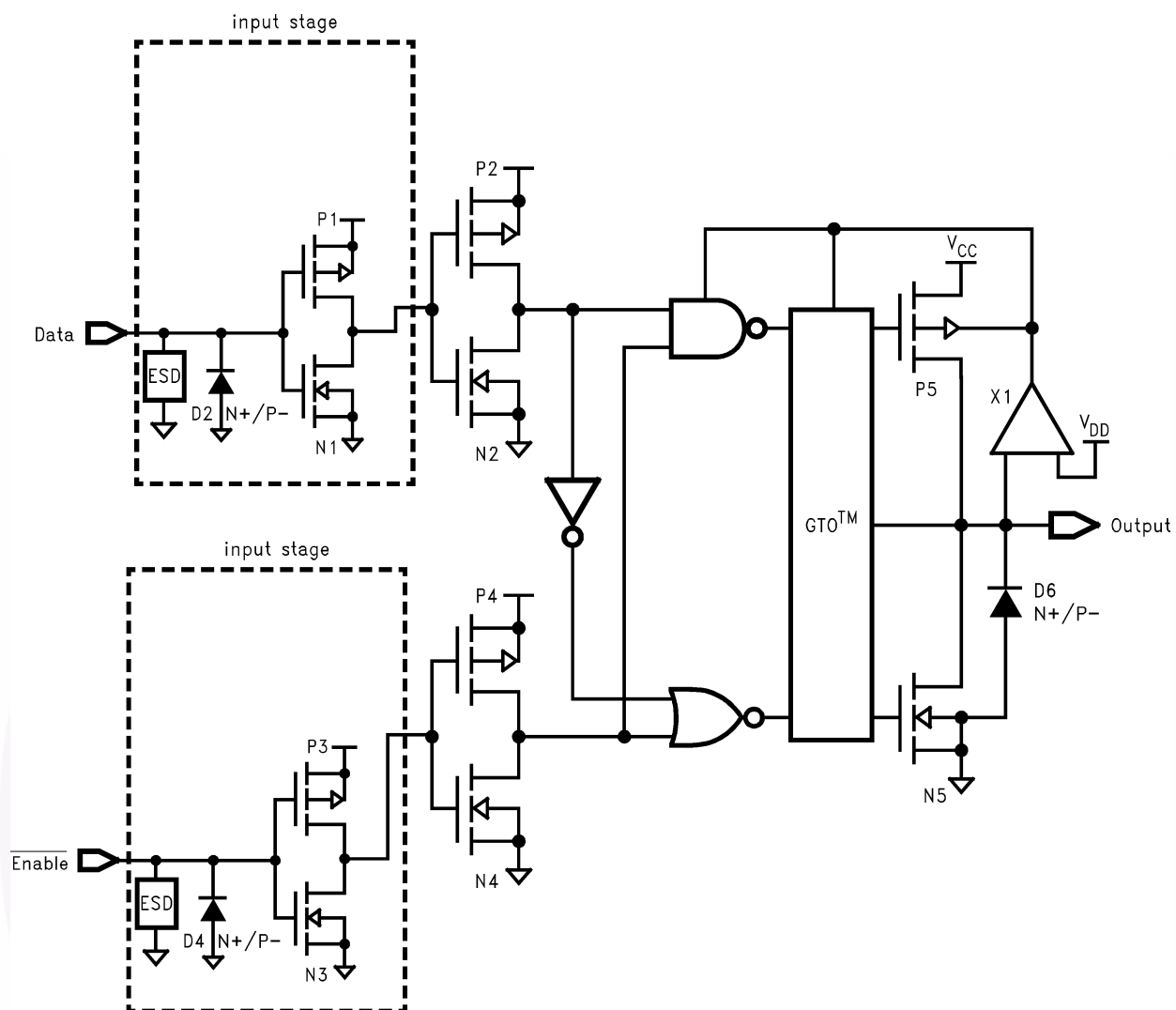
3-STATE Output Low Enable and Disable Times for Logic

 $t_{rise}$  and  $t_{fall}$ 

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Figure 2. Waveforms (Input Characteristics;  $f = 1MHz$ ,  $t_r = t_f = 3ns$ )

# **Schematic Diagram** (Generic for LCX Family)



## Physical Dimensions

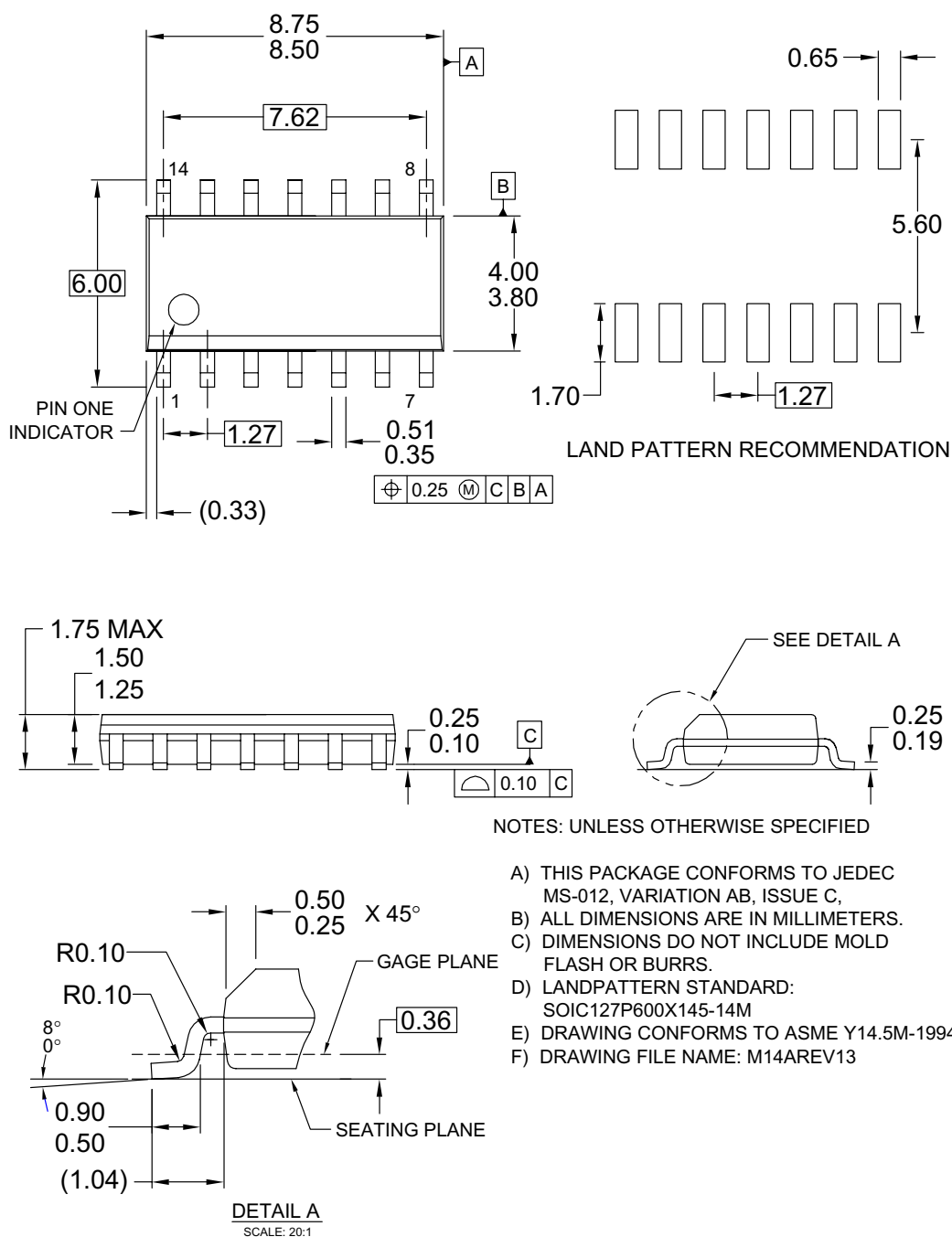


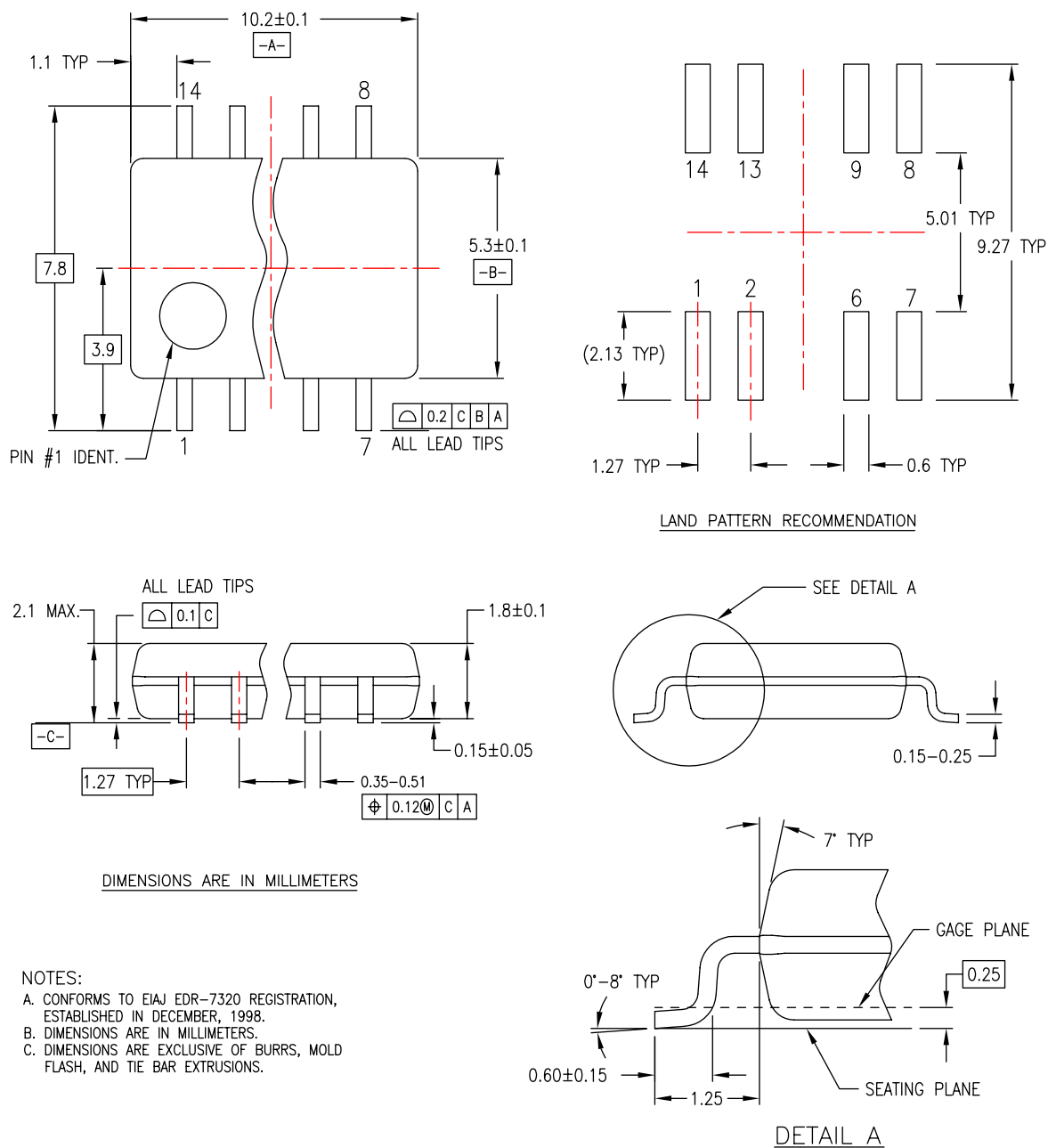
Figure 3. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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## Physical Dimensions (Continued)



M14DREVC

Figure 4. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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## Physical Dimensions (Continued)

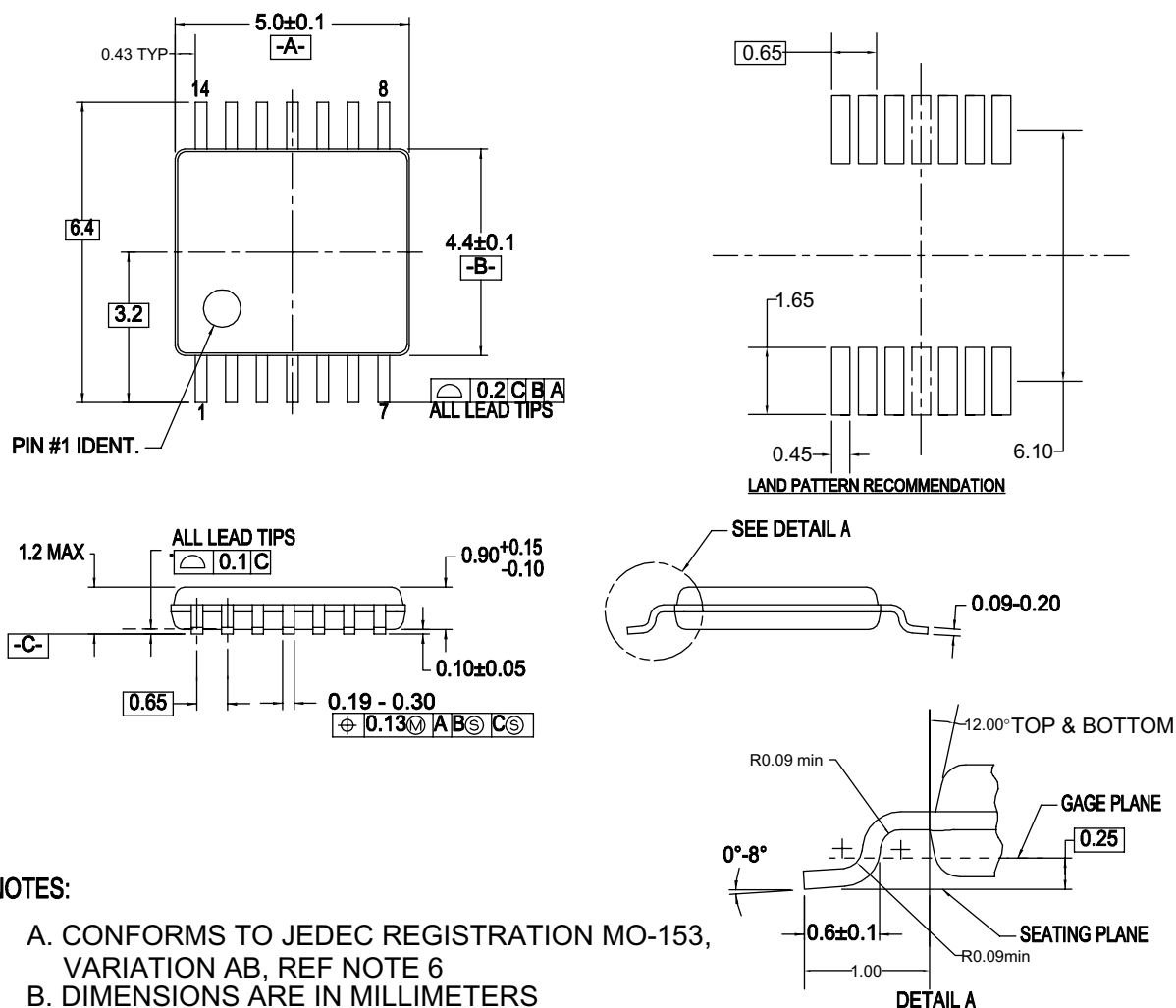


Figure 5. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Rev. I33

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