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STK551U362A-E

Thick-Film Hybrid IC

Inverter Power H-IC for 3-phase Motor Drive

Overview

This “Inverter Power H-IC” is highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single SIP module (Single-In line Package). Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.

Function

- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control input and status output are at low voltage levels directly compatible with microcontrollers
- Built-in dead time for shoot-thru protection
- Externally accessible embedded thermistor for substrate temperature measurement
- The level of the over-current protection current is adjustable with the external resistor, “RSD”

Certification

- UL1557 (File Number : E339285).

Specifications

Absolute Maximum Ratings at $T_c = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VCC	V+ to V-, surge < 500V *1	450	V
Collector-emitter voltage	VCE	V+ to U,V,W or U,V,W to V-	600	V
Output current	Io	V+, V-, U,V,W terminal current	±10	A
		V+, V-, U,V,W terminal current at $T_c = 100^\circ\text{C}$	±5	A
Output peak current	Iop	V+, V-, U,V,W terminal current for a Pulse width of 1ms.	±20	A
Pre-driver voltage	VD1,2,3,4	VB1 to U, VB2 to V, VB3 to W, VDD to VSS *2	20	V
Input signal voltage	VIN	HIN1, 2, 3, LIN1, 2, 3	-0.3 to VDD	V
FAULT terminal voltage	VFAULT	FAULT terminal	-0.3 to VDD	V
Maximum power dissipation	Pd	IGBT per channel	30	W
Junction temperature	Tj	IGBT,FRD	150	°C
Storage temperature	Tstg		-40 to +125	°C
Operating case temperature	Tc	H-IC case temperature	-40 to +100	°C
Tightening torque		Case mounting screws *3	1.0	Nm
Withstand voltage	Vis	50Hz sine wave AC 1 minute *4	2000	VRMS

Reference voltage is “VSS” terminal voltage unless otherwise specified.

*1: Surge voltage developed by the switching operation due to the wiring inductance between + and U-(V-, W-) terminal.

*2: Terminal voltage: VD1=VB1-U, VD2=VB2-V, VD3=VB3-W, VD4=VDD-VSS

*3: Flatness of the heat-sink should be 0.15mm and below.

*4: Test conditions : AC2500V, 1 second.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

STK551U362A-E

Electrical Characteristics at Tc = 25°C, VD1, VD2, VD3, VD4 = 15V

Parameter	Symbol	Conditions		Test circuit	Ratings			Unit
					min	typ	max	
Power output section								
Collector-emitter cut-off current	ICE	VCE = 600V		Fig.1	-	-	0.1	mA
Bootstrap diode reverse current	IR(BD)	VR(BD)			-	-	0.1	mA
Collector to emitter saturation voltage	VCE(SAT)	Io = 10A Tj = 25°C	Upper side	Fig.2	-	1.8	2.4	V
			Lower side *1		-	2.1	2.7	
		Io = 5A Tj = 100°C	Upper side		-	1.3	-	
			Lower side *1		-	1.6	-	
Diode forward voltage	VF	Io = 10A Tj = 25°C	Upper side	Fig.3	-	1.8	2.3	V
			Lower side *1		-	2.1	2.6	
		Io = 5A Tj = 100°C	Upper side		-	1.3	-	
			Lower side *1		-	1.6	-	
Junction to case thermal resistance	θj-c(T)	IGBT			-	-	4	°C/W
	θj-c(D)	FRD			-	-	5	
Control (Pre-driver) section								
Pre-driver power dissipation	ID	VD1, 2, 3 = 15V		Fig.4	-	0.08	0.4	mA
		VD4 = 15V			-	1.6	4	
High level Input voltage	Vin H	HIN1, HIN2, HIN3, LIN1, LIN2, LIN3 to VSS			2.5	-	-	V
Low level Input voltage	Vin L				-	-	0.8	V
Input threshold voltage hysteresis*1	Vinth(hys)				0.5	0.8	-	V
Logic 1 input leakage current	IIN+	VIN = +3.3V			-	100	143	μA
Logic 0 input leakage current	IIN-	VIN = 0V			-	-	2	μA
FAULT terminal input electric current	IoSD	FAULT : ON/VFAULT = 0.1V			-	2	-	mA
FAULT clear time	FLTCLR	Fault output latch time.			18	-	80	ms
VCC and VS undervoltage positive going threshold.	VCCUV+ VSUV+				10.5	11.1	11.7	V
VCC and VS undervoltage negative going threshold.	VCCUV- VSUV-				10.3	10.9	11.5	V
VCC and VS undervoltage hysteresis	VCCUVH VSUVH-				0.14	0.2	-	A
Over current protection level	ISD	PW = 100μs, RSD = 0Ω		Fig.5	18.1	-	22.9	A
Output level for current monitor	ISO	Io = 10A			0.31	0.33	0.35	V
Thermistor for substrate temperature	Rt	Thermistor Resistance at 25°C (Vth)			90	100	110	kΩ

Reference voltage is “VSS” terminal voltage unless otherwise specified.

*1: The lower side's VCE(SAT) and VF include a loss by the shunt resistance

Parameter	Symbol	Conditions	Test circuit	Ratings			Unit
				min	typ	max	
Switching Character							
Switching time	tON	Io = 10A	Fig.6	0.3	0.6	1.3	μs
	tOFF	Inductive load		-	1.0	1.8	
Turn-on switching loss	Eon	Ic = 5A, V ⁺ = 300V,		-	100	-	μJ
Turn-off switching loss	Eoff	VDD = 15V, L = 3.9mH		-	110	-	μJ
Total switching loss	Etot	Tc = 25°C		-	210	-	μJ
Turn-on switching loss	Eon	Ic = 5A, V ⁺ = 300 V,		-	110	-	μJ
Turn-off switching loss	Eoff	VDD = 15V, L = 3.9mH		-	230	-	μJ
Total switching loss	Etot	Tc = 100°C		-	340	-	μJ
Diode reverse recovery energy	Erec	IF = 5A, V ⁺ = 400V, VDD = 15V,		-	10	-	μJ
Diode reverse recovery time	Trr	L = 3.9mH, Tc = 100°C		-	50	-	ns
Reverse bias safe operating area	RBSOA	Io = 20A, VCE = 450V		Full square			
Short circuit safe operating area	SCSOA	VCE = 400V, Tc = 100°C		4	-	-	μs
Allowable offset voltage slew rate	dv/dt	Between U,V,W to U-,V-,W-		-50	-	50	V/ns

Reference voltage is “VSS” terminal voltage unless otherwise specified.

Notes:

- When the internal protection circuit operates, a Fault signal is turned ON (When the Fault terminal is low level, Fault signal is ON state : output form is open DRAIN) but the Fault signal does not latch. After protection operation ends, it returns automatically within about 18ms to 80ms and resumes operation beginning condition. So, after Fault signal detection, set all input signals to OFF (Low) at once. However, the operation of pre-drive power supply low voltage protection (UVLO: with hysteresis about 0.2V) is as follows.

Upper side:

The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn ‘low’.

Lower side:

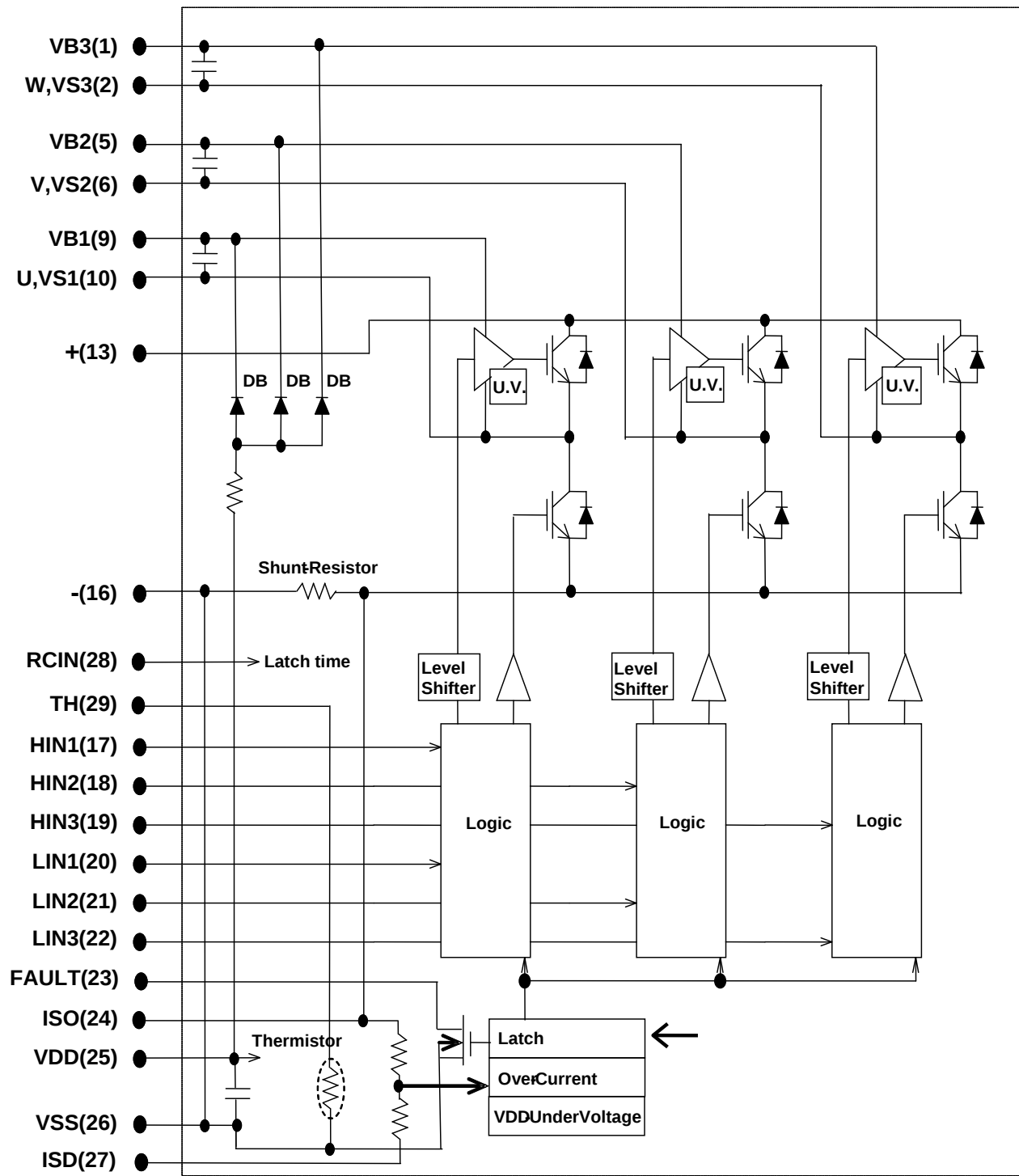
The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.

- When assembling the H-IC on the heat sink with M3 type screw, tightening torque range is 0.6 Nm to 0.9 Nm.
- The pre-drive low voltage protection is the feature to protect devices when the pre-driver supply voltage falls due to an operating malfunction.

Module Pin-Out Description

Pin	Name	Description
1	VB3	High Side Floating Supply Voltage 3
2	W, VS3	Output 3 - High Side Floating Supply Offset Voltage
3	—	Without Pin
4	—	Without Pin
5	VB2	High Side Floating Supply voltage 2
6	V, VS2	Output 2 - High Side Floating Supply Offset Voltage
7	—	Without Pin
8	—	Without Pin
9	VB1	High Side Floating Supply voltage 1
10	U, VS1	Output 1 - High Side Floating Supply Offset Voltage
11	—	Without Pin
12	—	none
13	V+	Positive Bus Input Voltage
14	NA	none
15	NA	none
16	V-	Negative Bus Input Voltage
17	HIN1	Logic Input High Side Gate Driver - Phase 1
18	HIN2	Logic Input High Side Gate Driver - Phase V
19	HIN3	Logic Input High Side Gate Driver - Phase W
20	LIN1	Logic Input Low Side Gate Driver - Phase U
21	LIN2	Logic Input Low Side Gate Driver - Phase V
22	LIN3	Logic Input Low Side Gate Driver - Phase W
23	FLTEN	Enable input / Fault output
24	ISO	Current monitor output
25	VDD	+15V Main Supply
26	VSS	Negative Main Supply
27	ISD	Over current detection and setting
28	RCIN	Fault clear time setting output
29	TH	Thermistor output

Equivalent Block Diagram



Test Circuit

(The tested phase : U+ shows the upper side of the U phase and U- shows the lower side of the U phase.)

■ ICE / IR(BD)

	U+	V+	W+	U-	V-	W-
M	13	13	13	10	6	2
N	10	6	2	16	16	16

	U(BD)	V(BD)	W(BD)
M	9	5	1
N	26	26	26

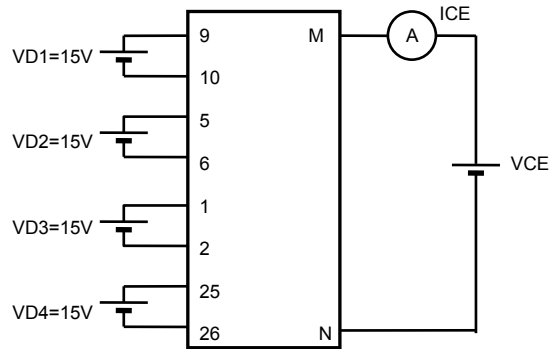


Fig. 1

■ VCE(SAT) (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	13	13	13	10	6	2
N	10	6	2	16	16	16
m	17	18	19	20	21	22

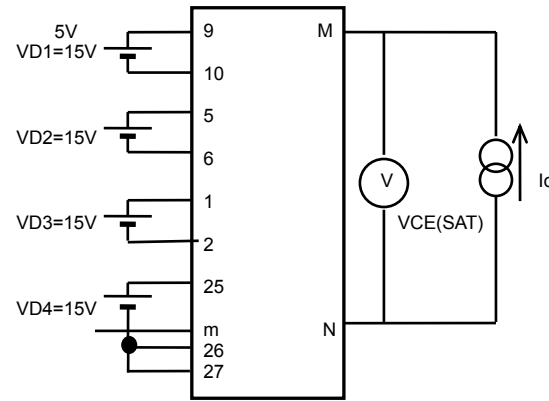


Fig. 2

■ VF (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	13	13	13	10	6	2
N	10	6	2	16	16	16

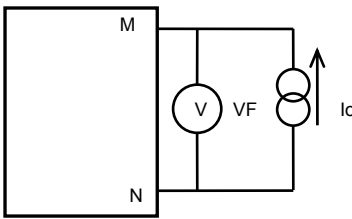


Fig. 3

■ ID

	VD1	VD2	VD3	VD4
M	9	5	1	25
N	10	6	2	26

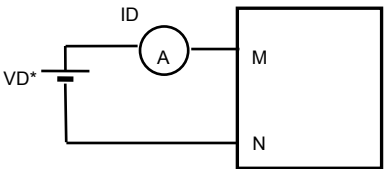


Fig. 4

■ ISD

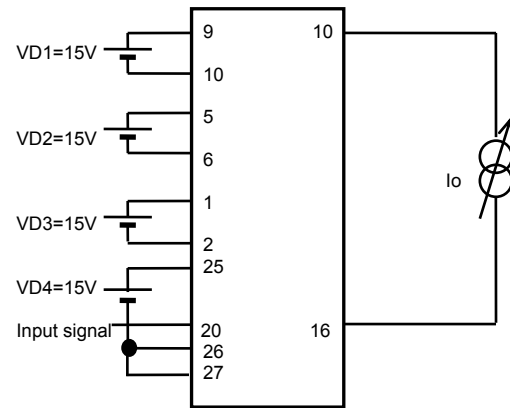
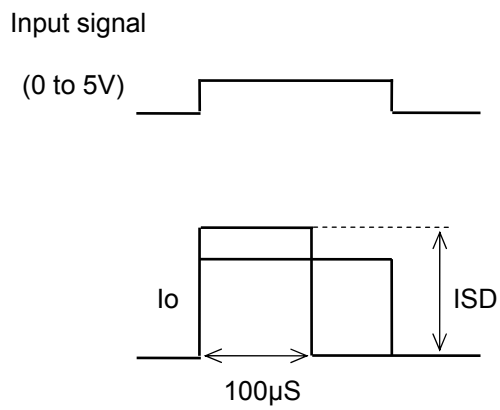


Fig. 5

■ Switching time (The circuit is a representative example of the lower side U phase.)

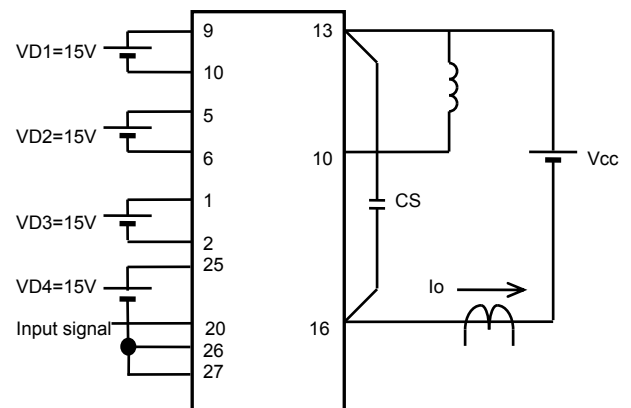
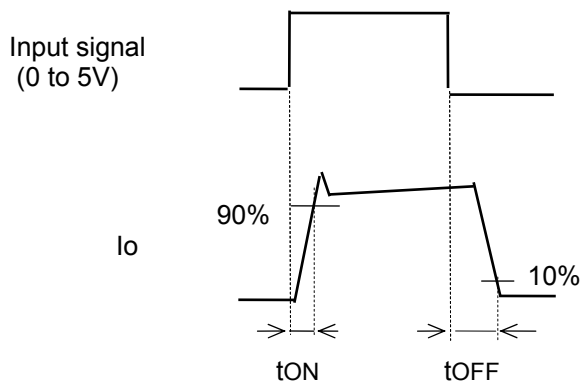


Fig. 6

Logic Timing Chart

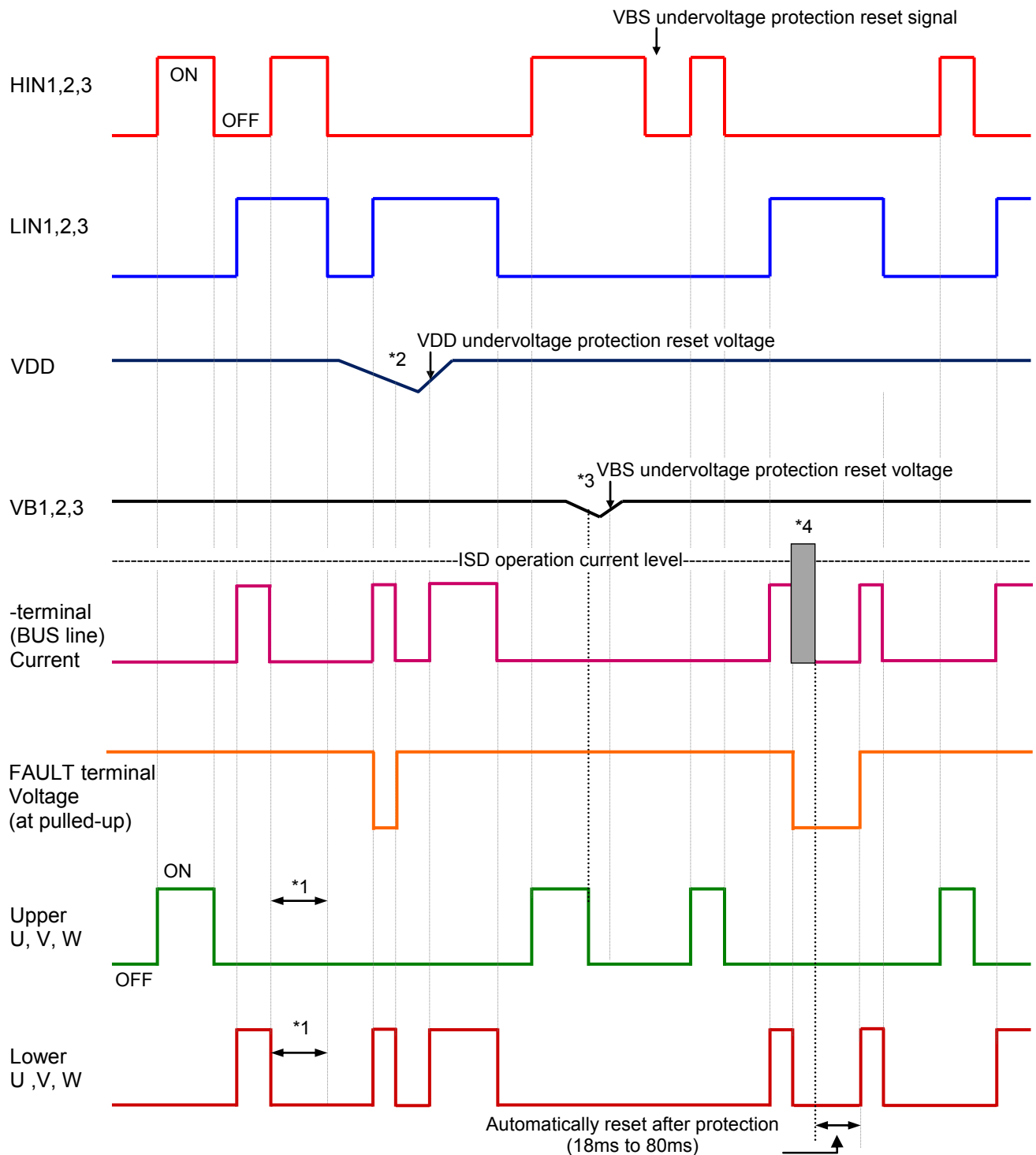
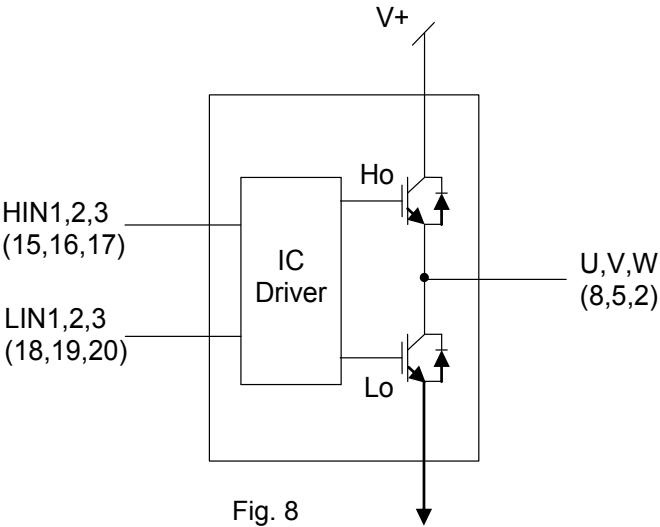


Fig. 7

Notes

- *1 : Diagram shows the prevention of shoot-through via control logic. More dead time to account for switching delay needs to be added externally.
- *2 : When VDD decreases all gate output signals will go low and cut off all of 6 IGBT outputs. part. When VDD rises the operation will resume immediately.
- *3 : When the upper side gate voltage at VB1, VB2 and VB3 drops only, the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gat voltage rises.
- *4 : In case of over current detection, all IGBT's are turned off and the FAULT output is asserted. Normal operation resumes in 18 to 80ms after the over current condition is removed.

Logic level table



FLTEN	Itrip	HIN1,2,3	LIN1,2,3	U,V,W
1	0	1	0	Vbus
1	0	0	1	0
1	0	0	0	Off
1	0	1	1	Off
1	1	X	X	Off
0	X	X	X	Off

Sample Application Circuit

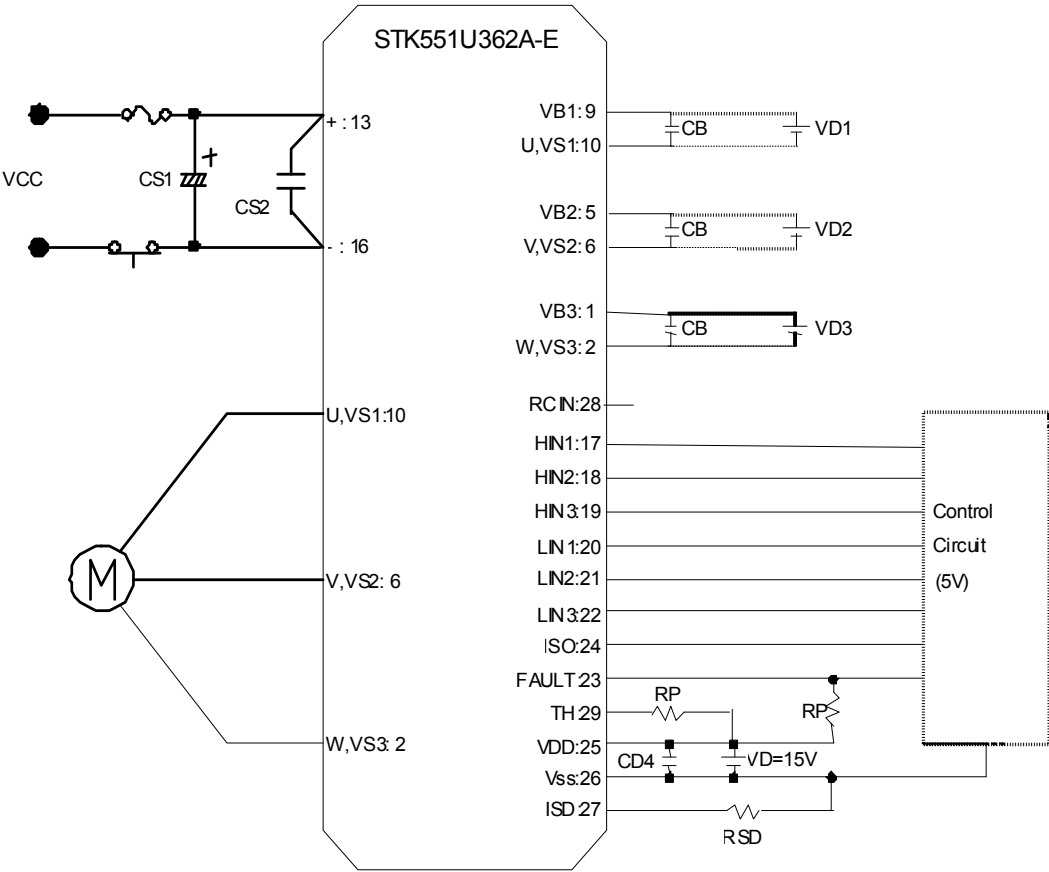


Fig. 9

Recommended Operating Conditions at T_c = 25°C

Item	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	VCC	+ to U-(V-,W-)	0	280	450	V
Pre-driver supply voltage	VD1,2,3	VB1 to U, VB2 to V, VB3 to W	12.5	15	17.5	V
	VD4	VDD to VSS *1	13.5	15	16.5	
ON-state input voltage	VIN(ON)	HIN1, HIN2, HIN3,	3.0	-	5.0	V
OFF-state input voltage	VIN(OFF)	LIN1, LIN2, LIN3	0	-	0.3	
PWM frequency	fPWM		1	-	20	kHz
Dead time	DT	Turn-off to turn-on	1.5	-	-	μs
Allowable input pulse width	PWIN	ON and OFF	1	-	-	μs
Tightening torque		'M3' type screw	0.6	-	0.9	Nm

*1 Pre-drive power supply (VD4=15±1.5V) must be have the capacity of I_o=20mA(DC), 0.5A(Peak).

Usage Precautions

1. This H-IC includes bootstrap diode and resistors. Therefore, by adding a capacitor “CB”, a high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47μF, however this value needs to be verified prior to production. If selecting the capacitance more than 47μF (±20%), connect a resistor (about 20Ω) in series between each 3-phase upper side power supply terminals (VB1,2,3) and each bootstrap capacitor. When not using the bootstrap circuit, each upper side pre-drive power supply requires an external independent power supply.
2. It is essential that wiring length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of “CS” is in the range of 0.1 to 10μF.
3. “ISO” (pin24) is terminal for current monitor. When the pull-down resistor is used, please select it more than 5.6kΩ
4. “FAULT” (pin23) is open DRAIN output terminal. (Active Low). Pull up resistor is recommended more than 5.6kΩ.
5. Inside the H-IC, a thermistor used as the temperature monitor for internal substrate is connected between VSS terminal and TH terminal, therefore, an external pull up resistor connected between the TH terminal and an external power supply should be used. The temperature monitor example application is as follows, please refer the Fig.10, and Fig.11 below.
6. pull down resistor of 33kΩ is provided internally at the signal input terminals. An external resistor of 2.2k to 3.3kΩ should be added to reduce the influence of external wiring noise.
7. The over-current protection feature is not intended to protect in exceptional fault condition. An external fuse is recommended for safety.
8. When “-” and “VSS” terminal are short-circuited on the outside, level that over-current protection (ISD) might be changed from designed value as H-IC. Please check it in your set (“N” terminal and “VSS” terminal are connected in H-IC).
9. The over-current protection function operates normally when an external resistor RSD is connected between ISD and VSS terminals. Be sure to connect this resistor. The level of the overcurrent protection can be changed according to the RSD value.
10. When input pulse width is less than 1.0μs, an output may not react to the pulse. (Both ON signal and OFF signal)

This data shows the example of the application circuit, does not guarantee a design as the mass production set.

The characteristic of thermistor

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resistance	R_{25}	$T_c = 25^{\circ}\text{C}$	97	100	103	k Ω
Resistance	R_{100}	$T_c = 100^{\circ}\text{C}$	4.93	5.38	5.88	k Ω
B-Constant (25 to 50 $^{\circ}\text{C}$)	B		4165	4250	4335	k
Temperature Range			-40	-	+125	$^{\circ}\text{C}$

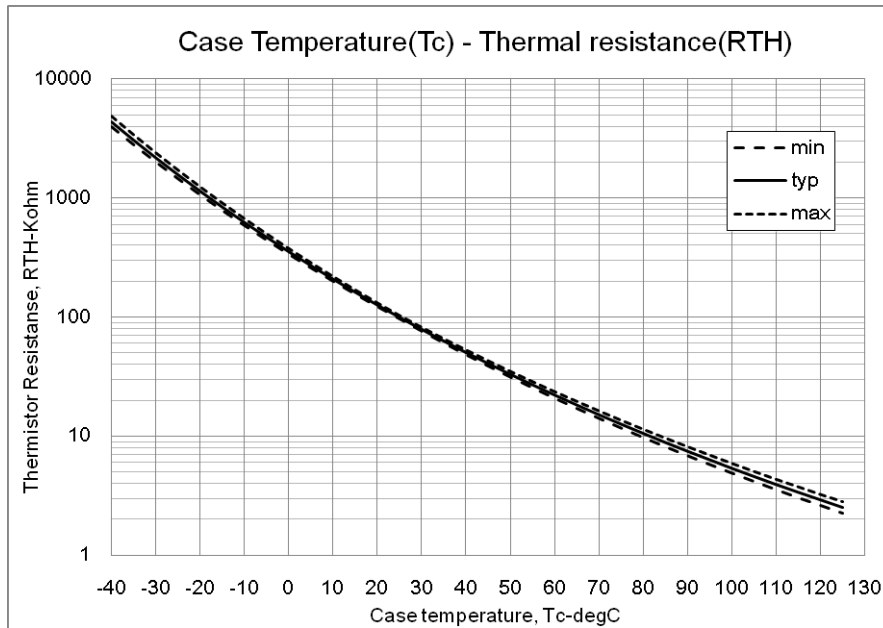


Fig. 10

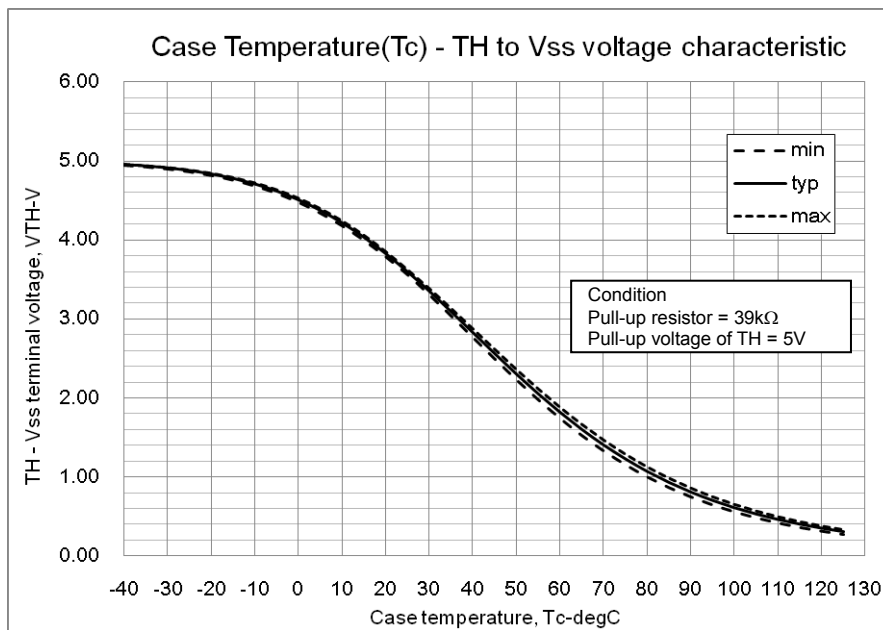


Fig. 11

The characteristic of PWM switching frequency

Maximum sinusoidal phase current as function of switching frequency (VBUS=400V, Tc=100°C)

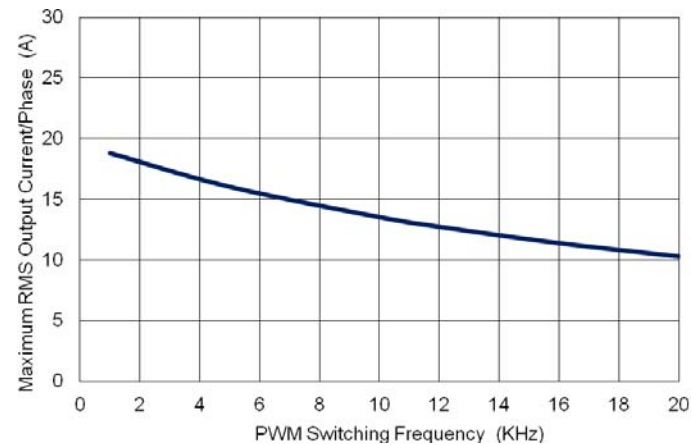


Fig.12

Switching waveform

IGBT Turn-on. Typical turn-on waveform @Tc=100deg, VBUS=400V

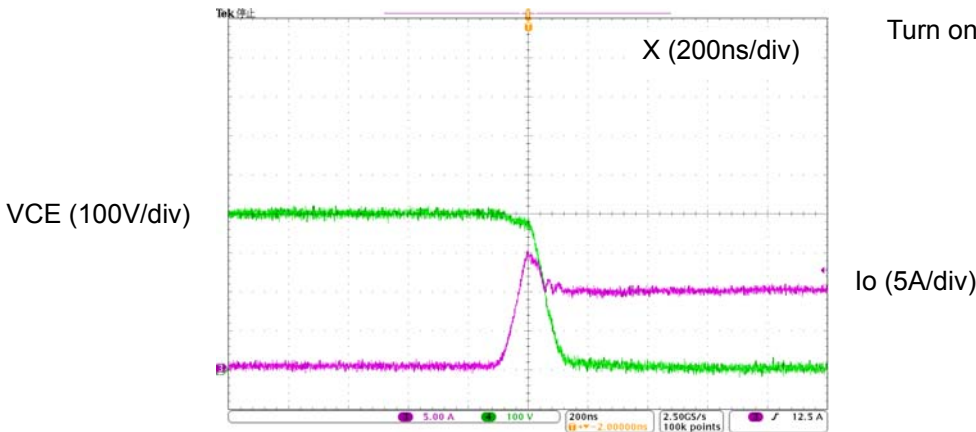


Fig. 13

IGBT Turn-off. Typical turn-off waveform @Tc=100deg, VBUS=400V

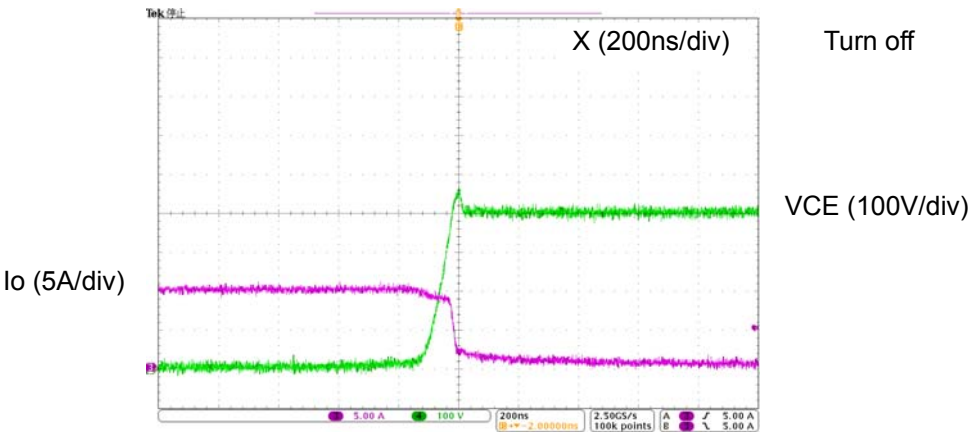


Fig. 14

CB capacitor value calculation for bootstrap circuit

Calculate condition

Item	Symbol	Value	Unit
Upper side power supply.	VBS	15	V
Total gate charge of output power IGBT at 15V.	Qg	89	nC
Upper side power supply low voltage protection.	UVLO	12	V
Upper side power dissipation.	IDmax	400	μA
ON time required for CB voltage to fall from 15V to UVLO	Ton-max	-	s

Capacitance calculation formula

CB must not be discharged below to the upper limit of the UVLO - the maximum allowable on-time (Ton-max) of the upper side is calculated as follows:

$$VBS * CB - Qg - IDmax * Ton-max = UVLO * CB$$

$$CB = (Qg + IDmax * Ton-max) / (VBS - UVLO)$$

The relationship between Ton-max and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47μF, however, the value needs to be verified prior to production.

Tonmax-Cb characteristic

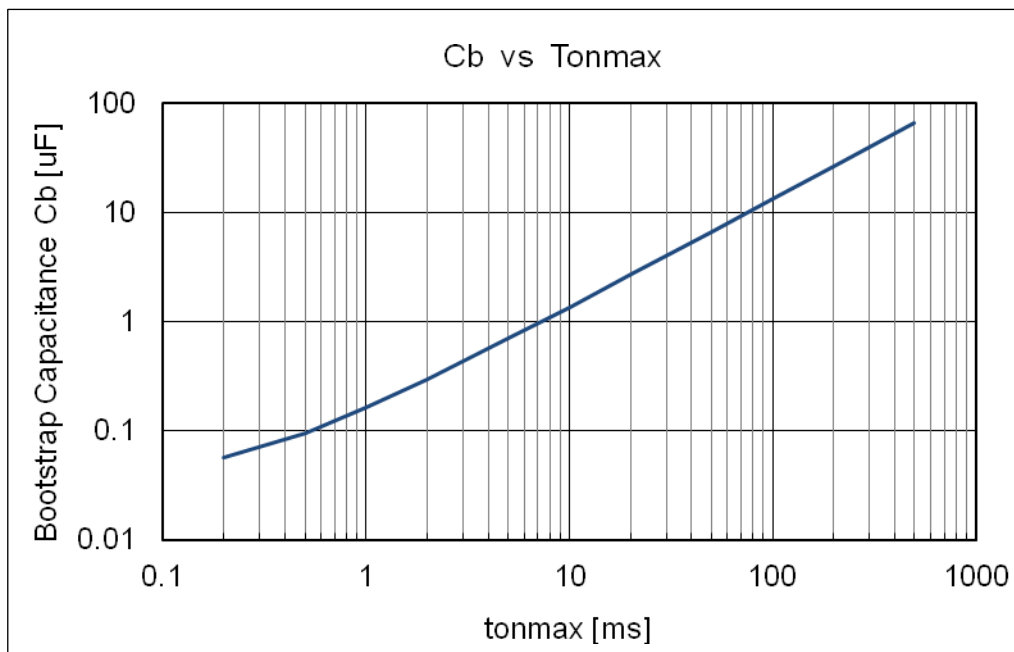
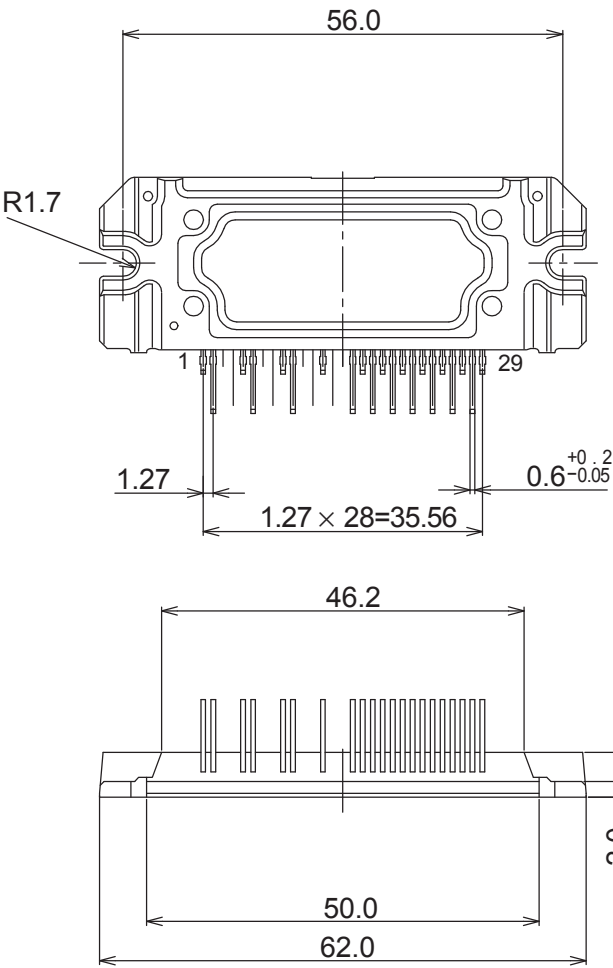


Fig 15

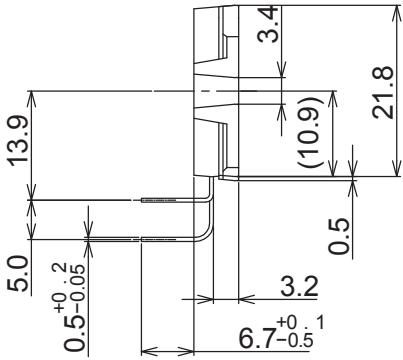
Package Dimensions

(unit : mm)

SIP29 56x21.8
CASE 127BW
ISSUE O



missing pin : 3,4,7,8,11,12,14,15



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK551U362A-E	SIP29 56x21.8 (Pb-Free)	8 / Tube

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