BLF7G22L-100P; BLF7G22LS-100P

Power LDMOS transistor

Rev. 3 — 2 January 2012 — Product data sheet

1. Product profile

1.1 General description

100 W LDMOS power transistor for base station applications at frequencies from 2000 MHz to 2200 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Test signal	f (MHz)	I_{Dq} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	$ACPR_{5M}$ (dBc)
2-carrier W-CDMA	2110 to 2170	720	28	20	19.1	28.5	−34[1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.

1.2 Features and benefits

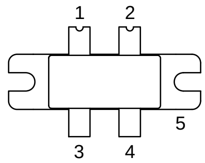
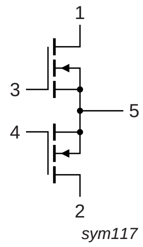
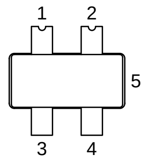
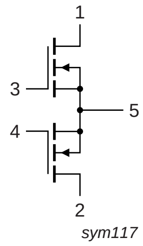
- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (2000 MHz to 2200 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 2000 MHz to 2200 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF7G22L-100P (SOT1121A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLF7G22LS-100P (SOT1121B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF7G22L-100P	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT1121A
BLF7G22LS-100P	-	earless flanged LDMOST ceramic package; 4 leads	SOT1121B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 20 W	0.36	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.6 mA	65	70	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 60 mA	1.5	2	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	12.3	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	200	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 60 mA	-	530	-	mS
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 2100 mA	-	240	-	mΩ

7. Test information

Table 7. Functional test information

Test signal: 2-carrier W-CDMA; PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1, 1-64 PDPCH; f_1 = 2112.5 MHz; f_2 = 2117.5 MHz; f_3 = 2162.5 MHz; f_4 = 2167.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 720 mA; T_{case} = 25 °C; 2 sections combined unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	20	-	W
G_p	power gain	$P_{L(AV)}$ = 20 W	17.8	19.1	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 20 W	-	−16	−9	dB
η_D	drain efficiency	$P_{L(AV)}$ = 20 W	24	28.5	-	%
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)}$ = 20 W	-	−34	−28	dBc

7.1 Ruggedness in class-AB operation

The BLF7G22L-100P and BLF7G22LS-100P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 720 mA; P_L = 100 W (CW); f = 2110 MHz.

7.2 Impedance information

Table 8. Typical push-pull impedance
Measured load pull data. Typical values unless otherwise specified.

f MHz	Z_S Ω	Z_L Ω
2110	1.79 – j4.95	2.27 – j3.64
2140	2.37 – j5.49	2.27 – j3.64
2170	2.54 – j5.86	1.84 – j3.57

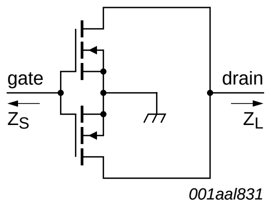
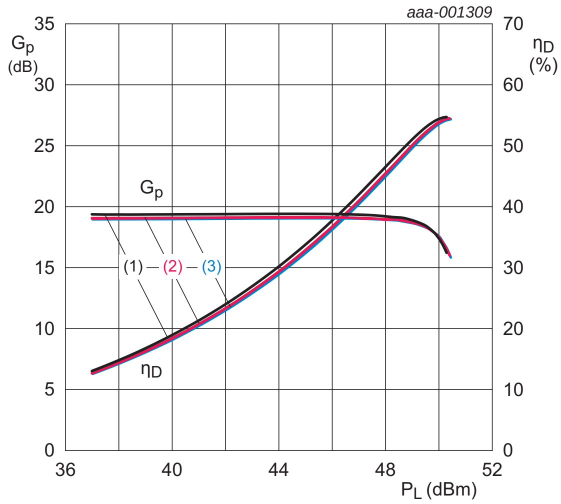


Fig 1. Definition of transistor impedance

7.3 One Tone CW



V_{DS} = 28 V; I_{Dq} = 720 mA.

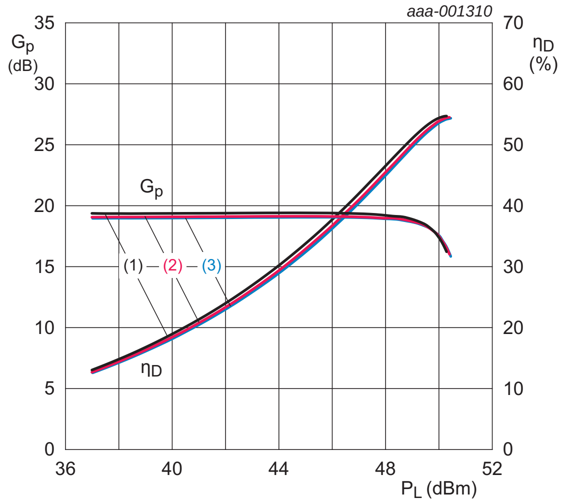
(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 2. Power gain and drain efficiency as function of load power; typical values

7.4 One Tone CW-Pulsed



V_{DS} = 28 V; I_{Dq} = 720 mA.

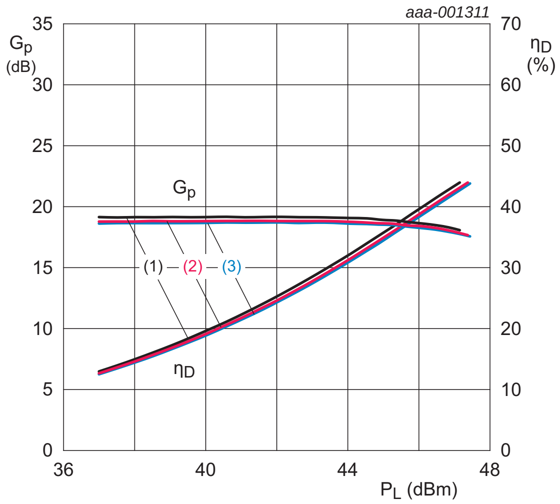
(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 3. Power gain and drain efficiency as a function of load power; typical values

7.5 1-Carrier W-CDMA



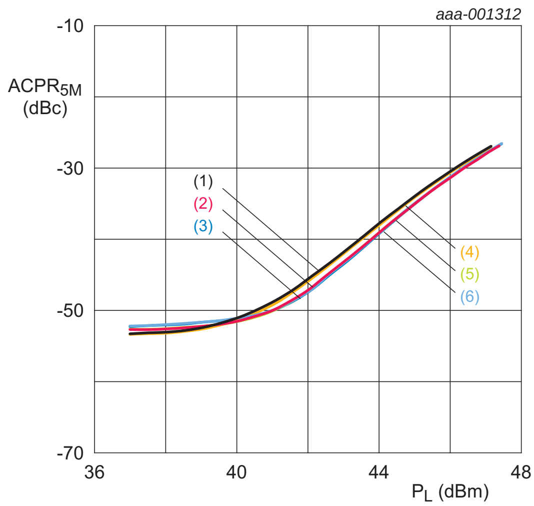
V_{DS} = 28 V; I_{Dq} = 720 mA.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 4. Power gain and drain efficiency as a function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 720 mA.

(1) f = 2110 MHz; f + 5 MHz

(2) f = 2140 MHz; f + 5 MHz

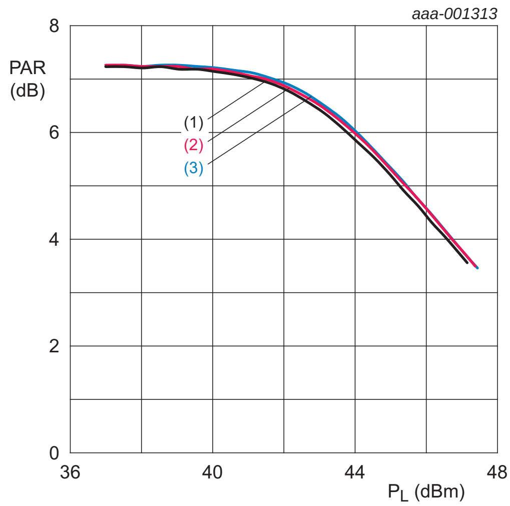
(3) f = 2170 MHz; f + 5 MHz

(4) f = 2110 MHz; f − 5 MHz

(5) f = 2140 MHz; f − 5 MHz

(6) f = 2170 MHz; f − 5 MHz

Fig 5. Adjacent channel power ratio (±5 MHz) as a function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 720 mA.

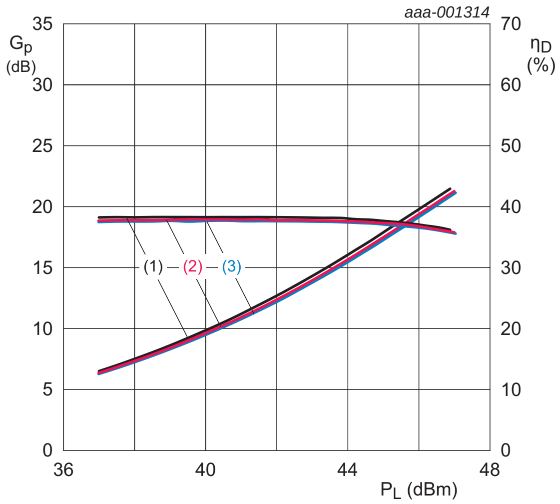
(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 6. Peak-to-average ratio as a function of load power; typical values

7.6 2-Carrier W-CDMA



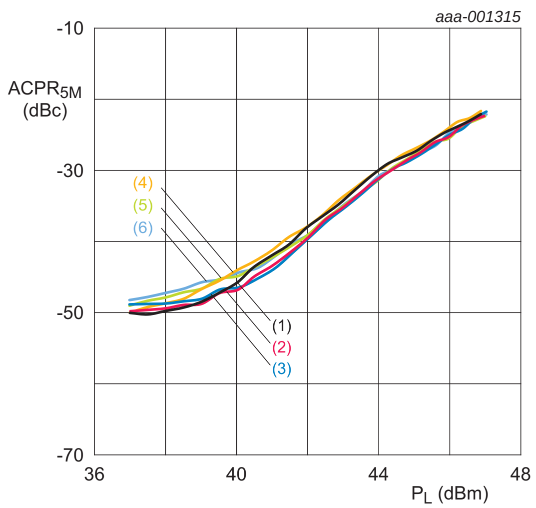
V_{DS} = 28 V; I_{Dq} = 720 mA.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 7. Power gain and drain efficiency as a function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 720 mA.

(1) f = 2110 MHz; f + 5 MHz

(2) f = 2140 MHz; f + 5 MHz

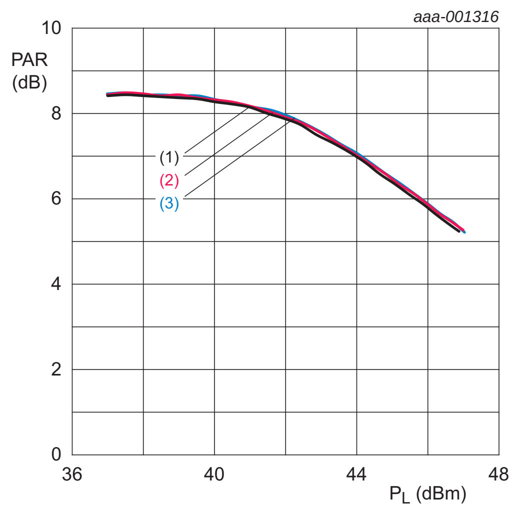
(3) f = 2170 MHz; f + 5 MHz

(4) f = 2110 MHz; f − 5 MHz

(5) f = 2140 MHz; f − 5 MHz

(6) f = 2170 MHz; f − 5 MHz

Fig 8. Adjacent channel power ratio (±5 MHz) as a function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 720 mA.

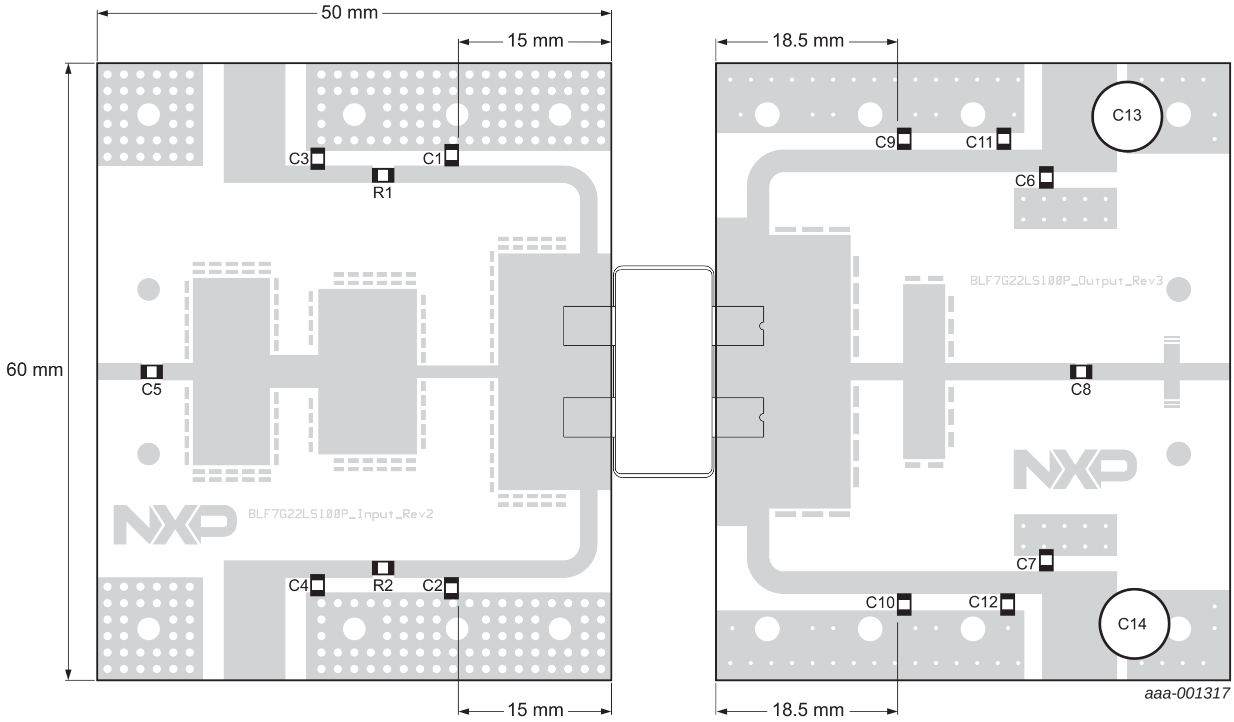
(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 9. Peak-to-average ratio as a function of load power; typical values

7.7 Test circuit



Printed-Circuit Board (PCB): Taconic RF35; ε_r = 3.5; thickness = 0.76 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

Fig 10. Component layout for class-AB production test circuit

Table 9. List of components

For test circuit see Figure 10.

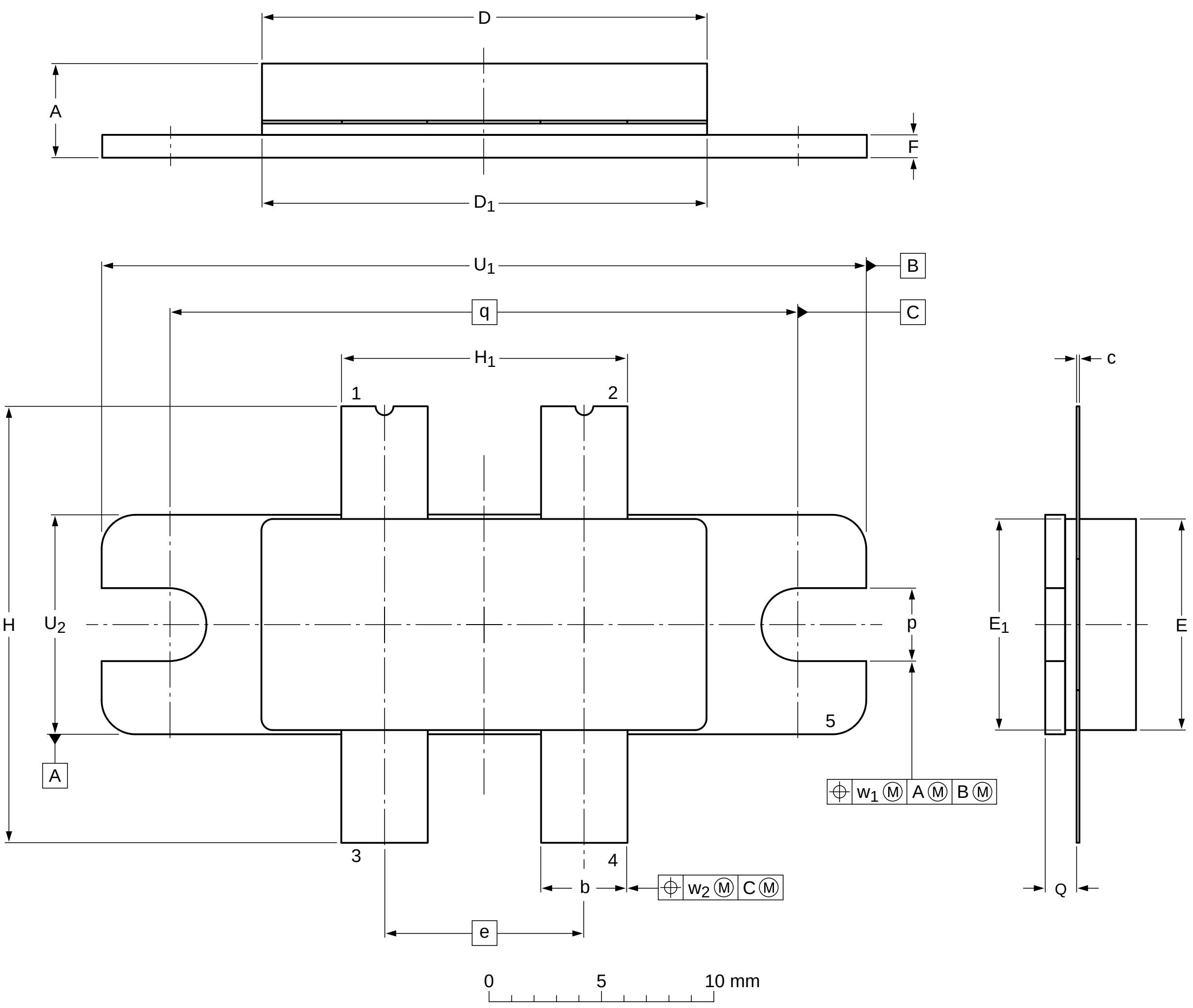
Component	Description	Value		Remarks
C1, C2, C9, C10	multilayer ceramic chip capacitor	8.2 pF	[1]	
C3, C4, C6, C7	multilayer ceramic chip capacitor	1 μF		Murata
C5, C8	multilayer ceramic chip capacitor	33 pF	[2]	
C11, C12	multilayer ceramic chip capacitor	0.1 μF		Murata
C13, C14	electrolytic capacitor	1000 μF; 50 V		
R1, R2	Chip resistor	5.1 Ω		Vishay Dale 0805

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 800B or capacitor of same quality.

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads **SOT1121A**



Dimensions

Unit[1]		A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q[2]	q	U_1	U_2	w_1	w_2
mm	max	4.75	3.94	0.18	20.02	19.96		9.53	9.53	1.14	19.94	12.83	3.38	1.70		34.16	9.91		
	nom						8.89								27.94			0.25	0.51
	min	3.45	3.68	0.10	19.61	19.66		9.27	9.27	0.89	18.92	12.57	3.12	1.45		33.91	9.65		
inches	max	0.187	0.155	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.505	0.133	0.067		1.345	0.39		
	nom						0.35								1.1			0.01	0.02
	min	0.136	0.145	0.004	0.772	0.774		0.365	0.365	0.035	0.745	0.495	0.123	0.057		1.335	0.38		

Note

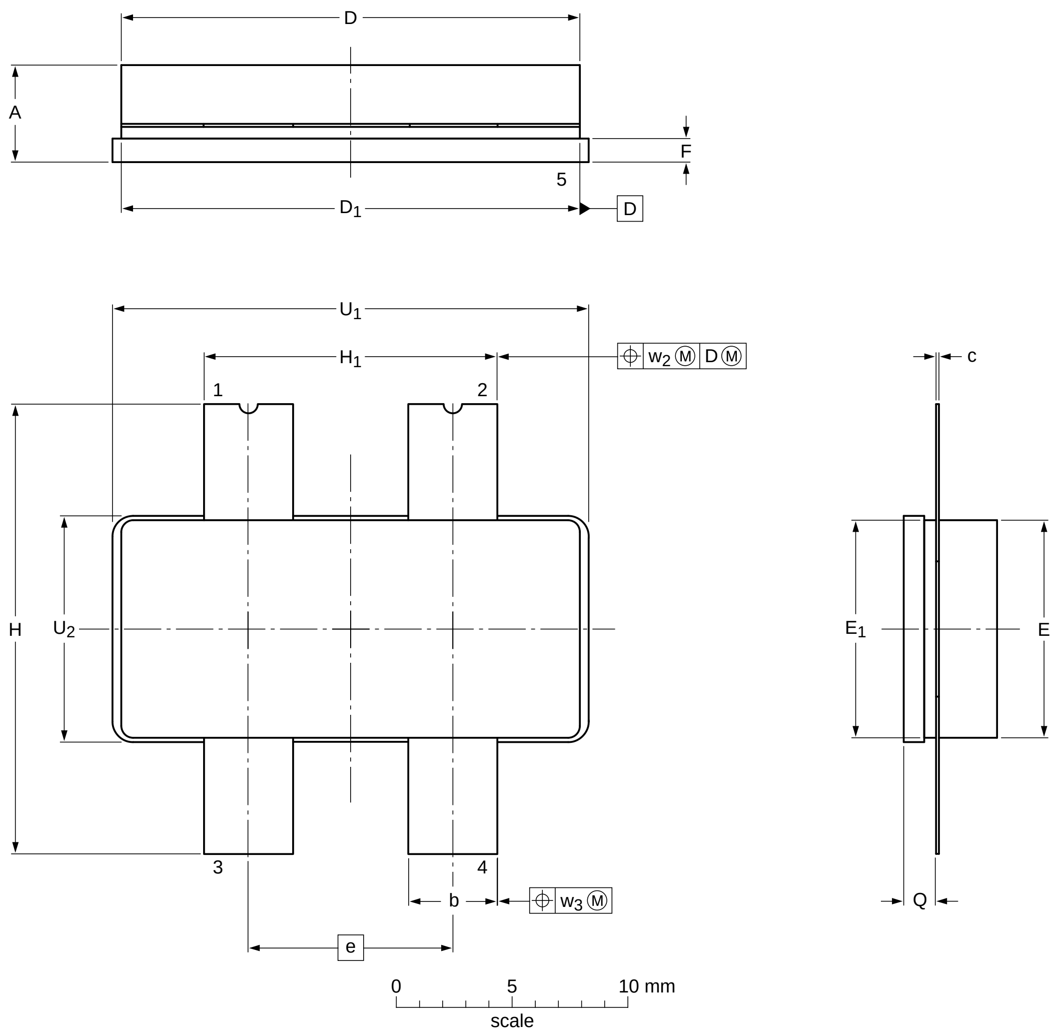
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1121A						~~09-10-12~~ 10-02-02

Fig 11. Package outline SOT1121A

Earless flanged LDMOST ceramic package; 4 leads **SOT1121B**



Dimensions

Unit(1)		A	b	c	D	D1	e	E	E1	F	H	H1	Q	U1	U2	w2	w3
mm	max	4.75	3.94	0.18	20.02	19.96		9.53	9.53	1.14	19.94	12.83	1.70	20.70	9.91		
	nom						8.89									0.51	0.25
	min	3.45	3.68	0.08	19.61	19.66		9.27	9.27	0.89	18.92	12.57	1.45	20.45	9.65		
inches	max	0.187	0.155	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.505	0.067	0.815	0.39		
	nom						0.35									0.02	0.01
	min	0.136	0.145	0.003	0.772	0.774		0.365	0.365	0.035	0.745	0.495	0.057	0.805	0.38		

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1121B						~~09-10-12~~ 09-12-14

Fig 12. Package outline SOT1121B

9. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical Channel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
PDPCH	Transmission Power of Dedicated Physical Channel
RF	Radio Frequency
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

10. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF7G22L-100P_BLF7G22LS-100P v.3	20120102	Product data sheet	-	BLF7G22L-100P_BLF7G22LS-100P v.2
Modifications:	• The status of this document has been changed to Product data sheet. • Figure 1 on page 4: figure has been changed.			
BLF7G22L-100P_BLF7G22LS-100P v.2	20111110	Preliminary data sheet	-	BLF7G22L-100P_BLF7G22LS-100P v.1
BLF7G22L-100P_BLF7G22LS-100P v.1	20110519	Objective data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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13. Contents

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