Doc No. TT4-EA-12408

Revision. 2

MOS FET

Unit: mm

0.13

MTM78E2B0LBF

Panasonic

MTM78E2B0LBF

Gate Resistor installed Dual N-Channel MOS Type

For lithium-ion secondary battery protection circuit

Features

- Low drain-source On-state Resistance RDS(on) typ. = 21.5 m Ω (VGS =4.0 V)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)
- Marking Symbol: 5A

■ Packaging

Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

1. Source 1 5. Drain
2. Gate 1 6. Drain
3. Source 2 7. Drain
4. Gate 2 8. Drain

Panasonic WSMini8-F1-B

JEITA SC-113E

2.0

8 17 16

Code

		-	_	~-	~ ~
Absolute	Maximum	Ratings	la=	25	°C

Parameter		Symbol	Rating	Unit	
	Drain-source Voltage	VDS	20	V	
	Gate-source Voltage	VGS	±12	V	
FET2	Drain current	ID	4.0	Α	
	Peak drain current *1	IDp	40	Α	
Overall	Total power dissipation	PD1 ⁻²	700	mW	
	Total power dissipation	PD2 ⁻³	150		
	Channel temperature	Tch	150	°C	
	Operating ambient temperature	Topr	-40 to +85	°C	
	Storage temperature	Tstg	-55 to +150	°C	

Note)

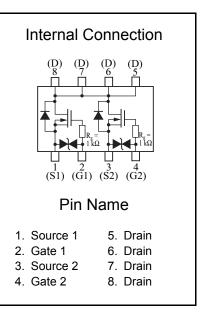
- *1 t = 10 µs, Duty Cycle < 1 %
 - Ceramic substrate (70 \times 70 \times t 1.0 mm)
- *2 Dual operating

Established: 2010-03-03

: 2013-10-15

Revised

*3 Stand-alone (without the substrate)



Doc No. TT4-EA-12408 Revision. 2

Panasonic

MOS FET MTM78E2B0LBF

■ Electrical Characteristics Ta = 25°C ± 3°C

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source surrender voltage	VDSS	ID = 1.0 mA, VGS = 0	20			V
Drain-source cutoff current	IDSS	VDS = 20 V, VGS = 0			1.0	μΑ
Gate-source cutoff current	IGSS	VGS = ±12 V, VDS = 0			±10	μΑ
Gate threshold voltage	Vth	ID = 1.0 mA, VDS = 10 V	0.40	0.85	1.30	V
	RDS(ON)1	ID = 2.0 A, VGS = 4.0 V		21.5	25.0	mΩ
Drain-source ON resistance	RDS(ON)2	ID = 1.5 A, VGS = 3.0 V		26.0	30.0	mΩ
	RDS(ON)3	ID = 1.0 A, VGS = 2.5 V		30.0	36.0	mΩ
Forward transfer admittance	Yfs	ID = 1.0 A, VDS = 10 V	1.0			S
Short-circuit input capacitance (Common source)	Ciss			1100		pF
Short-circuit output capacitance (Common source)	Coss	VDS = 10 V, VGS = 0, f = 1 MHz		75		pF
Reverse transfer capacitance (Common source)	Crss			70		рF
Turn-on delay time *1, *2	td(on)			0.2		μs
Rise time *1, *2	tr	VDD = 10 V, VGS = 4 V,		0.5		μs
Turn-off delay time *1, *2	td(off)	ID = 1.0 A, RL = 10 Ω		2.0		μs
Fall time *1, *2	tf			1.5		μs

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

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Established: 2010-03-03 : 2013-10-15 Revised

^{2. *1} t = 10 μ s, Duty Cycle < 1 %

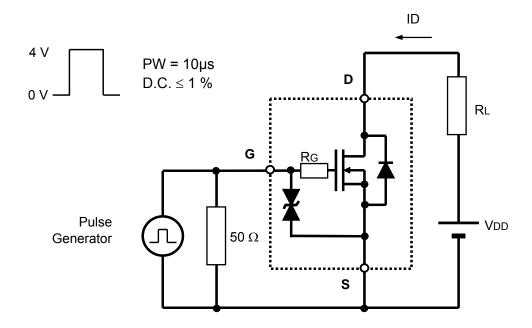
^{*2} Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time

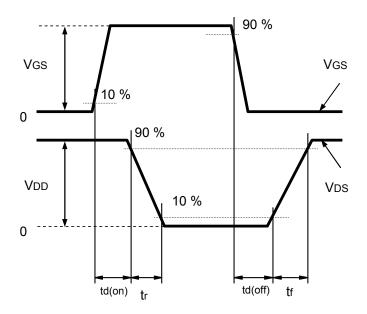
MOS FET

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*2 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time



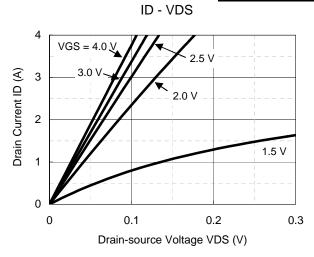


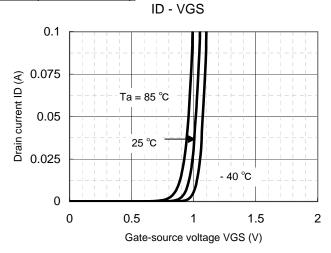
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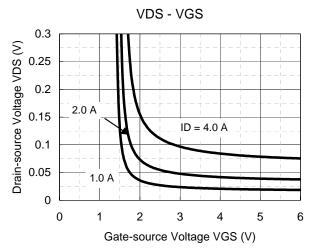
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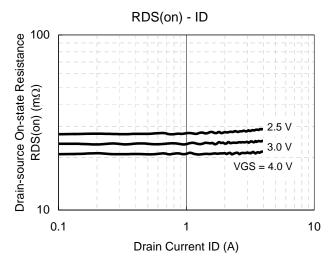
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Technical Data (reference)

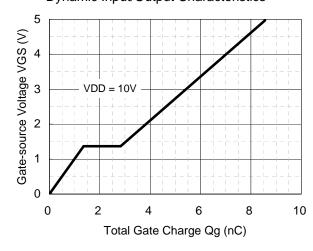








Dynamic Input/Output Characteristics



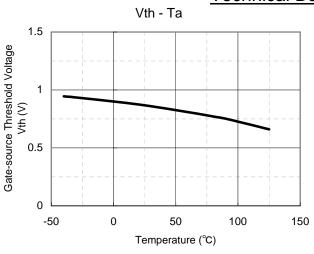
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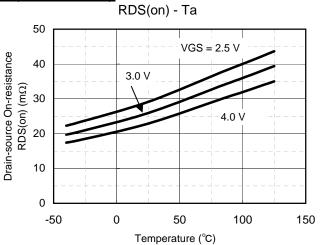
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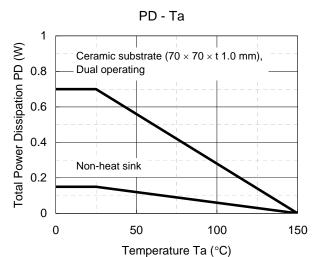
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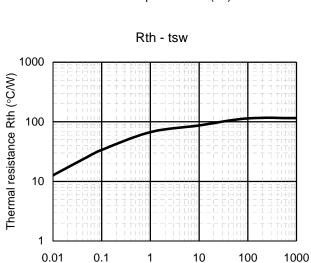
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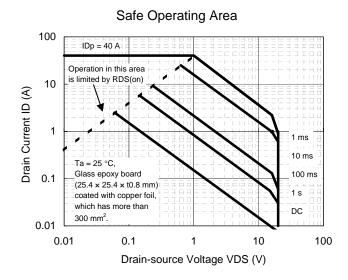








Pulse Width tsw (s)



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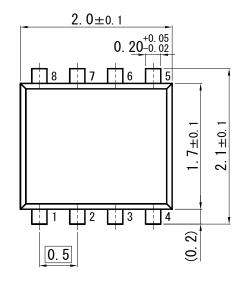
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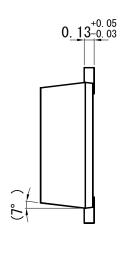
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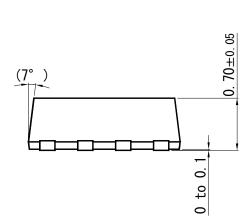
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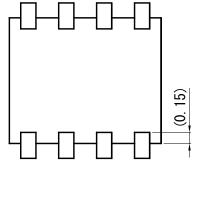
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Unit: mm

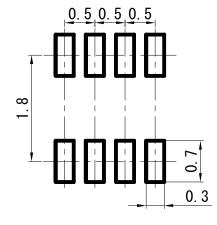








■ Land Pattern (Reference) (Unit : mm)



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