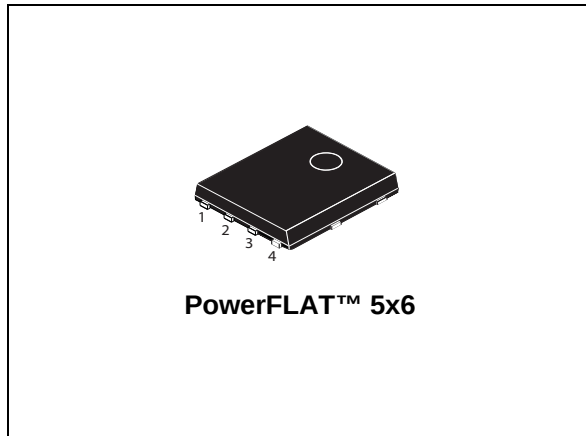


Automotive-grade N-channel 40 V, 6.1 mΩ typ., 18 A STripFET™ F5 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL70N4LLF5	40 V	6.7 mΩ	70 A

- Designed for automotive applications and AEC-Q101 qualified
- Low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™ F5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Figure 1. Internal schematic diagram

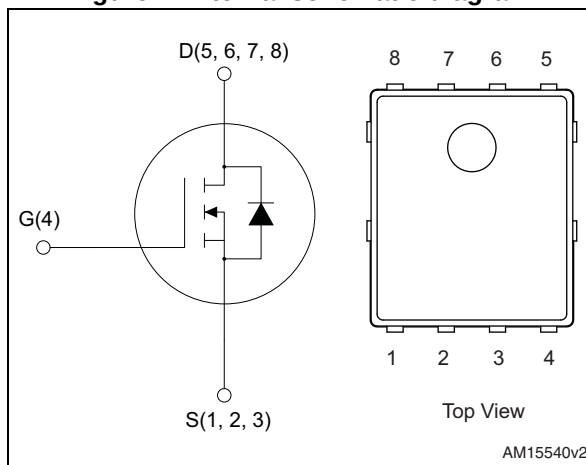


Table 1. Device summary

Order code	Marking	Package	Packaging
STL70N4LLF5	70N4LLF5	PowerFLAT™ 5x6	Tape and reel

Contents

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 2.1 **Electrical characteristics (curves)** 6

3 **Test circuits** 8

4 **Package mechanical data** 9

5 **Packaging mechanical data** 13

6 **Revision history** 15



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 22	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	70	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	44	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	18	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb}=100\text{ }^\circ\text{C}$	11.5	A
$I_{DM}^{(2),(3)}$	Drain current (pulsed)	72	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	72	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
	Derating factor ⁽²⁾	0.03	W/°C
T_J	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		

1. The value is rated according to R_{thj-c} .
2. The value is rated according to $R_{thj-pcb}$.
3. Pulse width limited by safe operating area.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.08	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10$ sec.

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current, (pulse width limited by $T_{j\max}$)	9	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 24\text{ V}$)	470	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 250\text{ }\mu\text{A}$	40			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 40\text{ V}$			1	μA
		$V_{DS} = 40\text{ V}, T_C = 125\text{ }^{\circ}\text{C}$			10	μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 22\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 9\text{ A}$		6.1	6.7	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 9\text{ A}$		7.6	9	m Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	1570	-	pF
C_{oss}	Output capacitance		-	257	-	pF
C_{rss}	Reverse transfer capacitance		-	32	-	pF
Q_g	Total gate charge	$V_{DD} = 15\text{ V}, I_D = 18\text{ A}$ $V_{GS} = 4.5\text{ V}$ (Figure 14)	-	12.9	-	nC
Q_{gs}	Gate-source charge		-	3.9	-	nC
Q_{gd}	Gate-drain charge		-	5.3	-	nC
R_G	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV $I_D = 0$	-	1.5	-	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}, I_D = 9\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (Figure 13)	-	14	-	ns
t_r	Rise time		-	42	-	ns
$t_{d(off)}$	Turn-off delay time		-	37	-	ns
t_f	Fall time		-	5.2	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		18	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		72	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 18\text{ A}$, $V_{GS}=0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 18\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 25\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	27.2		ns
Q_{rr}	Reverse recovery charge		-	24.5		nC
I_{RRM}	Reverse recovery current		-	1.8		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

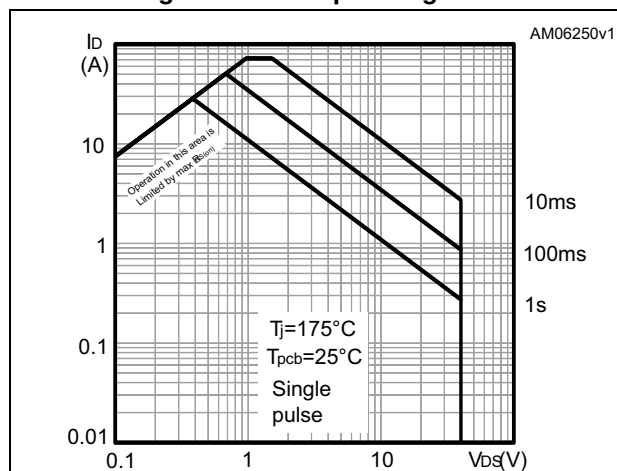


Figure 3. Thermal impedance

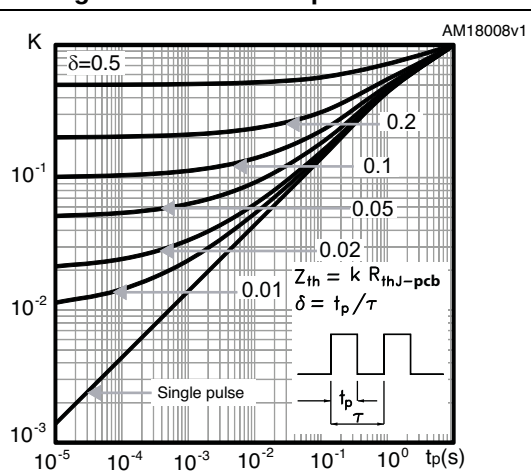


Figure 4. Output characteristics

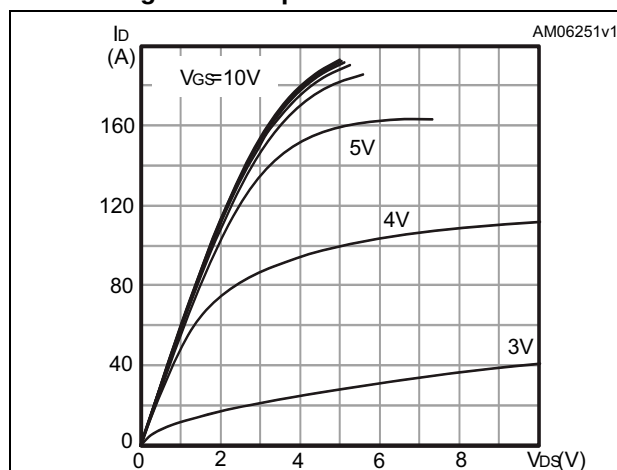


Figure 5. Transfer characteristics

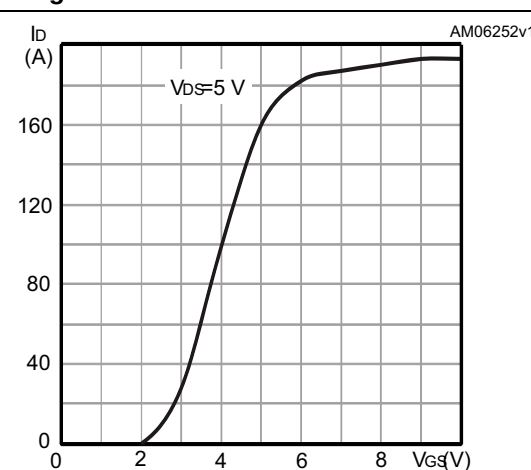
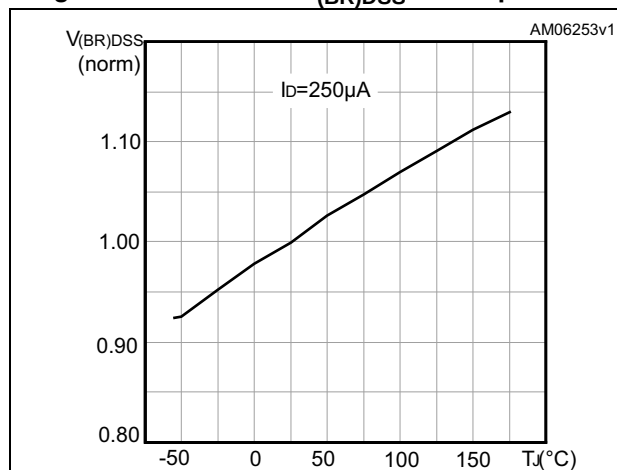
Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

Figure 7. Static drain-source on-resistance

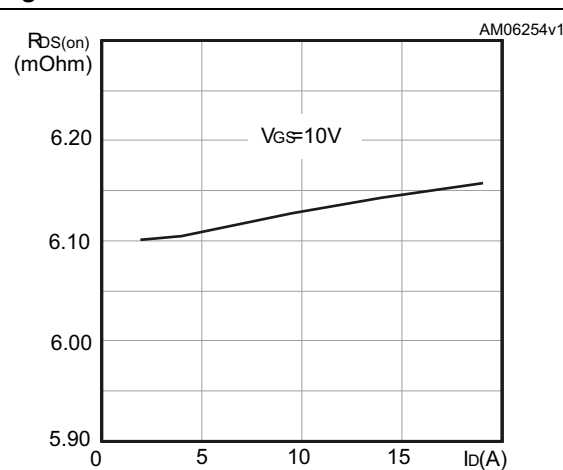


Figure 8. Gate charge vs gate-source voltage

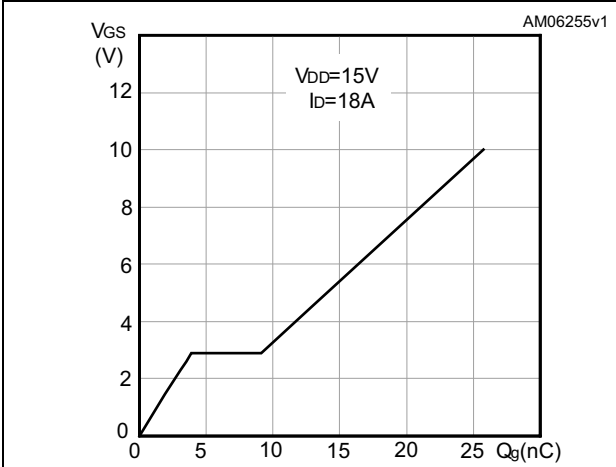


Figure 9. Capacitance variations

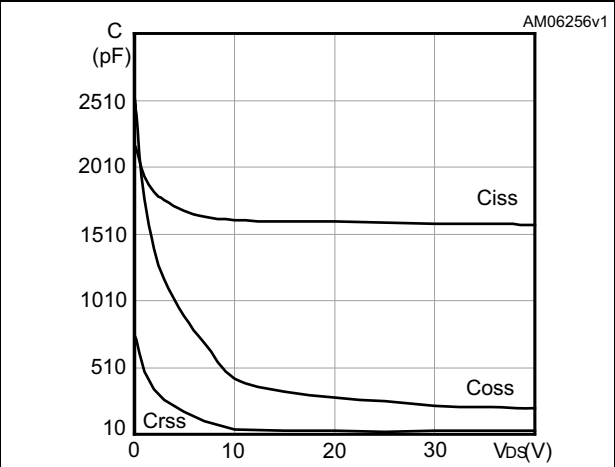


Figure 10. Normalized gate threshold voltage vs temperature

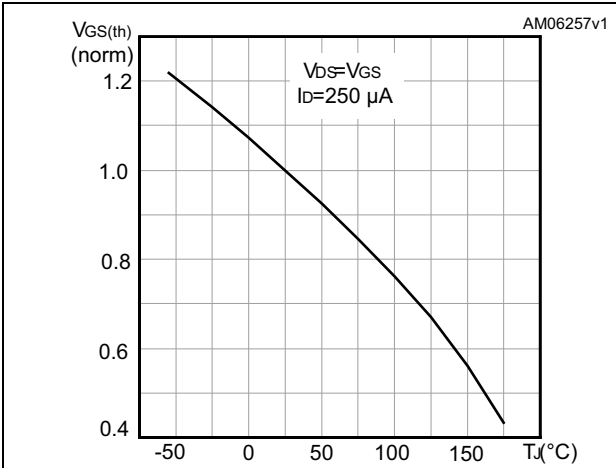


Figure 11. Normalized on-resistance vs temperature

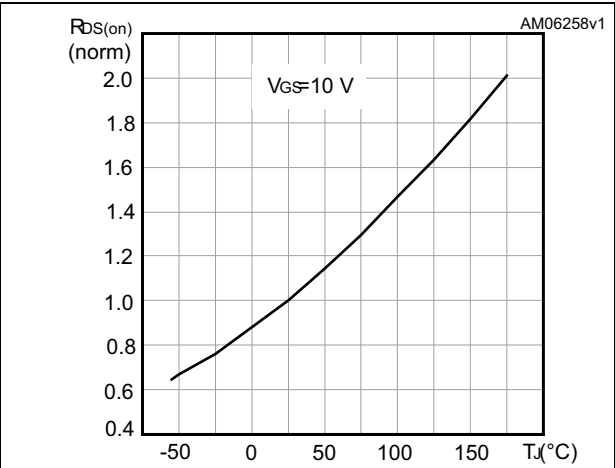
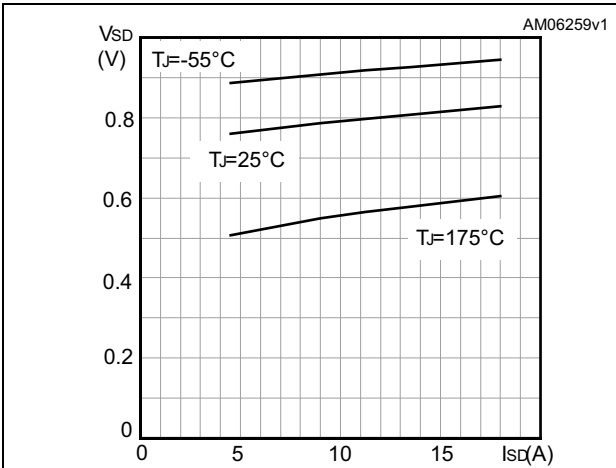


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

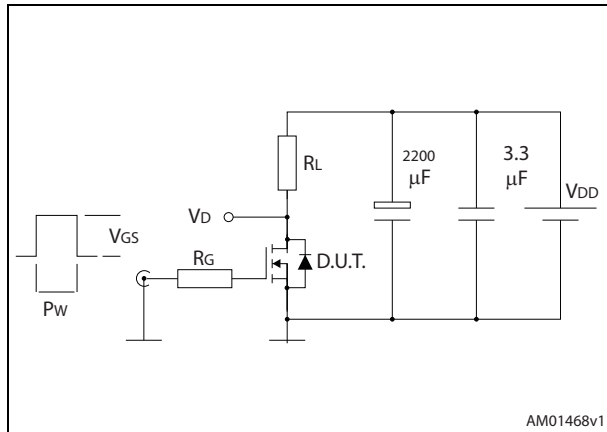


Figure 14. Gate charge test circuit

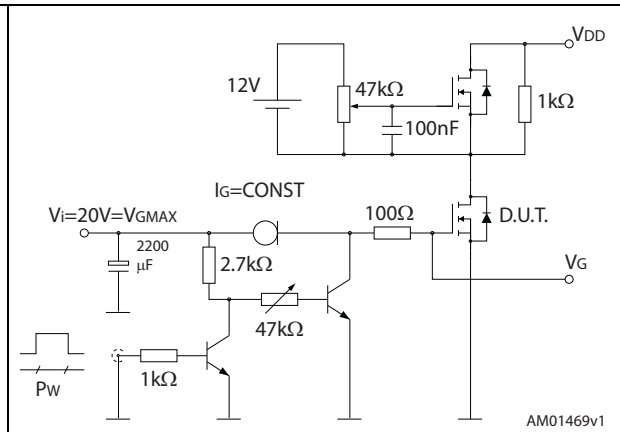


Figure 15. Test circuit for inductive load switching and diode recovery times

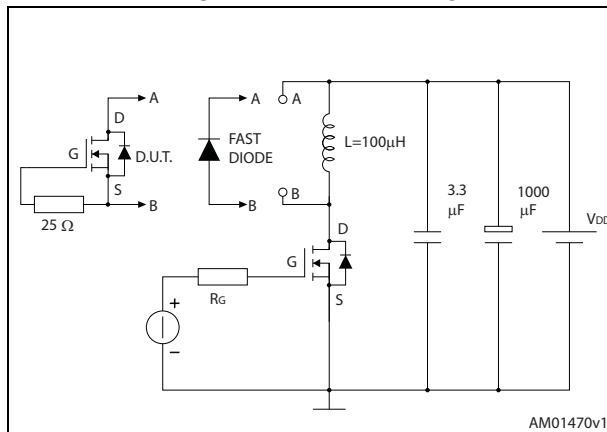


Figure 16. Unclamped inductive load test circuit

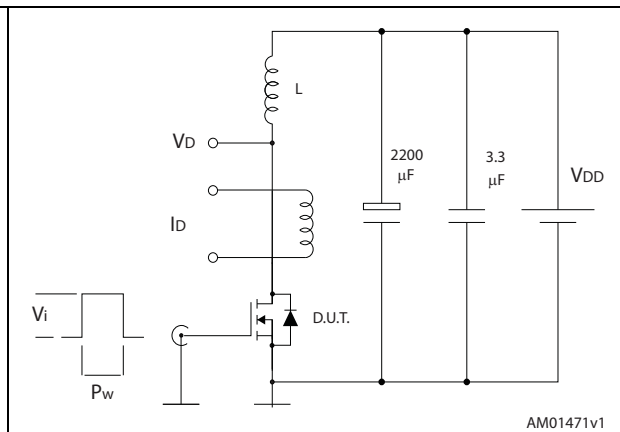


Figure 17. Unclamped inductive waveform

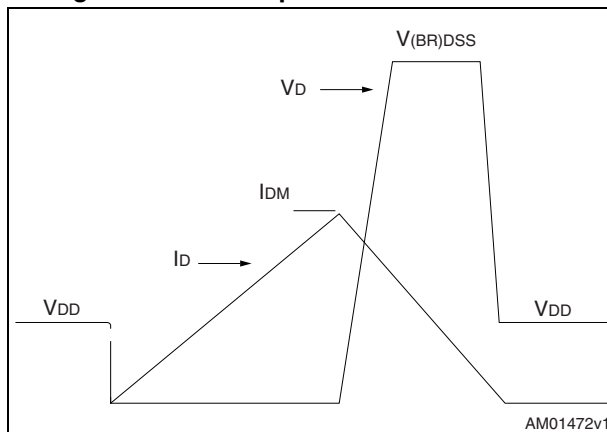
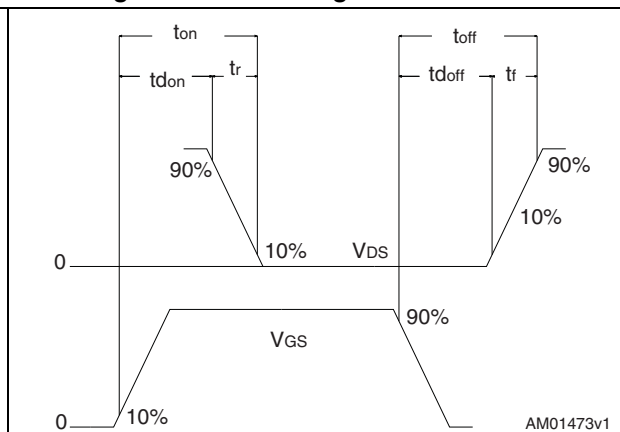


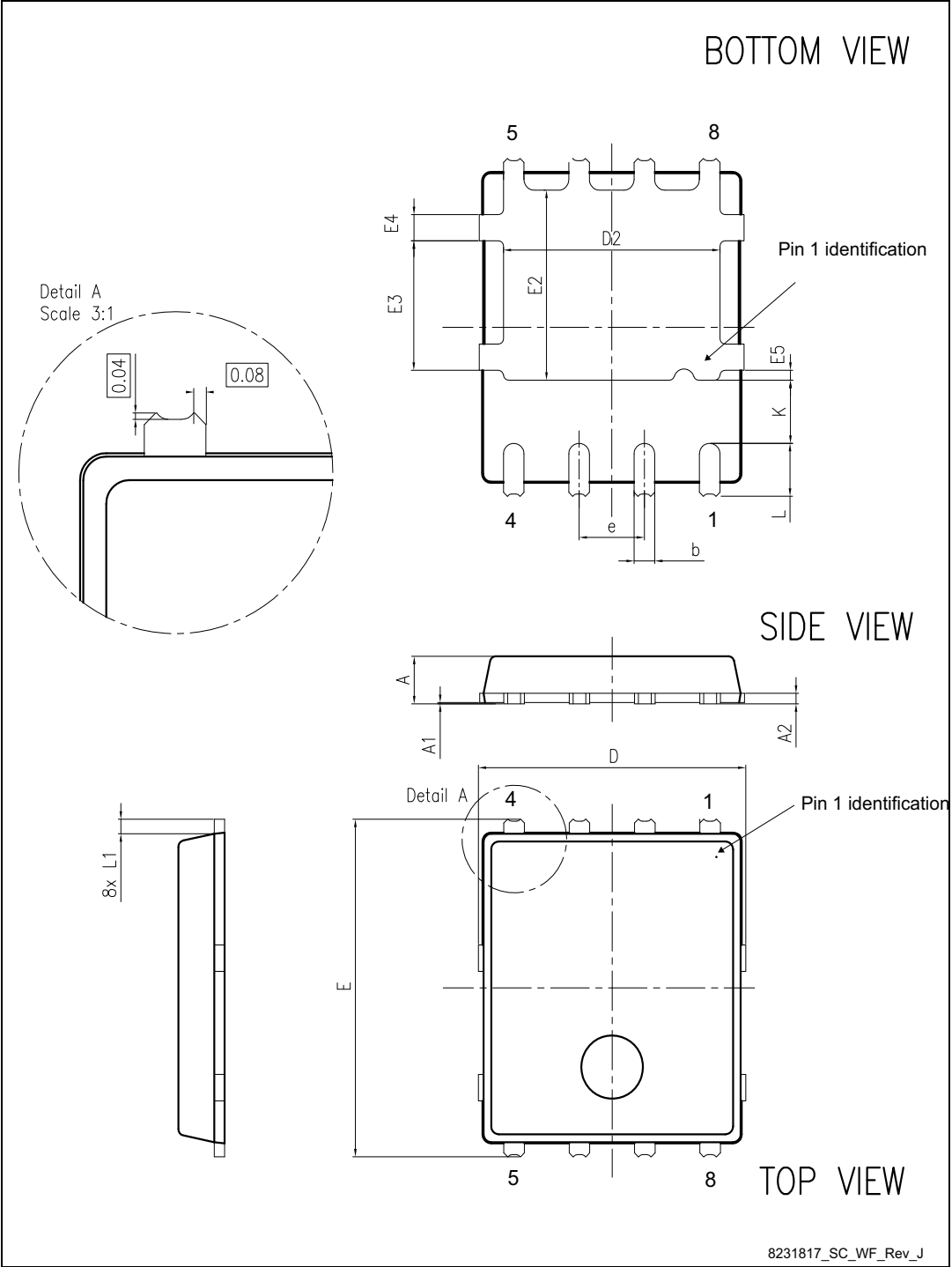
Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 19. PowerFLAT™ 5x6 WF type S-C drawing

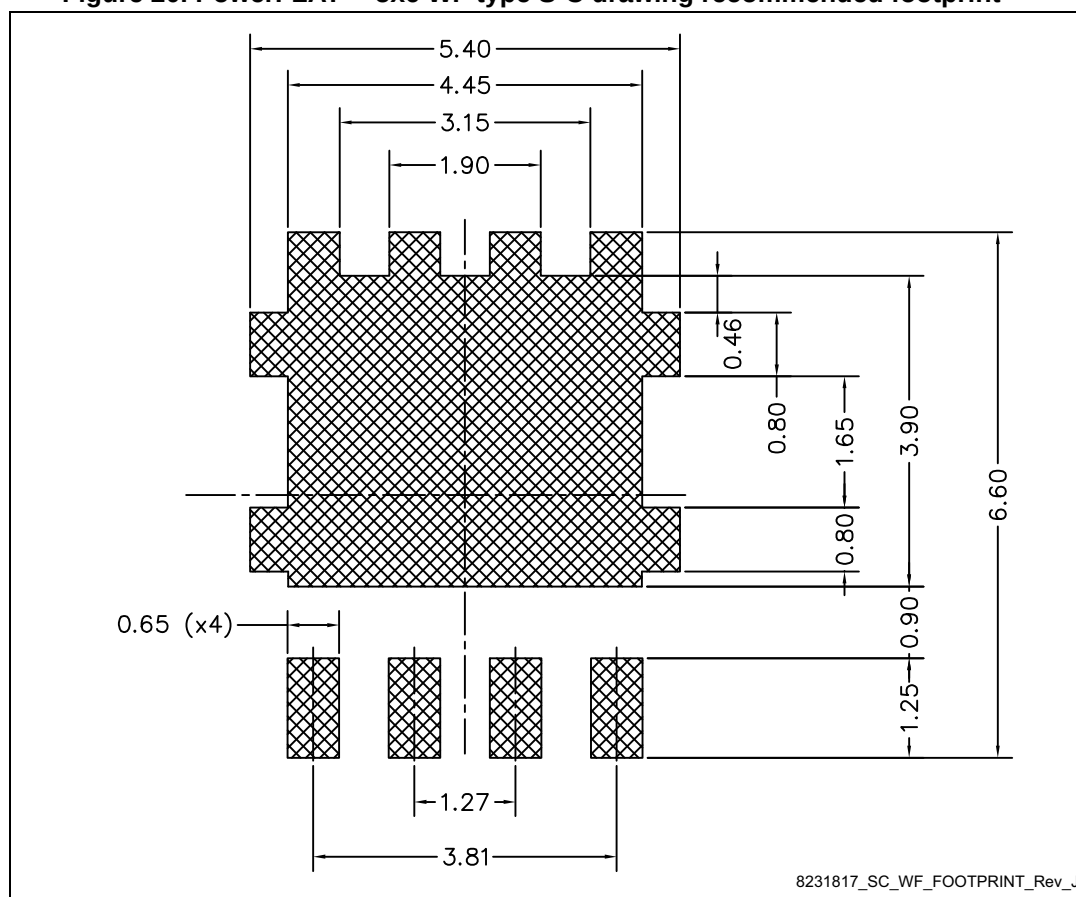


8231817_SC_WF_Rev_J

Table 9. PowerFLAT™ 5x6 WF type S-C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	6.20	6.40	6.60
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
e1		0.65	
L	0.90		1.10
L1		0.275	
K	1.05		1.35
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28

Figure 20. PowerFLAT™ 5x6 WF type S-C drawing recommended footprint (a)



a. All dimensions are in mm.

5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 tape^(b)

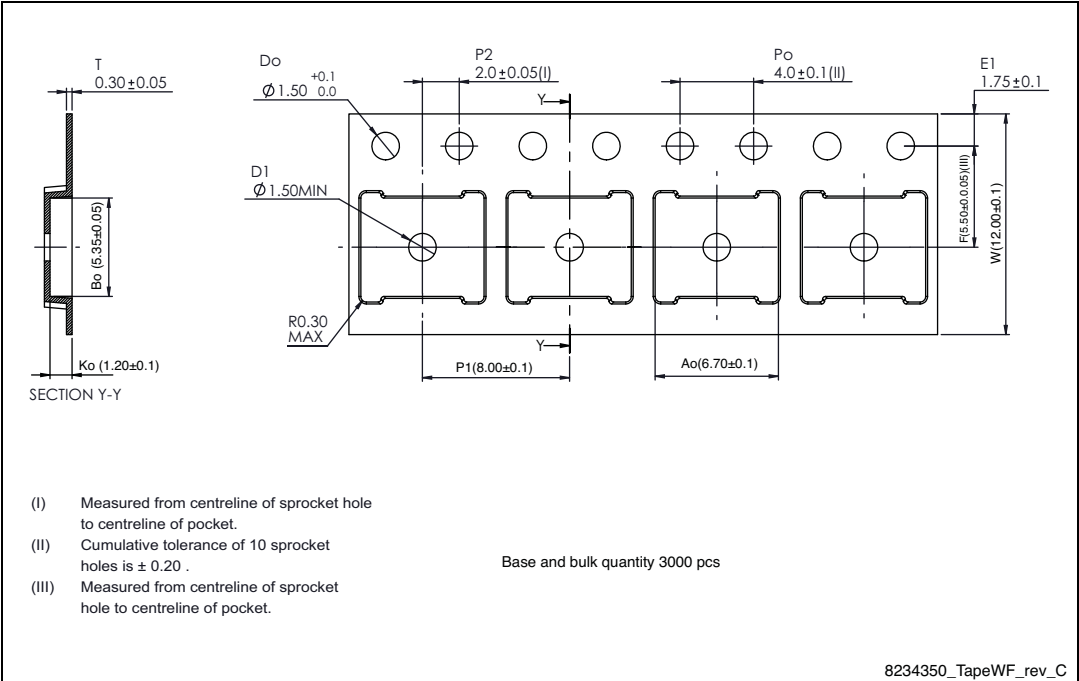
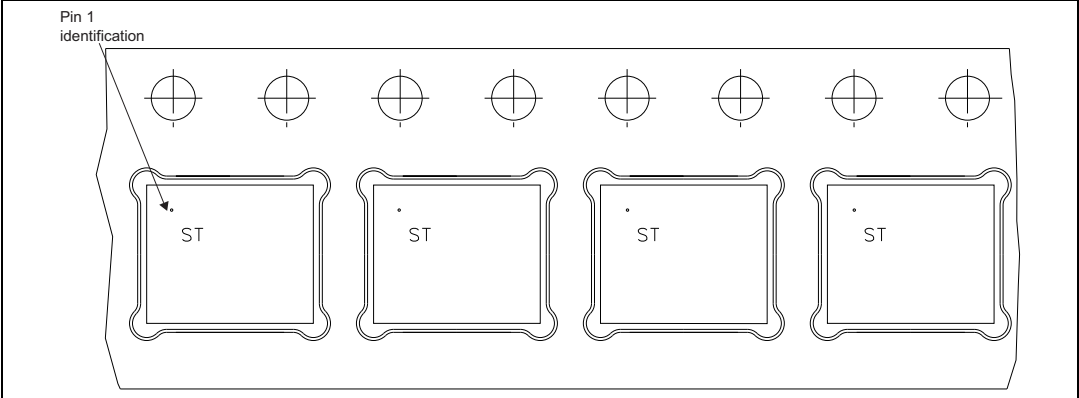
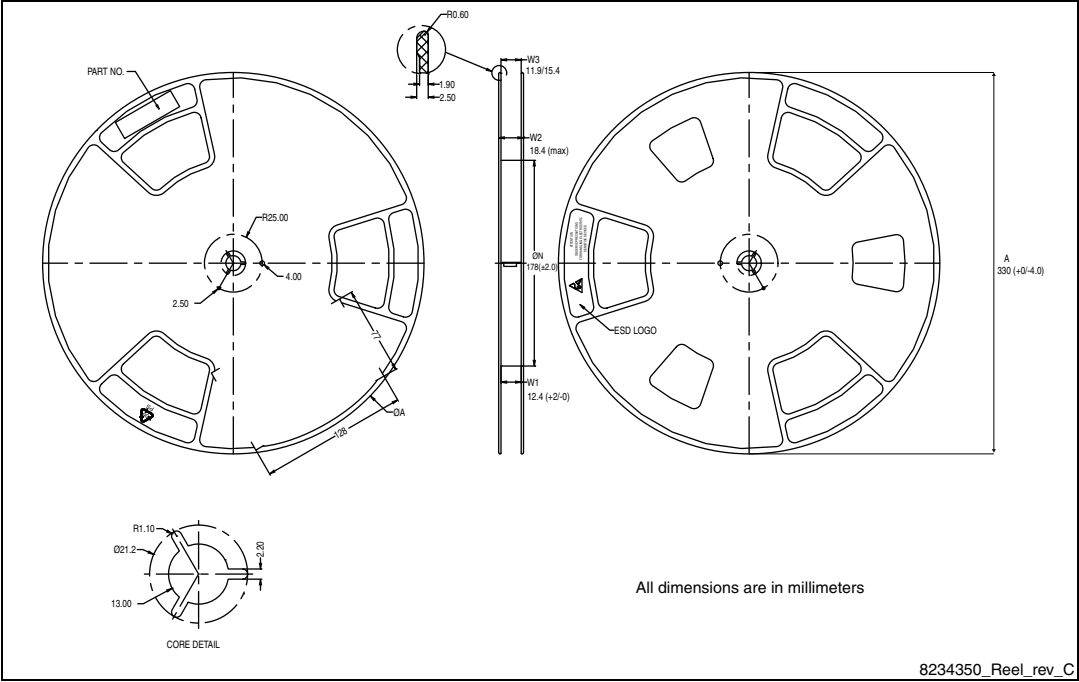


Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape



b. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 reel



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
01-Dec-2008	1	First release
18-Jul-2011	2	Section 4: Package mechanical data has been modified: – Added Table 9: PowerFLAT™ 5x6 type S-C mechanical data – Added Figure 19: PowerFLAT™ 5x6 type S-C mechanical data – Added PowerFLAT™ 5x6 type C-B mechanical data – Added PowerFLAT™ 5x6 type C-B drawing – Minor text changes.
21-Dec-2011	3	Section 4: Package mechanical data has been modified.
25-Jan-2013	4	– Table 1: Device summary has been updated. – Minor text changes. – Changed: Figure 1 – Added: Section 5: Packaging mechanical data
12-Feb-2013	5	– Updated T_J and T_{stg} in Table 2: Absolute maximum ratings. – Updated Section 4: Package mechanical data and Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape.
24-May-2013	6	– Modified: title and Section 4: Package mechanical data – Minor text changes
17-Dec-2014	7	– Modified: Figure 2 and 3 – Updated: Figure 13, 14, 15 and 16 – Updated: Section 4: Package mechanical data and Section 5: Packaging mechanical data – Minor text changes

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