

1024KX 16 BITLOW POWER CMOS SRAM

#### **FEATURES**

- Fast access time : 55/70ns
- Low power consumption: Operating current : 45/30mA (TYP.) Standby current : 4µA (TYP.) SL-version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7) UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.2V (MIN.)
- Lead free and green package available
- Package : 48-ball 6mm x 8mm TFBGA

#### PRODUCT FAMILY

## **GENERAL DESCRIPTION**

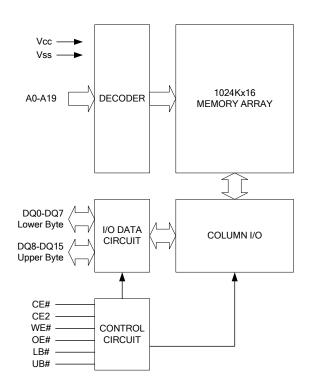
The AS6C1616 is a 16,777,216-bit low power CMOS static random access memory organized as 1,048,576 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C1616 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C1616 operates from a single power supply of 2.7V  $\sim$  3.6V and all inputs and outputs are fully TTL compatible

Product	Operating	Vcc Range	Speed	Power Dissipation				
Family	Temperature	vec ixange	Speed	Standby(IsB1,TYP.)	Operating	(Icc,TYP.)		
AS6C1616(I)	-40 ~ 85℃	2.7 ~ 3.6V	55/70ns	4µA	45/30mA			

#### **FUNCTIONAL BLOCK DIAGRAM**

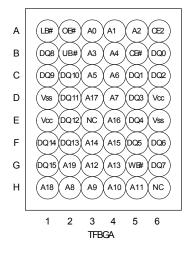


## **PIN DESCRIPTION**

SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vœ	Power Supply
Vss	Ground



## **PIN CONFIGURATION**



### **ABSOLUTE MAXIMUN RATINGS\***

PARAMETER SYMBOL		RATING	UNIT
Voltage on Vcc relative to Vss	Vt1	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	Vt2	-0.5 to V $\infty$ +0.5 V	
Operating Temperature	Та	-40 to 85(I grade)	°C
Storage Temperature	Tsīg	-65 to 150	°C
Power Dissipation	Pd 1		W
DC Output Current	Іолт <b>50</b>		mA
Soldering Temperature (under 10 sec)	Tsolder 260		°C

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.



## **TRUTH TABLE**

MODE	CE#	CE2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
MODE					<b>U</b> LI	DQ0-DQ7 DQ8-DQ15			
	Н	Х	Х	Х	Х	Х	High – Z	High – Z	
Standby	Х	L	Х	Х	Х	Х	High – Z	High – Z	ISB,ISB1
	Х	Х	Х	Х	Н	Н	High – Z	High – Z	
Output Disable	L	Н	Н	Н	L	Х	High – Z	High – Z	lœ,lca
	L	Н	Н	Н	Х	L	High – Z	High – Z	100,100
	L	Н	L	Н	L	Н	D <sub>OUT</sub>	High – Z	
Read	L	Н	L	Н	Н	L	High – Z	D <sub>OUT</sub>	lœ,lca
	L	Н	L	Н	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	
	L	Н	Х	L	L	Н	D <sub>IN</sub>	High – Z	
Write	L	Н	Х	L	Н	L	High – Z	D <sub>IN</sub>	lœ,lca
	L	Н	Х	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	

Note:  $H = V \parallel H, L = V \parallel L, X = Don'tcare.$ 

## **DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION		MIN.	<b>TYP.</b> <sup>•4</sup>	MAX.	UNIT
Supply Voltage	Vcc			2.7	3.0	3.6	V
Input High Voltage	Vih *1			2.2	- '	Vcc +0.3	V
Input Low Voltage	VIL *2			- 0.2	-	0.6	V
Input Leakage Current	LI	$V_{CC} \ge V_{IN} \ge V_{SS}$		- 1	-	1	μA
Output Leakage Current	Ilo	Vcc ≧ Vour ≧ Vss Output Disabled		- 1	-	1	μA
Output High Voltage	Vон	Іон <b>=</b> -1 <b>m</b> A		2.2	2.7	-	V
Output Low Voltage	Vol	Io∟ <b>= 2mA</b>		-	-	0.4	V
	lœ	Cycle time =Min. CE# =V ⊫ and CE2 = V⊮	-55		45	60	mA
AverageOperating		I⊮o = 0mA Other pins at V⊫ or Vн	-70	-	30	45	mA
Power supply Current	lca	Cyde time = $1\mu s$ CE# $\leq 0.2V$ and CE $2 \geq V\infty$ -0.2V $I_{1/0} = 0mA$ Other pins at 0.2V or V $\infty$ -0.2V	,	-	8	16	mA
Standby Power Supply Curent	Isb	CE# =V⊪ or CE2 =V⊩ Other pins at V⊩ or Vн		-	0.3	2	mA
	ISB1	CE# $\forall c \ge -02V$ or CE2 $\le 0.2V$ Other pins at 0.2V or $\forall c$ -0.2V	-SLI	-	6	40	μA

Notes:

1.  $V_{H}(max) = V_{CC} + 3.0V$  for pulse width less than 10ns. 2.  $V_{IL}(min) = V_{SS} - 3.0V$  for pulse width less than 10ns. 3. Over/Undershoot specifications are characterized, not 100% tested.

4. Typical values are included for reference only and are not guaranteed or tested.

Typical values are measured at Vcc = Vcc(TYP.) and TA =  $25^{\circ}$ C



# CAPACITANCE (TA = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	Cin	i <del>n</del>	6	pF
Input/Output Capacitance	Ci/o	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

#### **AC TEST CONDITIONS**

Input Pulse Levels	0.2V to Vcc - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	Сь = 30pF + 1TTL, Iон/Iоь = -1mA/2mA

# AC ELECTRICAL CHARACTERISTICS

#### (1) READ CYCLE

PARAMETER	SYM.	AS6C1	<b>616</b> -55	AS6C1	616-70	UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	trc	55	8	70		ns
Address Access Time	taa		55		70	ns
Chip Enable Access Time	TACE		55	1. <b></b> .	70	ns
Output Enable Access Time	toe		30	3 <b></b>	35	ns
Chip Enable to Output in Low-Z	tcLz*	10		10		ns
Output Enable to Output in Low-Z	toLz*	5	( <b>#</b> )	5	i.	ns
Chip Disable to Output in High-Z	tcHz*		20	5 <b>.</b>	25	ns
Output Disable to Output in High-Z	tonz*		20	3 <b>11</b>	25	ns
Output Hold from Address Change	toн	10		10		ns
LB#, UB# Access Time	tba		55		70	ns
LB#, UB# to High-Z Output	tвнz*	-	25	5 <b>.</b>	30	ns
LB#, UB# to Low-Z Output	telz*	10	-	10	. <b></b>	ns

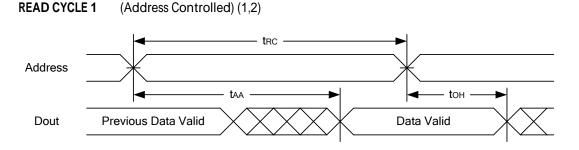
#### (2) WRITE CYCLE

PARAMETER	SYM.	AS6C1	616-55	AS6C1	UNIT	
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	twc	55		70	<b>.</b>	ns
Address Valid to End of Write	taw	50	-	60	-	ns
Chip Enable to End of Write	tcw	50	-	60	-	ns
Address Set-up Time	tas	0	1007	0	1007 3008	ns
Write Pulse Width	twp	45	1000	55	1000	ns
Write Recovery Time	twr	0	-	0	-	ns
Data to Write Time Overlap	tow	25	-	30	-	ns
Data Hold from End of Write Time	toн	0	1007 3009	0	1007 3009	ns
Output Active from End of Write	tow*	5		5	-	ns
Write to Output in High-Z	twnz*	-	20	-	25	ns
LB#, UB# Valid to End of Write	tвw	45	-	60	-	ns

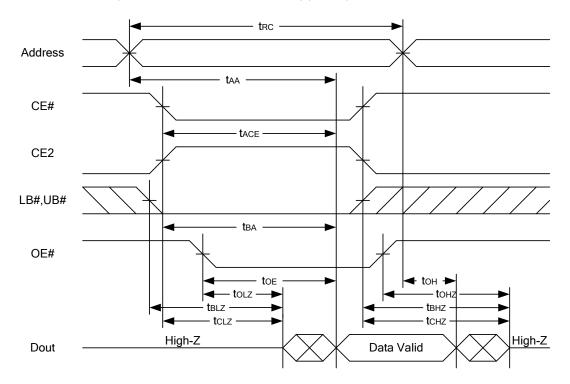
\*These parameters are guaranteed by device characterization, but not production tested.



### **TIMING WAVEFORMS**



**READ CYCLE 2** (CE# and CE2 and OE# Controlled) (1,3,4,5)



Notes :

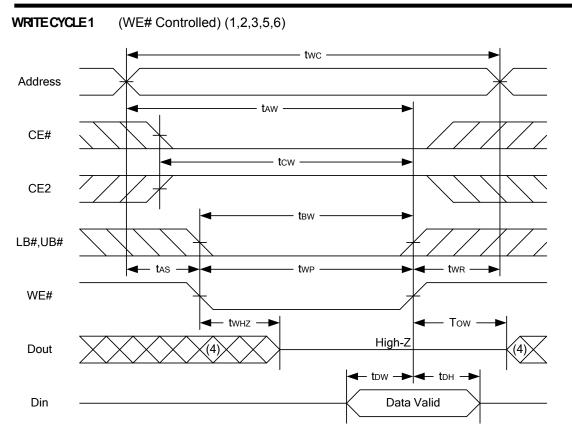
1.WE#is high for read cycle.

2.Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low

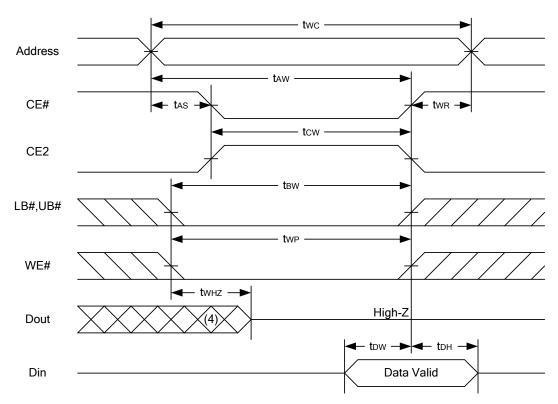
3.Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise tAA is the limiting parameter.

 $4.t_{CLZ}$ ,  $t_{BLZ}$ ,  $t_{CLZ}$ ,  $t_{CLZ}$ ,  $t_{CLZ}$ ,  $t_{CLZ}$ ,  $t_{BHZ}$  and  $t_{CHZ}$  are specified with  $C_{L} = 5pF$ . Transition is measured  $\pm 500 \text{mV}$  from steady state. 5.At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{BHZ}$  is less than  $t_{BLZ}$ ,  $t_{OHZ}$  is less than  $t_{CLZ}$ . AS6C1616





#### WRITE CYCLE2 (CE# ad CE2 Cotrolled) (1,2,5,6)



#### AS6C1616

FEBRUARY/2009, V1.a



(LB#,UB# Controlled) (1,2,5,6) twc Address taw 🗕 twr 🗕 CE# 🗲 tas 🖡 tcw CE2 tвw LB#,UB# twp WE# twnz High-Z Dout 4 - tow — 🛏 🗲 - **t**DH

Notes :

Din

1.WE#,CE#, LB#, UB# must be high or CE2 must be low during all address transitions. 2.A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.

3. During a WE# controlled write cycle with OE# low, twp must be greater than twHz + tow to allow the drivers to turn off and data to be placed on the bus.

Data Valid

4. During this period, I/O pins are in the output state, and input signals must not be applied.

5.If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.

6.tow and twHz are specified with  $C_L = 5pF$ . Transition is measured ±500mV from steady state.

WRITE CYCLE3



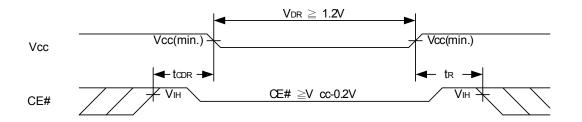
# DATA RETENTION CHARACTERISTICS

PARAMETER SYMBOL		TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	Vdr	CE# $\geq$ V <sub>CC</sub> - 0.2V or CE2 $\leq$ 0.2V	1.2	-	3.6	V	
Data Retention Current		Vcc = 1.2V CE# $\geq$ Vcc-0.2V or CE2 $\leq$ 0.2V	SLI	-	4	40	μA
Chip Disable to Data Retention Time		See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t <sub>R</sub>			t <sub>RC∗</sub>	_	-	ns

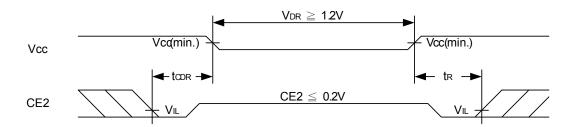
tRC∗ = Read Cycle Time

#### DATA RETENTION WAVEFORM

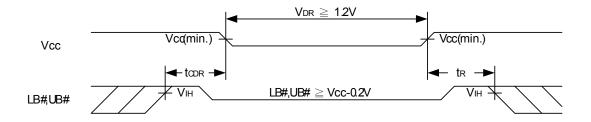
Low Vcc Data Retention Waveform (1) (CE# controlled)



Low Vcc Data Retention Waveform (2) (CE2 contribed)



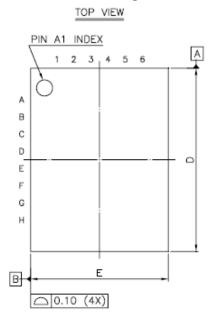
Low Vcc Data Retention Waveform (3) (LB#, UB#controlled)

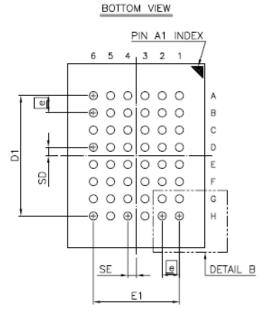




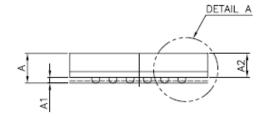
#### PACKAGE OUTLINE DIMENSION

#### 48-ball 6mm × 8mm TFBGA Package Outline Dimension

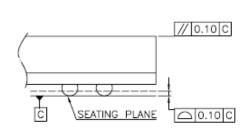




AS6C1616



SIDE VIEW



DIMENSION (inch)

NOM.

0.010

0.207 BSC

0.148 BSC

0.015 TYP

0.015 TYP

0.030 BSC

MAX.

0.055

0.012

0.041



MIN.

MAX.

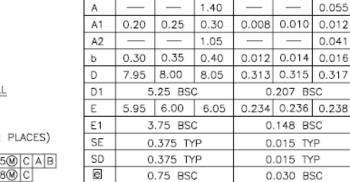
DIMENSION

(mm)

NOM.

\_

SOLDER BALL
Øb(48x PLACES) ⊕ 0.15@ C A B 0.08@ C



MIN.

SYM.

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.

2. REFERENCE DOCUMENT : JEDEC MO-207.

DETAIL B

FEBRUARY/2009, V1.a

#### Alliance Memory Inc.

# 1024K X 16 BIT LOW POWER CMOS SRAM

# **Ordering Information**

Alliance	Organization	VCC Range	Package	Operating Temp	Speed ns
AS6C1616-70BIN	1024K x 16	2.7 - 3.6V	48ball TFBGA	Industrial ~ -40 C – 85 C)	70
AS6C1616-55BIN	1024K x 16	2.7 - 3.6V	48ball TFBGA	Industrial ~ -40 C – 85 C)	55

# Part Numbering System

AS6C	1616	-70	Х	Х	N
low power SRAM prefix	Device Number 16 = 16M 16 = x16	Access Time	Package Option 48ball TFBGA	Temperature Range I = Industrial (-40 to + 85 C)	N = Lead Free RoHS compliant part





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Alliance Memory Inc.

# **AMEYA360** Components Supply Platform

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