#### **Power MOSFET**

## –20 V, –5.6 A, μCool™ Dual P–Channel, 2.0x2.0x0.55 mm UDFN Package

#### **Features**

- UDFN Package with Exposed Drain Pads for Excellent Thermal Conduction
- Low R<sub>DS(on)</sub>
- Low Profile UDFN 2.0x2.0x0.55 mm for Board Space Saving
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### **Applications**

- High Side Load Switch
- Reverse Current Protection
- Battery Switch
- Optimized for Power Management Applications for Portable Products, such as Cell Phones, PMP, DSC, GPS, and others

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter			Symbol	Value	Units
Drain-to-Source Voltage			$V_{DSS}$	-20	V
Gate-to-Source Vol	tage		V <sub>GS</sub>	±8.0	V
Continuous Drain	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	-4.4	Α
Current (Note 1)	State	T <sub>A</sub> = 85°C		-3.2	
	t ≤ 5 s	T <sub>A</sub> = 25°C		-5.6	
Power Dissipation (Note 1)	Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub>	1.4	W
	t ≤ 5 s	T <sub>A</sub> = 25°C	l	2.2	
Continuous Drain	Steady T <sub>A</sub> = 25°C		I <sub>D</sub>	-2.8	Α
Current (Note 2)	State	T <sub>A</sub> = 85°C		-2.0	
Power Dissipation (Note 2) T <sub>A</sub> = 25°C			$P_{D}$	0.5	W
Pulsed Drain Curre	Pulsed Drain Current tp = 10 μs			-13	Α
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C
ESD (HBM, JESD22-A114) (MM, JESD22-A114)			V <sub>ESD</sub>	1400 200	V
Source Current (Body Diode) (Note 2)			I <sub>S</sub>	-1.0	Α
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

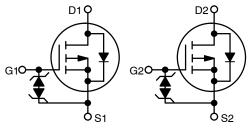
- Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces) based on both FETs on.
- Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm<sup>2</sup>, 1 oz. Cu based on both FETs on.



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MOSFET				
V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX		
	50 mΩ @ -4.5 V			
-20 V	70 mΩ @ -2.5 V	-5.6 A		
20 1	115 mΩ @ –1.8 V	0.071		
	175 mΩ @ -1.5 V			



P-Channel MOSFET

#### MARKING DIAGRAM



UDFN6 CASE 517BF μCOOL™



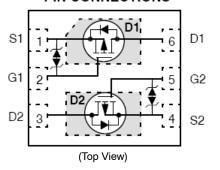
AA = Specific Device Code

M = Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

#### PIN CONNECTIONS



#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

#### THERMAL RESISTANCE RATINGS

Parameter		Max	Units
Junction-to-Ambient – Steady State (Note 3)		91	°C/W
Junction-to-Ambient – t ≤ 5 s (Note 3)		57	
Junction-to-Ambient – Steady State min Pad (Note 4)		228	

#### **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Units
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>I</sub>	ο = -250 μΑ	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	I <sub>D</sub> = -250 μA	., ref to 25°C		-13		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = -20 \text{ V}$	T <sub>J</sub> = 25°C			-1.0	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V	r <sub>GS</sub> = ±5.0 V			±5.0	μΑ
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}$	I <sub>D</sub> = -250 μA	-0.4		-1.0	V
Negative Threshold Temp. Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				3.0		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 \	/, I <sub>D</sub> = -4.0 A		37	50	mΩ
		V <sub>GS</sub> = -2.5 \	/, I <sub>D</sub> = -3.0 A		46	70	1
		V <sub>GS</sub> = -1.8 \	/, I <sub>D</sub> = -2.0 A		63	115	1
		V <sub>GS</sub> = -1.5 \	/, I <sub>D</sub> = -1.0 A		86	175	1
Forward Transconductance	9FS	$V_{DS} = -5.0 \text{ V}, I_D = -3.0 \text{ A}$			16		S
CHARGES AND CAPACITANCES							
Input Capacitance	C <sub>ISS</sub>	$V_{GS} = 0 \text{ V, f} = 1 \text{ MHz,} $ $V_{DS} = -15 \text{ V}$			920		pF
Output Capacitance	C <sub>OSS</sub>				85		1
Reverse Transfer Capacitance	C <sub>RSS</sub>				80		1
Total Gate Charge	Q <sub>G(TOT)</sub>				10.4		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	$V_{GS} = -4.5 \text{ V}, V_{DS} = -15 \text{ V};$ $I_{D} = -3.0 \text{ A}$			0.5		1
Gate-to-Source Charge	$Q_{GS}$				1.2		1
Gate-to-Drain Charge	$Q_{GD}$				3.0		1
SWITCHING CHARACTERISTICS, VO	S = 4.5 V (Note 6	6)		-	-	-	-
Turn-On Delay Time	t <sub>d(ON)</sub>	$V_{GS} = -4.5 \text{ V}, V_{DD} = -15 \text{ V}, \\ I_{D} = -3.0 \text{ A}, R_{G} = 1 \Omega$			7.0		ns
Rise Time	t <sub>r</sub>				12		1
Turn-Off Delay Time	t <sub>d(OEE)</sub>				39		1

Turn-On Delay Time	t <sub>d(ON)</sub>		7.0	ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DD</sub> = -15 V,	12	
Turn-Off Delay Time	t <sub>d(OFF)</sub>	$I_D = -3.0 \text{ A}, R_G = 1 \Omega$	39	
Fall Time	t <sub>f</sub>		30	

#### **DRAIN-SOURCE DIODE CHARACTERISTICS**

Forward Diode Voltage	VSD	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -1.0 A	T <sub>J</sub> = 25°C	-0.67	-1.0	V
		I <sub>S</sub> = -1.0 A	T <sub>J</sub> = 125°C	-0.56		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dis/dt = 100 A/μs, I <sub>S</sub> = -1.0 A		12.1		ns
Charge Time	t <sub>a</sub>			6.4		
Discharge Time	t <sub>b</sub>	I <sub>S</sub> = -	1.0 A	5.7		
Reverse Recovery Charge	Q <sub>RR</sub>			4.0		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

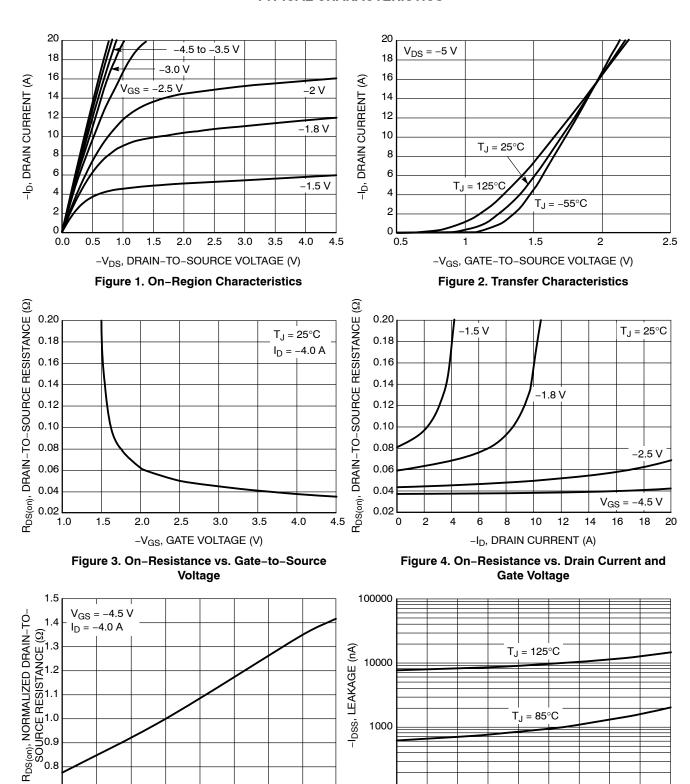
3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces) based on both FETs on.

4. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 1 oz. Cu based on both FETs on.

5. Pulse Test: pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2%.

6. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS**



T<sub>J</sub>, JUNCTION TEMPERATURE (°C)

Figure 5. On-Resistance Variation with

Temperature

0.7

-50

-25

Figure 6. Drain-to-Source Leakage Current vs. Voltage

-V<sub>DS</sub>, DRAIN-TO-SOURCE VOLTAGE (V)

#### **TYPICAL CHARACTERISTICS**

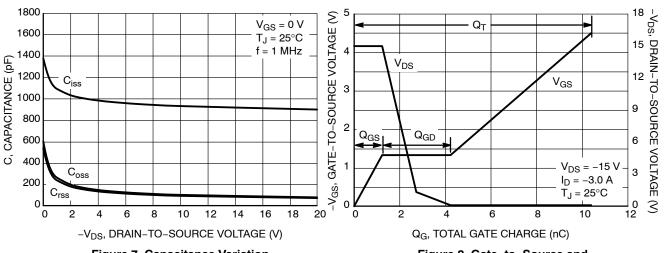


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

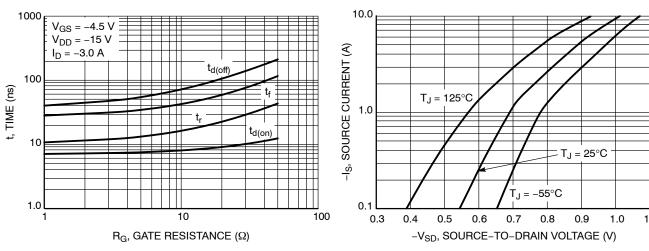


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

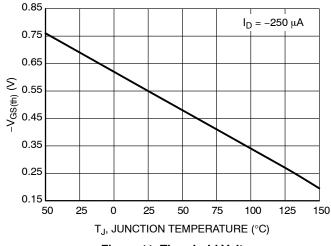


Figure 11. Threshold Voltage

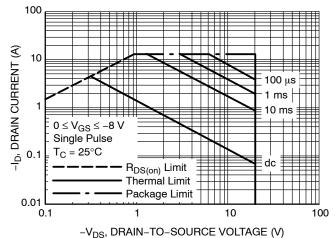


Figure 12. Maximum Rated Forward Biased Safe Operating Area

#### **TYPICAL CHARACTERISTICS**

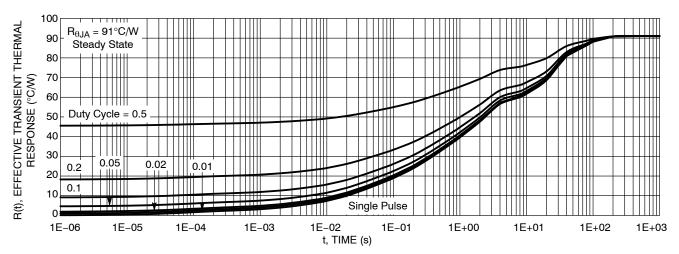


Figure 13. FET Thermal Response

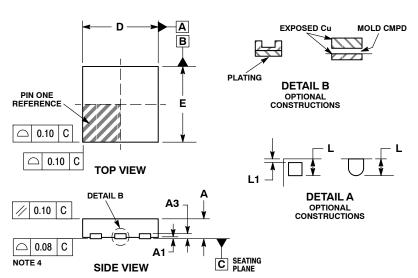
#### **DEVICE ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTLUD3A50PZTAG	UDFN6 (Pb-Free)	3000 / Tape & Reel
NTLUD3A50PZTBG	UDFN6 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

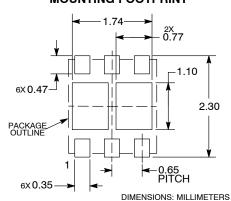
#### UDFN6 2x2, 0.65P CASE 517BF **ISSUE B**

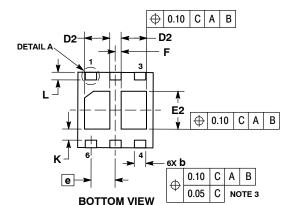


- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS.
  DIMENSION b APPLIES TO PLATED
- TERMINAL AND IS MEASURED BETWEEN
  0.15 AND 0.30 mm FROM THE TERMINAL TIP.
- COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

TABAG WELEARD THE TERM				
	MILLIMETERS			
DIM	MIN	MAX		
Α	0.45	0.55		
A1	0.00	0.05		
A3	0.13	REF		
b	0.25	0.35		
D	2.00 BSC			
D2	0.57	0.77		
E	2.00 BSC			
E2	0.90	1.10		
е	0.65	BSC		
F	0.15 BSC			
K	0.25 REF			
L	0.20	0.30		
L1		0.10		

#### **RECOMMENDED** MOUNTING FOOTPRINT





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