An 8-V to 18-V Input, 20-V to 35-V Output, 700-mA Non-Synchronous Boost Current Regulator for LED Drive

1 Introduction

The TPS40211EVM-352 evaluation module (EVM) is a fixed frequency, (300 kHz), non-synchronous boost converter providing fixed 700-mA output at 20 V to 35 V from a 8-V to 18-V input source. The EVM is designed to start up from a single supply, so no additional bias voltage is required for start-up. The module uses the TPS40211 Non-Synchronous Current Mode Control Boost Controller with integral N-channel FET driver.

1.1 Description

TPS40211EVM-352 is designed to use a loosely regulated 12-V (8 V to 18 V) source to produce a regulated current driver at 700 mV for constant current loads such as high-brightness LEDs. TPS40211EVM-352 is designed to demonstrate the TPS40211 in a typical LED Driver for 6 to 10 LEDs while providing a number of test points to evaluate the performance of the TPS40211 in a given application. The EVM can be modified to other input voltages or output currents by changing some of the components.

1.2 Applications

- High-Current LED Drivers
- LED Lighting Solutions
- LED Backlighting

1.3 Features

- 8-V to 18-V Input Range
- 700-mV Fixed Output Current, Adjustable with 1210 Package Resistor Change
- 42-V Open Circuit Protection
- 300-kHz Switching Frequency
- Single SO-8 Switching MOSFET and Rectifier Diode.
- Double Sided 2-Layer PCB With All Components On Top Side
- Active Converter Area 1.25" × 1.25" (less than 1.6 in^2)
- Convenient Test Points for Probing Output Voltage, Current Sense, Switching Waveforms and Non-Invasive Loop Response Testing

2 TPS40211EVM-352 Electrical Performance Specifications

Table 1. Electrical and Performance Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Input Characteristics						
V_{IN}	Input voltage		8	12	18	V
I_{IN}	Input current	V_{IN} = nom, I_{OUT} = max	–	1.6	2.0	A
	No load input current	V_{IN} = nom, I_{OUT} = 0 A	–	12	20	mA
V_{IN_UVLO}	Input UVLO	I_{OUT} = 100 mA	4.0	4.2	4.4	V
Output Characteristics						
I_{OUT}	Output current	V_{IN} = nom, V_{OUT} = 30 V	679	–	721	mA
	Line regulation	V_{IN} = min to max	–	–	1%	
	Load regulation	V_{OUT} = min to max	–	–	1%	
V_{OUT_ripple}	Output voltage ripple	V_{IN} = nom, I_{OUT} = max	–	–	500	mVpp
V_{OUT}	Output voltage	V_{IN} = min to max	20		35	A
V_{OCP}	Output over voltage	V_{IN} = nom, IOUT = I_{OUT2}- 5%	40	42	45	
Systems Characteristics						
F_{SW}	Switching frequency		240	300	360	kHz
ηpk	Peak efficiency	V_{IN} = nom	–	94%	–	
η	Full load efficiency	V_{IN} = nom, V_{OUT} = max	–	93%	–	

3 Schematic

For reference only, See Table 3 List of Materials for specific values.

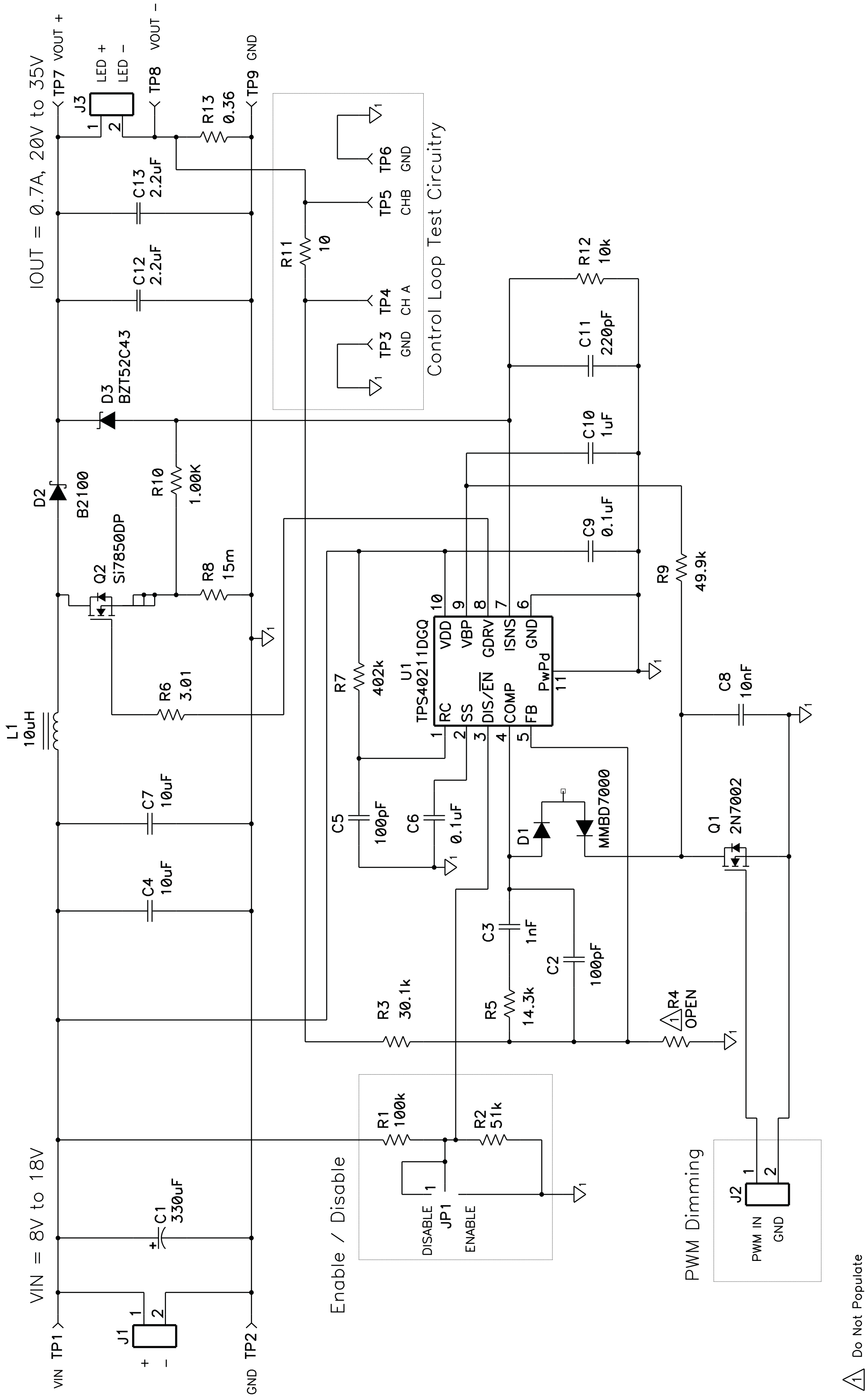

Figure 1. TPS40211EVM-352 Schematic

3.1 Enable Jumper (JP1)

TPS40211EVM-352 provides a 3-pin 100-mil header and shunt for exercising the TPS40211 Enable function. When the JP1 shunt is removed, R1 and R2 pull up on the TPS40211 inverted Enable and turn OFF the TPS40211 switcher. Inserting a shunt in the DOWN (Enable) position pulls the TPS40211 inverted Enable to ground and turns ON the TPS40210 Output. Due to diode D1, when the TPS40211 is “OFF” the output voltage will be maintained within 500mV of the input voltage.

3.2 Inverted PWM Dimming Input (J2)

TPS40211EVM-352 provides a 2-terminal input for a 5-V Logic PWM dimming the output current generated at the output terminal block (J3). Pin 2 is connected to the PCB ground. When a logic 1 is forced on Pin 1, the TPS40211 control voltage is forced low and no switching occurs. Due to diode D1, when no switching occurs, the output voltage will be maintained withing 500 mV of the input voltage. When a logic 0 is forced on P1, the TPS40211 control voltage is released and the current at the output terminal block (J3) is regulated.

This allows the user to provide an inverted PWM dimming signal to the EVM. Due to limitations in the bandwidth of the EVM, the minimum ON and minimum OFF times should be maintained above 100us.

3.3 Test Point Descriptions

Table 2. Test Point Descriptions

TEST POINT	LABLE	USE	SECTION
TP1	VIN	Monitor input voltage	Section 3.3.1
TP2	GND	Ground for input voltage	Section 3.3.1
TP3	GND	Ground for Channel A loop monitoring	Section 3.3.2
TP4	CH A	Channel A for loop monitoring	Section 3.3.2
TP5	CH B	Channel B for loop monitoring	Section 3.3.2
TP6	GND	Ground for Channel B loop monitoring	Section 3.3.2
TP7	VOUT +	Monitor positive output voltage (anode)	Section 3.3.3
TP8	VOUT–	Monitor negative output voltage (cathode)	Section 3.3.3
TP9	GND	Ground for output and current sense monitor	Section 3.3.3

3.3.1 Input Voltage Monitoring (TP1 and TP2)

TPS40211EVM-352 provides two test points for measuring the voltage applied to the module. This allows the user to measure the actual module voltage without losses from input cables and connectors. All input voltage measurements should be made between TP1 and TP2. To use TP1 and TP2, connect a voltmeter positive terminal to TP1 and negative terminal to TP2.

3.3.2 Loop Analysis (TP3, TP4, TP5 and TP6)

TPS40211EVM-352 contains a 10-Ω series resistor (R11) in the feedback loop to allow for signal injection into the feedback for loop response analysis. An isolation transformer should be used to apply a small (15 mV or less) signal across R11 through TP4 and TP5. By monitoring the ac injection level at TP4 and the returned ac level at TP5, the power supply loop response can be determined.

3.3.3 Output Voltage Monitoring (TP7, TP8 and TP9)

TPS40211EVM-352 provides two test points for measuring the voltage generated by the module. This allows the user to measure the actual module output voltage without losses from output cables and connectors. All output voltage measurements should be made between TP7 and TP8. To use TP7 and TP8, connect a voltmeter positive terminal to TP7 and negative terminal to TP8. Do not connect an oscilloscope ground to TP8, this will short the current sense to ground and may damage the EVM, Load or oscilloscope probe.

4 Test Set Up

4.1 Equipment

4.1.1 Voltage Source

V_{IN}

The input voltage source (V_{IN}) should be a 0-V to 18-V variable dc source capable of 4 A_{DC}. Connect V_{IN} to J1 as shown in Figure 2.

4.1.2 Meters

A1: 0 to 4 A_{DC}, ammeter
A2: 0 to 1 A_{DC}, ammeter
V1: V_{IN}, 0 V to 18 V voltmeter
V2: V_{OUT} 0 V to 45 V voltmeter

4.1.3 Loads

LOAD1

The Output1 Load (LOAD1) should be an electronic load in constant voltage or constant resistance mode capable of 0 V_{DC} to 45 V_{DC} at 700 mA or 6–10 series high brightness LEDs capable of handling 700 mA of diode current.

4.1.4 Oscilloscope

Oscilloscope
A digital or analog oscilloscope can be used to measure the ripple voltage on V_{OUT}. The oscilloscope should be set for 1-MΩ impedance, 20-MHz bandwidth, ac coupling, 1-µs/division horizontal resolution, 10-mV/division vertical resolution for taking output ripple measurements. TP7 and TP9 can be used to measure the output ripple voltages by connecting the oscilloscope probe to TP7 and connecting the ground clip TP9. Using a leaded ground connection may induce additional noise due to the large ground loop area, but the ground barrel of the oscilloscope probe should not be connected to TP8.

4.1.5 Recommended Wire Gauge

VIN to J1
The connection between the source voltage, VIN and J1 of HPA289 can carry as much as 48 A_{DC}. The minimum recommended wire size is AWG #16 with the total length of wire less than 4 feet (2 feet input, 2 feet return). J3 to LOAD1.

The power connection between J3 of HPA352 and LOAD1 can carry 700 mA_{DC}. The minimum recommended wire size is AWG #18, with the total length of wire less than 2 feet (1 foot output, 1 foot return).

4.1.6 Other

FAN
This evaluation module includes components that can get hot to the touch, because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200 lfm is recommended to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered. The EVM should not be probed while the fan is not running.

4.2 Equipment Setup

Shown in Figure 2 is the basic test set up recommended to evaluate the TPS40211EVM-352. Note that the return for J1 and JP3 are not the same system ground. The connections should remain separate as shown in Figure 2.

4.2.1 Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the dc input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 4.0 A maximum. Make sure V_{IN} is initially set to 0 V and connected as shown in Figure 2.
3. Connect the ammeter A1 (0 A to 4 A range) between V_{IN} and J1 as shown in Figure 2.
4. Connect voltmeter V1 to TP1 and TP2 as shown in Figure 2.
5. Connect LOAD1 to J3 as shown in Figure 2. Set LOAD1 to constant current mode to sink 0 A_{DC} before V_{IN} is applied.
6. Connect voltmeter, V2 across TP7 and TP8 as shown in Figure 2.
7. Place fan as shown in Figure 3 and turn on, making sure air is flowing across the EVM.

4.2.2 Diagram

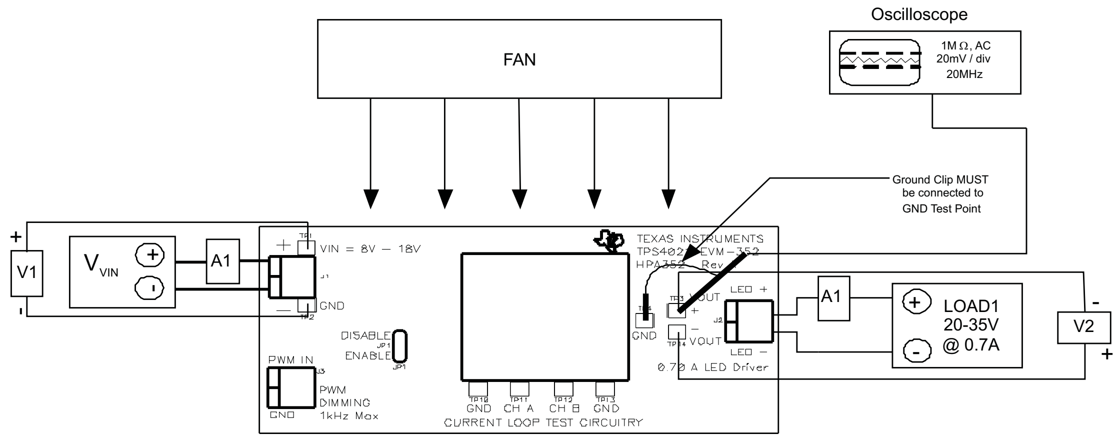

Figure 2. TPS40211EVM-352 Recommended Test Set-Up

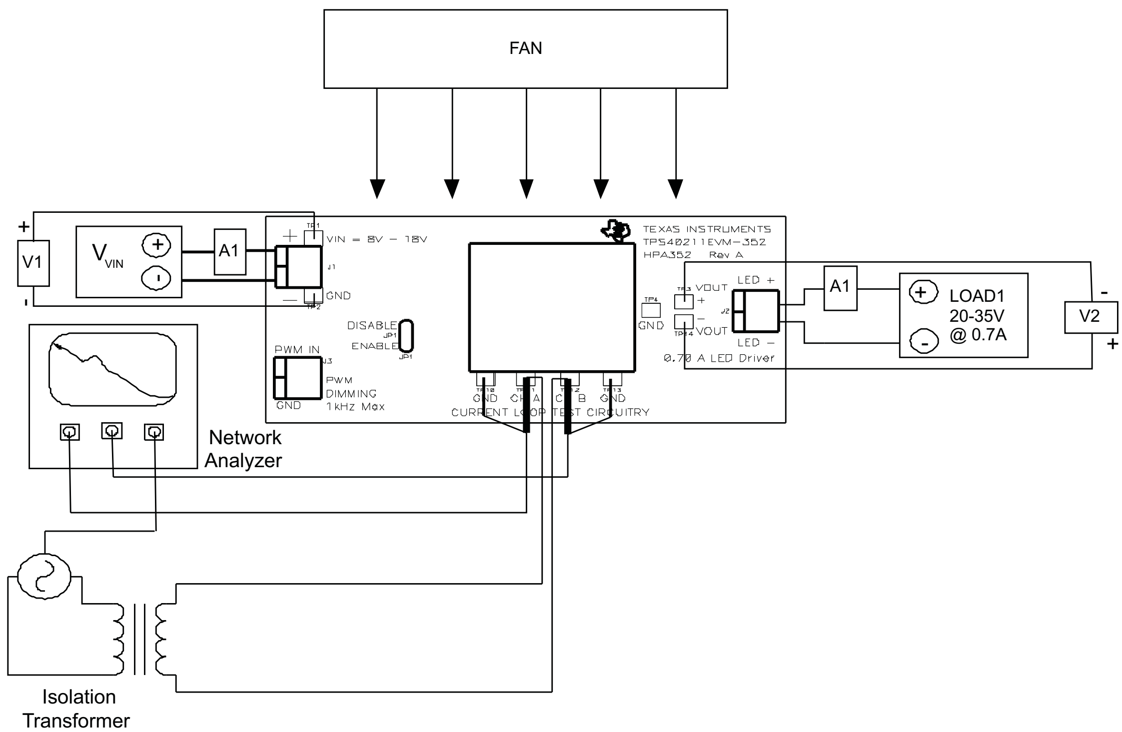

Figure 3. Control Loop Measurement Setup

4.3 Start Up/Shut Down Procedure

1. Increase V_{IN} from 0 V to 12 V_{DC}.
2. Vary LOAD1 from 20 V to 35 V_{DC}.
3. Vary V_{IN} from 8 V_{DC} to 18 V_{DC}.
4. Decrease V_{IN} to 0 V_{DC}.
5. Decrease LOAD1 to 0 V.

4.4 Output Ripple Voltage Measurement Procedure

1. Increase V_{IN} from 0 V to 12 V_{DC}.
2. Adjust LOAD1 to desired load between 0 A_{DC} and 2 A_{DC}.
3. Adjust V_{IN} to desired load between 8 V_{DC} and 14 V_{DC}.
4. Connect oscilloscope probe to TP14 and TP15 as shown in Figure 2.
5. Measure output ripple
6. Decrease V_{IN} to 0 V_{DC}.
7. Decrease LOAD1 to 0 A

4.5 Control Loop Gain and Phase Measurement Procedure

1. Connect 1-kHz to 1-MHz isolation transformer to TP4 and TP5 as show in Figure 4
2. Connect input signal amplitude measurement probe (Channel A) to TP4 as shown in Figure 4
3. Connect output signal amplitude measurement probe (Channel B) to TP5 as shown in Figure 4
4. Connect ground lead of Channel A and Channel B to TP3 and TP6 as shown in Figure 4
5. Inject 15 mV or less signal across R11 through isolation transformer
6. Sweep frequency from 1 kHz to 1 MHz with 10 Hz or lower post filter
7. Control Loop Gain can be measured by : $20 \times \mathrm{LOG}\left(\frac{\mathrm{ChannelB}}{\mathrm{ChannelA}}\right)$
8. Control Loop Phase is measured by the phase difference between Channel A and Channel B
9. Disconnect isolation transformer before making any other measurements (signal injection into feedback may interfere with accuracy of other measurements)

4.6 Equipment Shutdown

1. Shut down OSCILLOSCOPE
2. Shut down V_{IN}
3. Shut down LOAD1
4. Shut down FAN

5 TPS40211EVM-352 Typical Performance Data and Characteristic Curves

Figure 4 through Figure 10 present typical performance curves for the TPS40211EVM-352. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

5.1 Efficiency

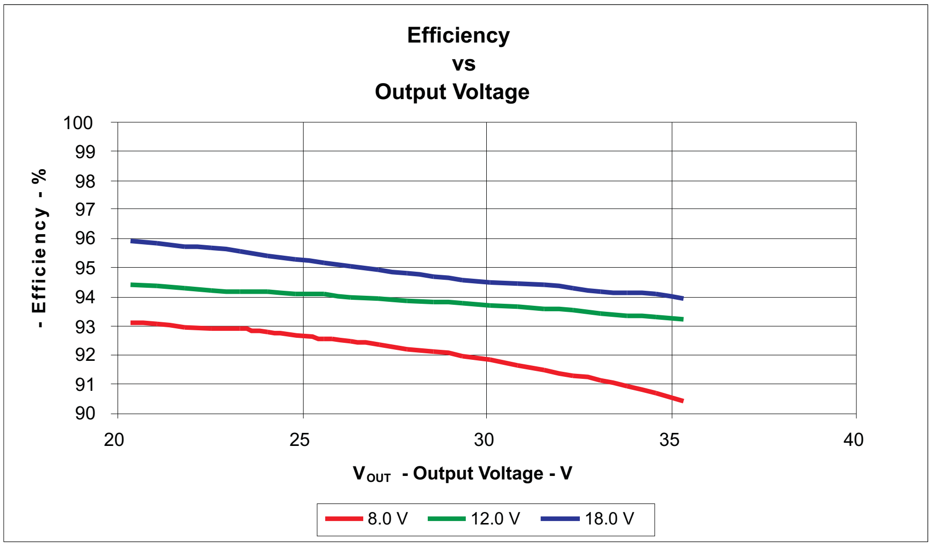

Figure 4. TPS40211EVM-352 Efficiency verse Output Voltage
V_{IN} = 8 V to 18 V, I_{OUT} = 0.70 A, V_{OUT} = 20 V to 35 V

5.2 Line and Load Regulation

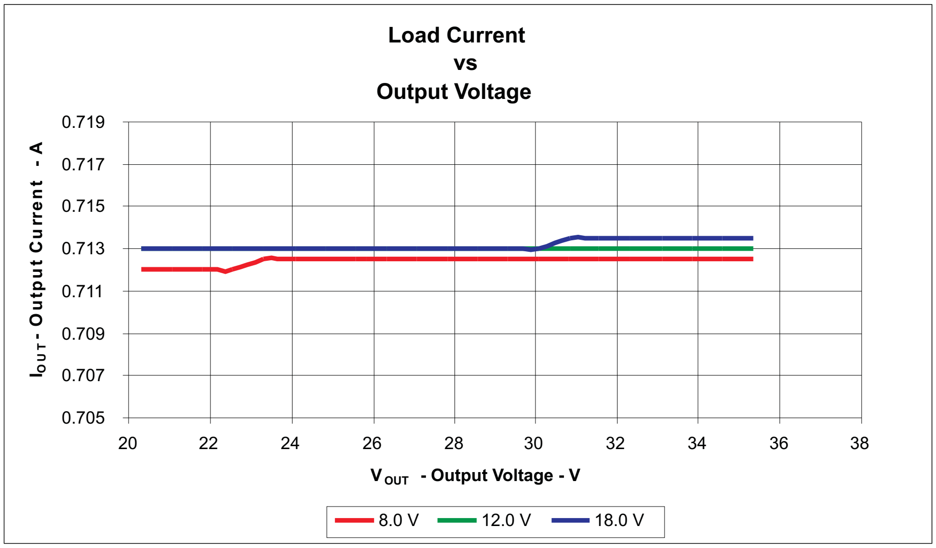

Figure 5. TPS40211EVM-352 Load Current verse Output Voltage
V_{IN} = 8 V to 18 V, I_{OUT} = 0.70 A, V_{OUT} = 20 V to 35 V

5.3 Output Voltage Ripple

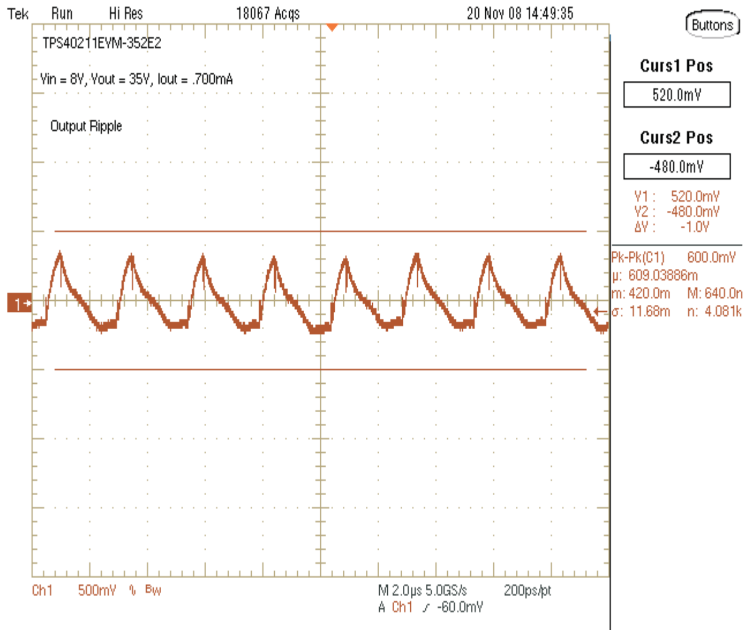

Figure 6. TPS40211EVM-352 Output Voltage Ripple
V_{IN} = 8 V, I_{OUT} = 0.70 A, V_{OUT} = 35 V

5.4 Switch Node

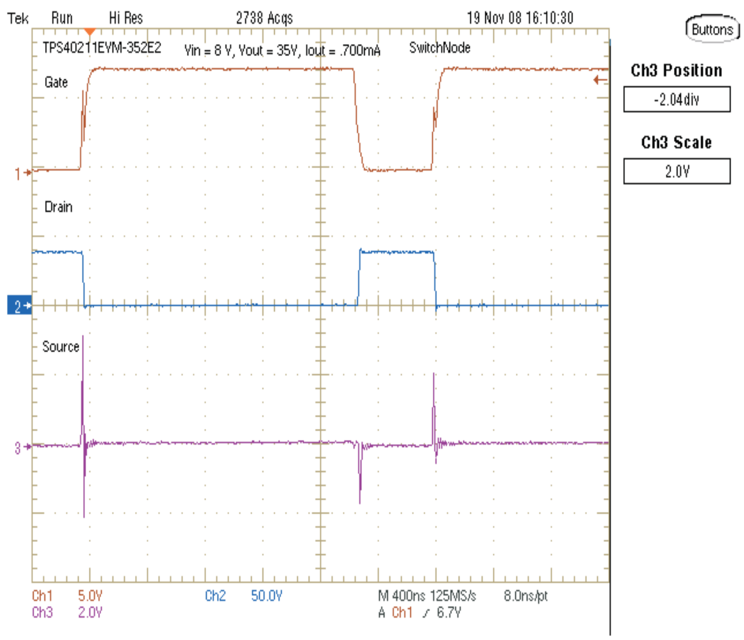

Figure 7. TPS40211EVM-352 Switching Waveforms
V_{IN} = 8 V, I_{OUT} = 0.70 A, V_{OUT} = 35 V,
Ch1: GATE, Ch2: TP9 DRAIN, Ch3: SOURCE

5.5 Control Loop Bode Plot

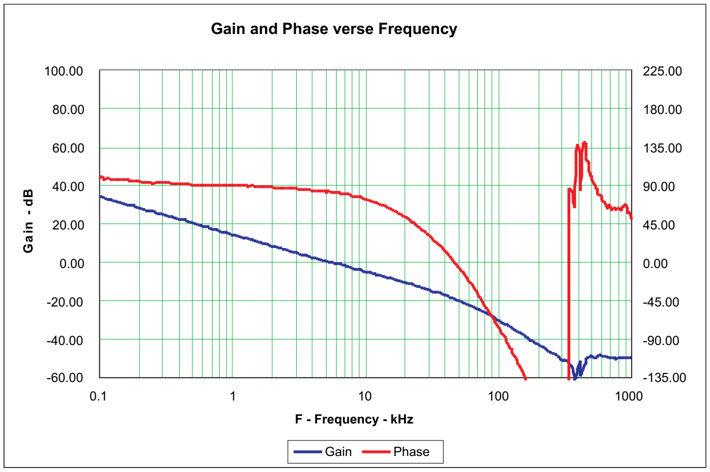

Figure 8. TPS40211EVM-352 Gain and Phase verse Frequency
V_{IN} = 12 V, I_{OUT} = 0.70 A VOUT = 24 V (8 white LEDs)
V_{OUT}: Bandwidth: 5.7 kHz Phase Margin: 82°

5.6 Start Up and Soft-Start

In a BOOST power stage, the rectifier diode connected the input voltage to the output voltage. During shut-down, disable, UVLO and the start-up delay, this diode connects the input to the output, producing a plateau soft-state waveform. This is normal and an unavoidable result of the BOOST topology. When starting into a constant voltage load there will be some over-shoot as the TPS40211 tries to regulate a load current into a load that draws no current until the constant voltage is exceeded. If open circuit protection is exceeded, the controller will shut down for 60 ms and then attempt a restart. (See Figure 9)

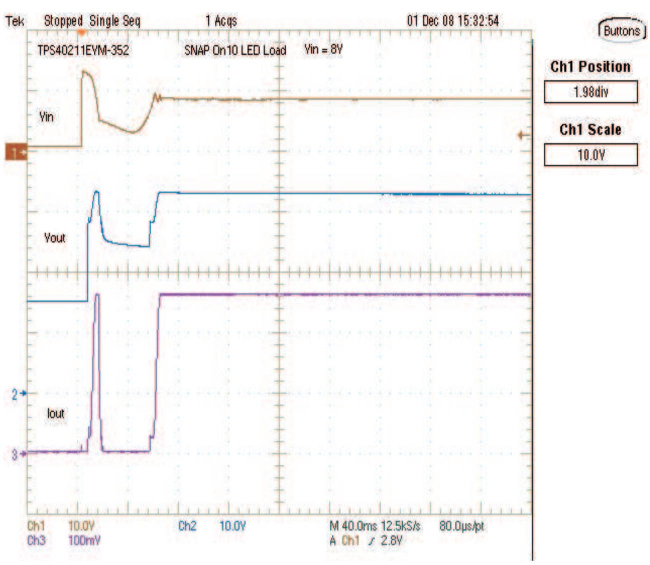

Figure 9. TPS40211EVM-352 Power ON (UVLO) Soft-Start
V_{IN} = 8 V, I_{OUT} = 0.70 A,
V_{OUT} = 32 V (10 white LEDs)

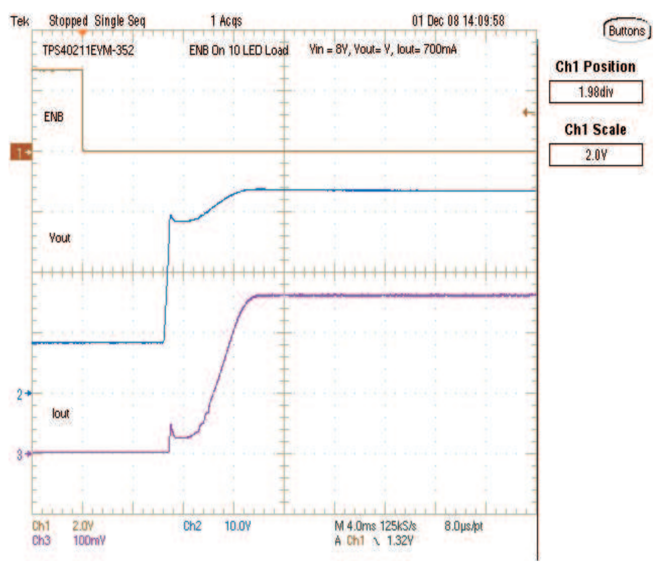

Figure 10. TPS40211EVM-352 Enable ON Soft-Start
V_{IN} = 8 V, I_{OUT} = 0.70 A, V_{OUT} = 32 V (10 LEDs)

6 EVM Assembly Drawings and Layout

The following (Figure 11 through Figure 14) shows the design of the TPS40211EVM-352 printed circuit board. The EVM has been designed using a 2-Layer, 2-oz copper-clad circuit board 2.0" × 4.0" with all components in a 1.25" × 1.25" active area on the top side and all traces to the top and bottom layers to allow the user to easily view, probe and evaluate the TPS40211 control device in a practical double-sided application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

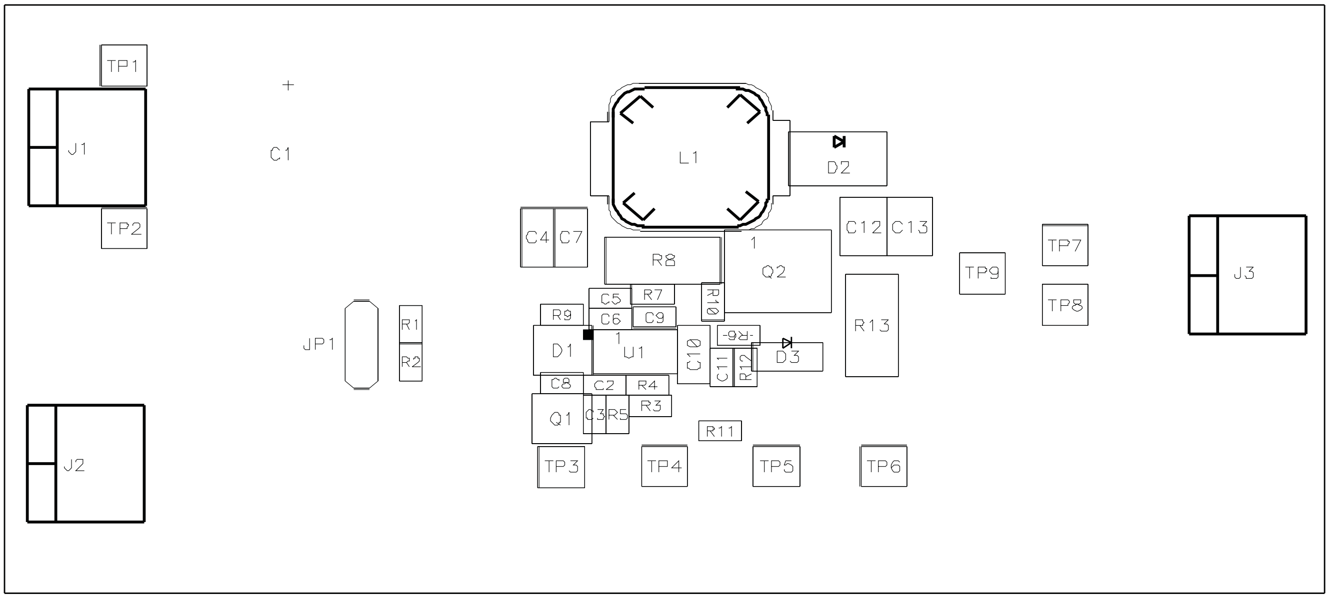

Figure 11. TPS40211EVM-352 Component Placement (viewed from top)

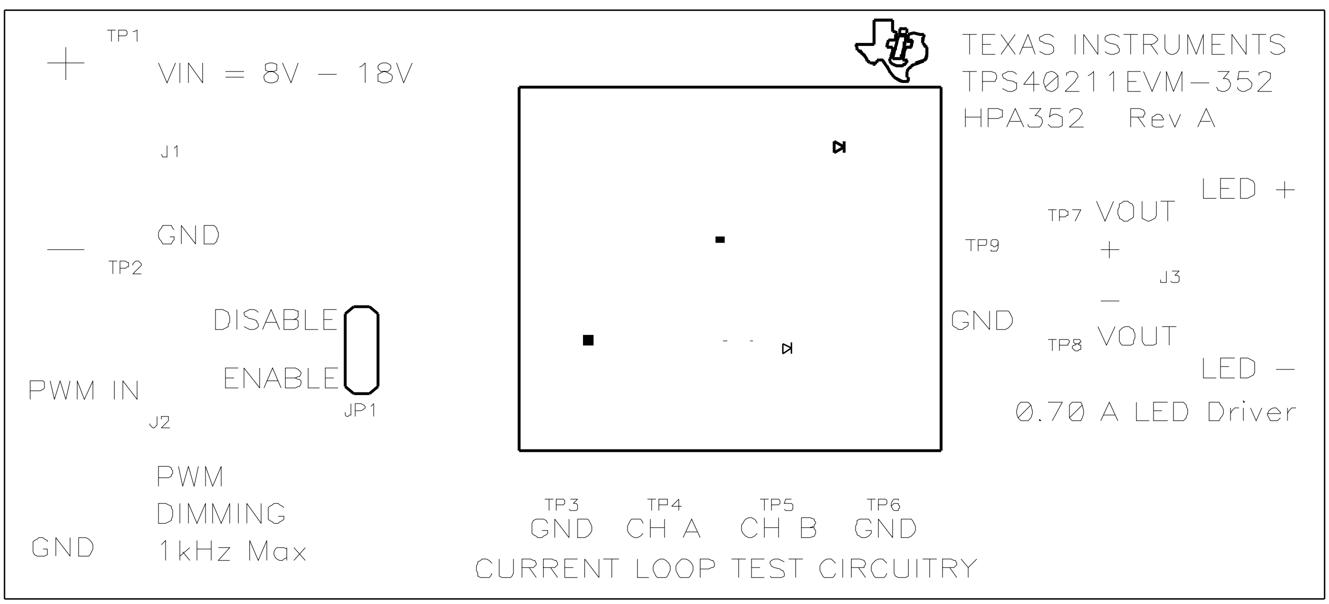

Figure 12. TPS40211EVM-352 Silkscreen (viewed from top)

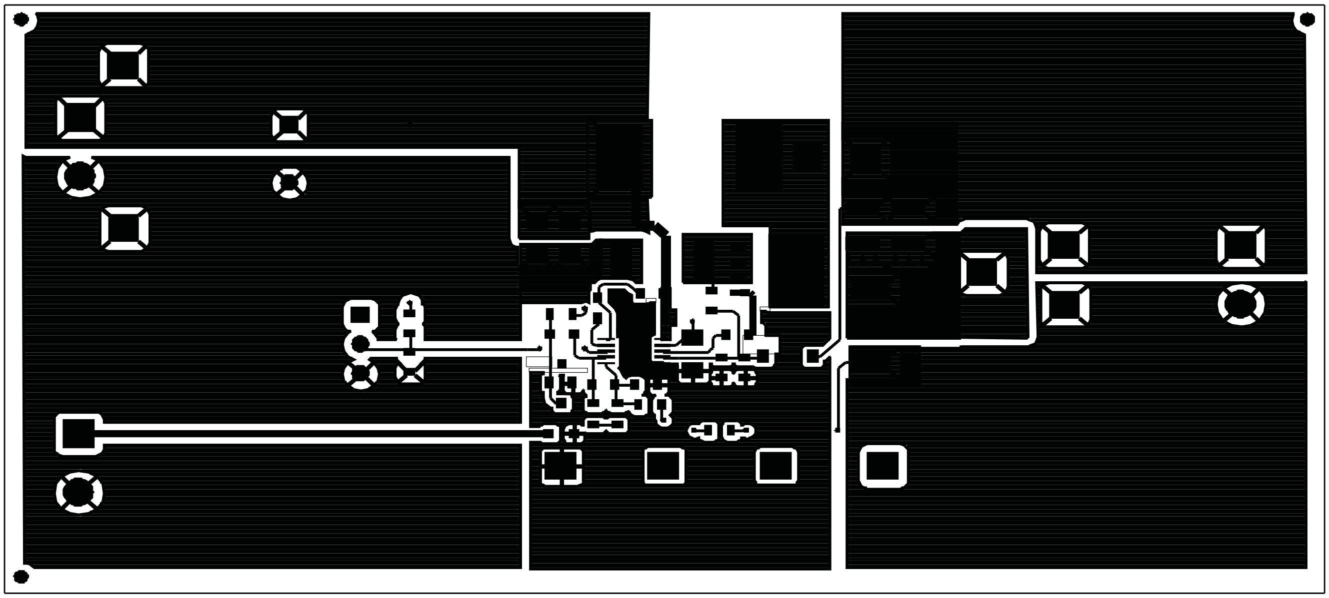

Figure 13. TPS40211EVM-352 Top Copper (viewed from top)

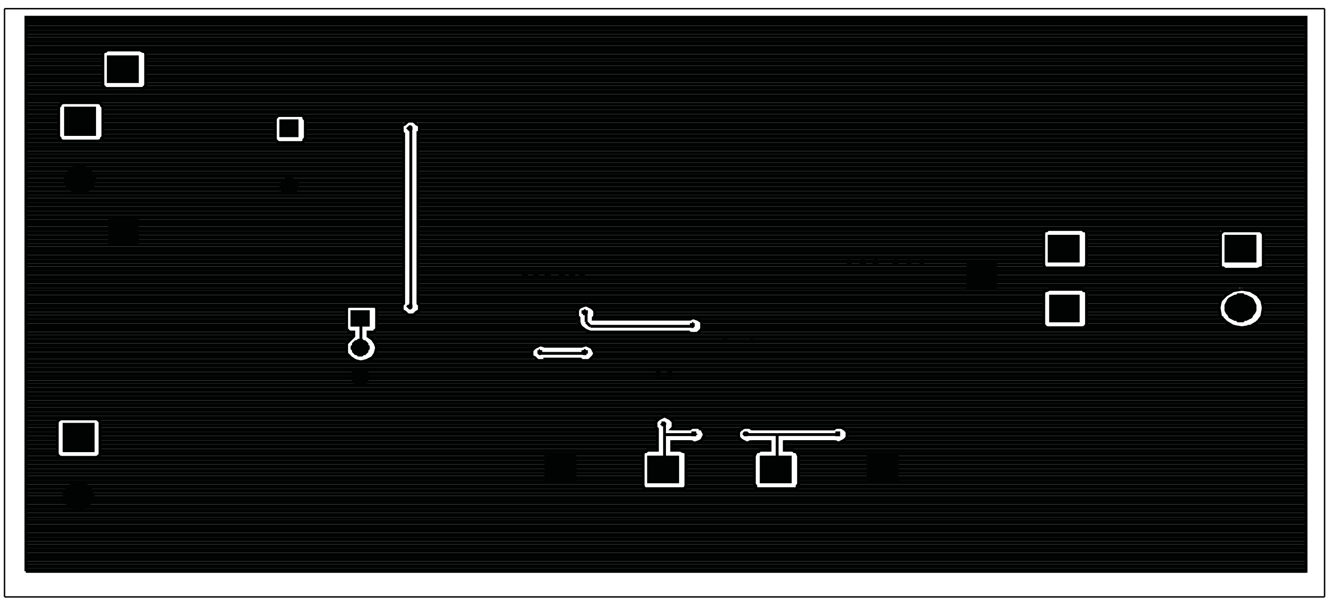

Figure 14. TPS40211EVM-352 Bottom Copper (x-ray view from top)

7 List of Materials

Table 3 lists the EVM components as configured according to the schematic shown in Figure 1.

Table 3. TPS40211EVM-352 List of Materials

Qty	RefDes	Description	Part No.	MFR
1	C1	Capacitor, aluminum, vvV, 20% (FC Series), 330 µF, 10×12,5 mm	EEUFC1E331	Panasonic
1	C10	Capacitor, ceramic, 25V, X7R, 10%, 1 µF, 1206	Std	Std
1	C11	Capacitor, ceramic, 50V, C0G, 5%, 220 pF, 0603	Std	Std
2	C12, C13	Capacitor, ceramic, 100V, X7R, 10%, 2.2 µF, 1210	Std	Std
2	C2, C5	Capacitor, ceramic, 50V, C0G, 5%, 100 pF, 0603	Std	Std
1	C3	Capacitor, ceramic, 50V, C0G, 5%, 1nF, 0603	Std	Std
2	C4, C7	Capacitor, ceramic, 25V, X5R, 10%, 10 µF , 1206	Std	Std
2	C6, C9	Capacitor, ceramic, 25V, X7R, 10%, 0.1 µF, 0603	Std	Std
1	C8	Capacitor, ceramic, 25V, X7R, 10%, 10 nF, 0603	Std	Std
1	D1	Diode, dual small signal, 200-mA, 100-V, SOT23	MMBD7000	Std
1	D2	Diode, Schottky, 2-A, 100-V, SMB	B2100	Std
1	D3	Diode, Zener, Planar Power, 500mW, 43V, SOD-123	BZT52C43	Std
3	J1, J2, J3	Terminal block, 2-pin, 15-A, 5,1mm, 0.40 × 0.35 inch	D120/2DS	OST
1	JP1	Header, 3-pin, 100mil spacing, (36-pin strip), 0.100 inch ×3	PTC36SAAN	Sullins
1	L1	Inductor, SMT, 6.04A, 17.2 mΩ, 10 µH, 0.492 sq"	DR127-100-R	Coiltronics
1	Q1	MOSFET, N-ch, 60-V, 115-mA, 7.5-Ω, SOT23	2N7002	Std
1	Q2	MOSFET, NChannel, 60V, 10.3 A, 0.022 mΩ, PWRPAK, S0-8	Si7850DP	Vishay
1	R1	Resistor, chip, 1/16W, 5%, 100 kΩ, 0603	Std	Std
1	R10	Resistor, chip, 1/16W, 1%, 1.00 kΩ, 0603	Std	Std
1	R11	Resistor, chip, 1/16W, 5%, 10 Ω, 0603	Std	Std
1	R12	Resistor, chip, 1/16W, 5%, 10 kΩ, 0603	Std	Std
1	R13	Resistor, chip, 1W, 1%, 0.36 Ω, 2512	Std	Std
1	R2	Resistor, chip, 1/16W, 5%, 51 kΩ, 0603	Std	Std
1	R3	Resistor, chip, 1/16W, 1%, 30.1 kΩ, 0603	Std	Std
0	R4	Resistor, chip, 1/16W, x%, open, 0603	Std	Std
1	R5	Resistor, chip, 1/16W, 1%, 14.3 kΩ, 0603	Std	Std
1	R6	Resistor, chip, 1/16W, 1%, 3.01 Ω, 0603	Std	Std
1	R7	Resistor, chip, 1/16W, 1%, 402 kΩ, 0603	Std	Std
1	R8	Resistor, chip, 1W, 5%, 15 m, 2512	Std	Std
1	R9	Resistor, chip, 1/16W, 1%, 49.9 kΩ, 0603	Std	Std
2	TP1,TP7	Test point, red, thru hole, 0.125 × 0.125 inch	5010	Keystone
4	TP2, TP3, TP6, TP9	Test point, black, thru hole, 0.125 × 0.125 inch	5011	Keystone
	TP4, TP5, TP8	Test point, white, thru hole , 0.125 × 0.125 inch	5012	Keystone
1	U1**	IC, 4.5V-52V I/P, Current Mode Boost Controller, DGQ10	TPS40211DGQ	TI
1	—	PCB, 3 In x 3 In x 0.063 In,	HPA352	Any
1	—	Shunt, 100-mil, black, 0.100	929950-00	3M

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