16-Bit, 1.5 LSB INL, 250 kSPS PulSAR Differential ADC in MSOP

Data Sheet **AD7687**

FEATURES

16-bit resolution with no missing codes
Throughput: 250 kSPS
INL: ±0.4 LSB typ, ±1.5 LSB max (±23 ppm of FSR)
Dynamic range: 96.5 dB
S/(N + D): 95.5 dB at 20 kHz
THD: −118 dB at 20 kHz
True differential analog input range
  $\pm V_{REF}$
  0 V to V_{REF} with V_{REF} up to VDD on both inputs
No pipeline delay
Single-supply 2.3 V to 5.5 V operation with
  1.8 V/2.5 V/3 V/5 V logic interface
Proprietary serial interface: SPI-/QSPI™-/MICROWIRE™-/DSP-compatible
Daisy-chain multiple ADCs and BUSY indicator
Power dissipation
  1.35 mW at 2.5 V/100 kSPS, 4 mW at 5 V/100 kSPS, and
  1.4 µW at 2.5 V/100 SPS
Standby current: 1 nA
10-lead MSOP (MSOP-8 size) and
  3 mm × 3 mm LFCSP (SOT-23 size)
Pin-for-pin compatible with AD7685, AD7686, and AD7688

APPLICATIONS

Battery-powered equipment
Data acquisitions
Instrumentation
Medical instruments
Process controls

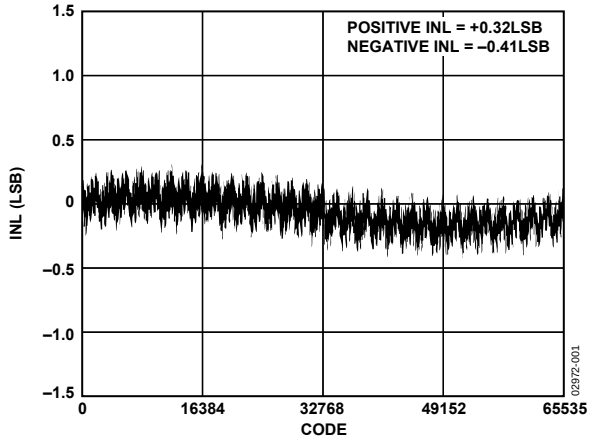

Figure 1. Integral Nonlinearity vs. Code

TYPICAL APPLICATION CIRCUIT

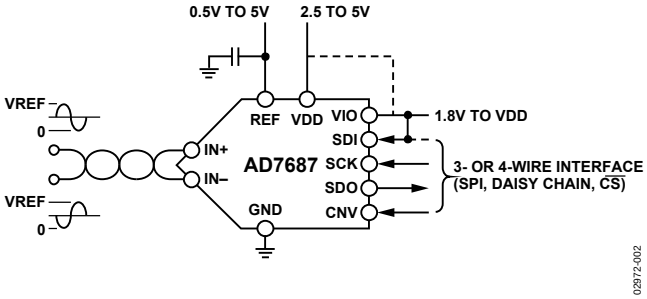

Figure 2.

Table 1. MSOP, LFCSP/SOT-23 16-Bit PulSAR™ ADC

Type	100 kSPS	250 kSPS	500 kSPS
True Differential	AD7684	AD7687	AD7688
Pseudo Differential/Unipolar	AD7683	AD7685 AD7694	AD7686
Unipolar	AD7680		

GENERAL DESCRIPTION

The AD7687[1] is a 16-bit, charge redistribution, successive approximation, analog-to-digital converter (ADC) that operates from a single power supply, VDD, between 2.3 V to 5.5 V. It contains a low power, high speed, 16-bit sampling ADC with no missing codes, an internal conversion clock, and a versatile serial interface port. The part also contains a low noise, wide bandwidth, short aperture delay track-and-hold circuit. On the CNV rising edge, it samples the voltage difference between IN+ and IN− pins. The voltages on these pins usually swing in opposite phase between 0 V to REF. The reference voltage, REF, is applied externally and can be set up to the supply voltage.

Its power scales linearly with throughput.

The SPI-compatible serial interface also features the ability, using the SDI input, to daisy-chain several ADCs on a single, 3-wire bus and provides an optional BUSY indicator. It is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic, using the separate supply VIO.

The AD7687 is housed in a 10-lead MSOP or a 10-lead LFCSP with operation specified from −40°C to +85°C.

[1] Protected by U.S. Patent 6,703,961.

Rev. D **Document Feedback**
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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Typical Application Circuit ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
Timing Specifications ... 5
Absolute Maximum Ratings ... 7
Thermal Resistance ... 7
ESD Caution ... 7
Pin Configurations and Function Descriptions ... 8
Terminology ... 9
Typical Performance Characteristics ... 10
Circuit Information ... 13
Converter Operation ... 13
Typical Connection Diagram ... 14
Analog Input ... 15
Driver Amplifier Choice ... 16
Single-to-Differential Driver ... 16
Voltage Reference Input ... 16
Power Supply ... 16
Supplying the ADC from the Reference ... 17
Digital Interface ... 17
$\overline{CS}$ Mode 3-Wire, No BUSY Indicator ... 18
$\overline{CS}$ Mode 3-Wire with BUSY Indicator ... 19
$\overline{CS}$ Mode 4-Wire, No BUSY Indicator ... 20
$\overline{CS}$ Mode 4-Wire with BUSY Indicator ... 21
Chain Mode, No BUSY Indicator ... 22
Chain Mode with BUSY Indicator ... 23
Application Hints ... 24
Layout ... 24
Evaluating the Performance of the AD7687 ... 24
Outline Dimensions ... 25
Ordering Guide ... 26

REVISION HISTORY

4/15—Rev. C to Rev. D

Added Patent Note, Note 1 ... 1
Changes to SNR Degradation Equation, Driver Amplifier Choice Section ... 16
Changes to Ordering Guide ... 26

7/14—Rev. B to Rev. C

Deleted QFN ... Throughout
Changed Application Diagram Section to Typical Application Circuit Section ... 1
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Added Note 1 ... 1
Changes to Figure 27 ... 14
Changes to Evaluating the Performance of the AD7687 Section ... 24
Updated Outline Dimensions ... 25
Changes to Ordering Guide ... 26

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Changes to Table 7 ... 7
Changes to Ordering Guide ... 26

2/11—Rev. 0 to Rev. A

Deleted QFN in Development Note ... Throughout
Changes to Table 6 ... 7
Added Thermal Resistance Section and Table 7 ... 7
Changes to Figure 6 and Table 8 ... 8
Updated Outline Dimensions ... 25
Changes to Ordering Guide ... 26

4/05—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.3 V to 5.5 V, VIO = 2.3 V to VDD, V_{REF} = VDD, T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	IN+ − IN−	$-V_{REF}$		$+V_{REF}$	V
Absolute Input Voltage	IN+, IN−	−0.1		V_{REF} + 0.1	V
Common-Mode Input Range	IN+, IN−	0	$V_{REF}/2$	$V_{REF}/2$ + 0.1	V
Analog Input CMRR	f_{IN} = 250 kHz		65		dB
Leakage Current at 25°C	Acquisition phase		1		nA
Input Impedance		See the Analog Input section			
ACCURACY					
No Missing Codes		16			Bits
Differential Linearity Error		−1	±0.4	+1	LSB[1]
Integral Linearity Error		−1.5	±0.4	+1.5	LSB
Transition Noise	REF = VDD = 5 V		0.35		LSB
Gain Error[2], T_{MIN} to T_{MAX}			±2	±6	LSB
Gain Error Temperature Drift			±0.3		ppm/°C
Offset Error[2], T_{MIN} to T_{MAX}	VDD = 4.5 V to 5.5 V		±0.1	±1.6	mV
	VDD = 2.3 V to 4.5 V		±0.7	±3.5	mV
Offset Temperature Drift			±0.3		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±0.05		LSB
THROUGHPUT					
Conversion Rate	VDD = 4.5 V to 5.5 V	0		250	kSPS
	VDD = 2.3 V to 4.5 V	0		200	kSPS
Transient Response	Full-scale step			1.8	µs
AC ACCURACY					
Dynamic Range	V_{REF} = 5 V	95.8	96.5		dB[3]
Signal-to-Noise	f_{IN} = 20 kHz, V_{REF} = 5 V	94	95.5		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V	92	92.5		dB
Spurious-Free Dynamic Range	f_{IN} = 20 kHz		−118		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		−118		dB
Signal-to-(Noise + Distortion)	f_{IN} = 20 kHz, V_{REF} = 5 V	94	95.5		dB
	f_{IN} = 20 kHz, V_{REF} = 5 V, −60 dB input		36.5		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V	92	92.5		dB
Intermodulation Distortion[4]			115		dB

[1] LSB means least significant bit. With the ±5 V input range, one LSB is 152.6 µV.
[2] See the Terminology section. These specifications do include full temperature range variation but do not include the error contribution from the external reference.
[3] All specifications in dB are referred to a full-scale input FSR. Tested with an input signal at 0.5 dB below full-scale, unless otherwise specified.
[4] f_{IN1} = 21.4 kHz, f_{IN2} = 18.9 kHz, each tone at −7 dB below full-scale.

VDD = 2.3 V to 5.5 V, VIO = 2.3 V to VDD, V_{REF} = VDD, T_A = −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		0.5		VDD + 0.3	V
Load Current	250 kSPS, REF = 5 V		50		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			2		MHz
Aperture Delay	VDD = 5 V		2.5		ns
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.3 × VIO	V
V_{IH}		0.7 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format		Serial 16-bits twos complement			
Pipeline Delay		Conversion results available immediately after completed conversion			
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD	Specified performance	2.3		5.5	V
VIO	Specified performance	2.3		VDD + 0.3	V
VIO Range		1.8		VDD + 0.3	V
Standby Current[1, 2]	VDD and VIO = 5 V, 25°C		1	50	nA
Power Dissipation	VDD = 2.5 V, 100 SPS throughput		1.4		µW
	VDD = 2.5 V, 100 kSPS throughput		1.35		mW
	VDD = 2.5 V, 200 kSPS throughput		2.7		mW
	VDD = 5 V, 100 kSPS throughput		4	5.5	mW
	VDD = 5 V, 250 kSPS throughput			12.5	mW
TEMPERATURE RANGE[3]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] With all digital inputs forced to VIO or GND as required.
[2] During acquisition phase.
[3] Contact sales for extended temperature range.

TIMING SPECIFICATIONS

−40°C to +85°C, VDD = 4.5 V to 5.5 V, VIO = 2.3 V to 5.5 V or VDD + 0.3 V, whichever is the lowest, unless otherwise stated.

See Figure 3 and Figure 4 for load conditions.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	0.5		2.2	µs
Acquisition Time	t_{ACQ}	1.8			µs
Time Between Conversions	t_{CYC}	4			µs
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}	15			ns
SCK Period (Chain Mode)	t_{SCK}				
VIO Above 4.5 V		17			ns
VIO Above 3 V		18			ns
VIO Above 2.7 V		19			ns
VIO Above 2.3 V		20			ns
SCK Low Time	t_{SCKL}	7			ns
SCK High Time	t_{SCKH}	7			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 4.5 V				14	ns
VIO Above 3 V				15	ns
VIO Above 2.7 V				16	ns
VIO Above 2.3 V				17	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO Above 4.5 V				15	ns
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				22	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			25	ns
SDI Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{SSDICNV}$	15			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	3			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	4			ns
SDI High to SDO High (Chain Mode with BUSY indicator)	$t_{DSDOSDI}$				
VIO Above 4.5 V				15	ns
VIO Above 2.3 V				26	ns

−40°C to +85°C, VDD = 2.3 V to 4.5 V, VIO = 2.3 V to 4.5 V or VDD + 0.3 V, whichever is the lowest, unless otherwise stated.

See Figure 3 and Figure 4 for load conditions.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	0.7		3.2	µs
Acquisition Time	t_{ACQ}	1.8			µs
Time Between Conversions	t_{CYC}	5			µs
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}	25			ns
SCK Period (Chain Mode)	t_{SCK}				
VIO Above 3 V		29			ns
VIO Above 2.7 V		35			ns
VIO Above 2.3 V		40			ns
SCK Low Time	t_{SCKL}	12			ns
SCK High Time	t_{SCKH}	12			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 3 V				24	ns
VIO Above 2.7 V				30	ns
VIO Above 2.3 V				35	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				22	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			25	ns
SDI Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{SSDICNV}$	30			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	8			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	5			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	4			ns
SDI High to SDO High (Chain Mode with BUSY indicator)	$t_{DSDOSDI}$			36	ns

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Inputs	
IN+[1], IN−[1]	GND − 0.3 V to VDD + 0.3 V or ±130 mA
REF	GND − 0.3 V to VDD + 0.3 V
Supply Voltages	
VDD, VIO to GND	−0.3 V to +7 V
VDD to VIO	±7 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature Range	JEDEC J-STD-20

[1] See the Analog Input section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
10-Lead LFCSP	84	2.96	°C/W
10-Lead MSOP	200	44	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

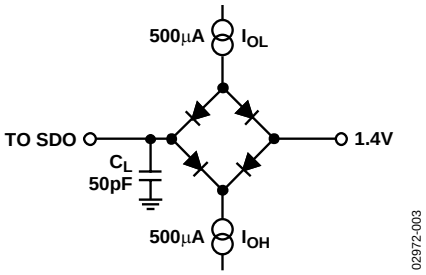

Figure 3. Load Circuit for Digital Interface Timing

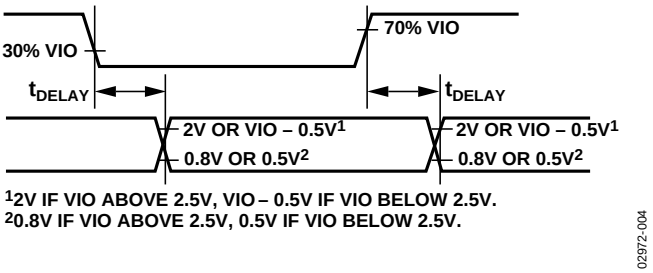

Figure 4. Voltage Levels for Timing

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

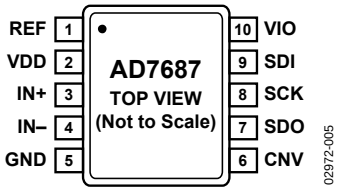

Figure 5. 10-Lead MSOP Pin Configuration

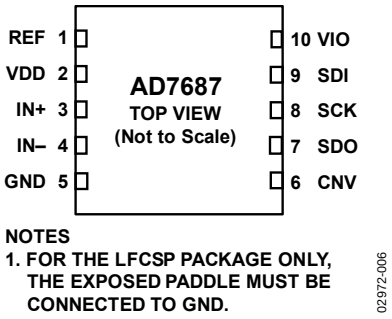

Figure 6. 10-Lead LFCSP Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Function
1	REF	AI	Reference Input Voltage. The REF range is from 0.5 V to VDD. It is referred to the GND pin. This pin should be decoupled closely to the pin with a 10 µF capacitor.
2	VDD	P	Power Supply.
3	IN+	AI	Differential Positive Analog Input.
4	IN–	AI	Differential Negative Analog Input.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode, chain or $\overline{CS}$. In $\overline{CS}$ mode, it enables the SDO pin when low. In chain mode, the data should be read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low, and if SDI or CNV is low when the conversion is complete, the BUSY indicator feature is enabled.
10	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
	EPAD	N/A	For the LFCSP package only, the exposed paddle must be connected to GND.

[1]AI = Analog Input, DI = Digital Input, DO = Digital Output, P = Power, and N/A = not applicable.

TERMINOLOGY

Integral Nonlinearity Error (INL)
It refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (Figure 26).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error
It is the difference between the ideal midscale voltage, that is, 0 V, from the actual voltage producing the midscale output code, that is, 0 LSB.

Gain Error
The first transition (from 100 . . . 00 to 100 . . . 01) should occur at a level ½ LSB above nominal negative full scale (−4.999924 V for the ±5 V range). The last transition (from 011…10 to 011…11) should occur for an analog voltage 1½ LSB below the nominal full scale (+4.999771 V for the ±5 V range.) The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N+D) by the following formula

$$ENOB = (S/[N + D]_{dB} - 1.76)/6.02$$

and is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

Dynamic Range
It is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in dB.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in dB.

Signal-to-(Noise + Distortion) Ratio (S/[N+D])
S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in dB.

Aperture Delay
Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
It is the time required for the ADC to accurately acquire its input after a full-scale step function was applied.

TYPICAL PERFORMANCE CHARACTERISTICS

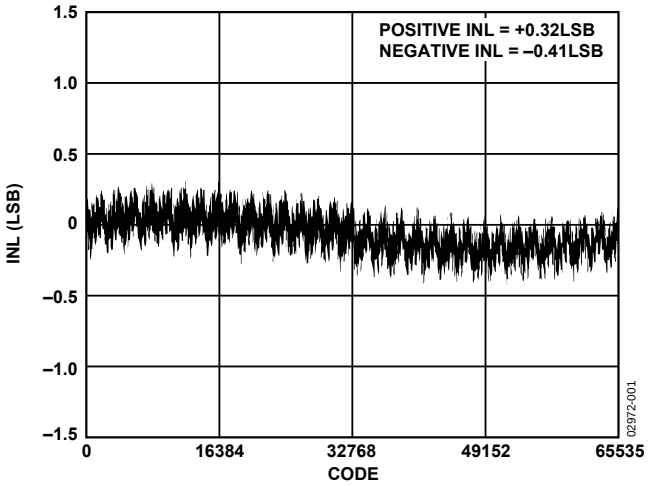

Figure 7. Integral Nonlinearity vs. Code

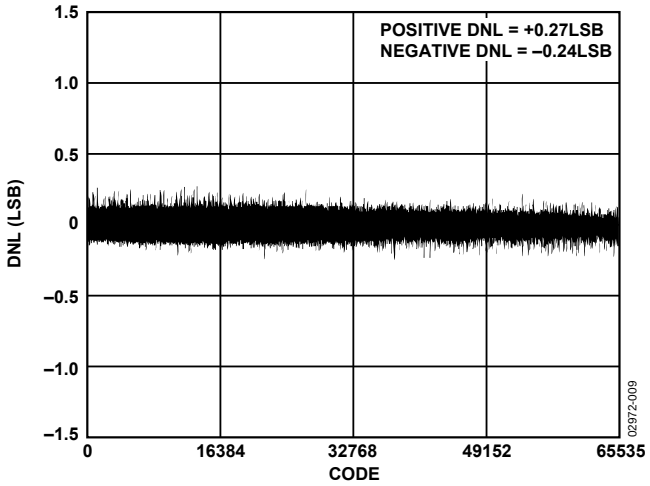

Figure 10. Differential Nonlinearity vs. Code

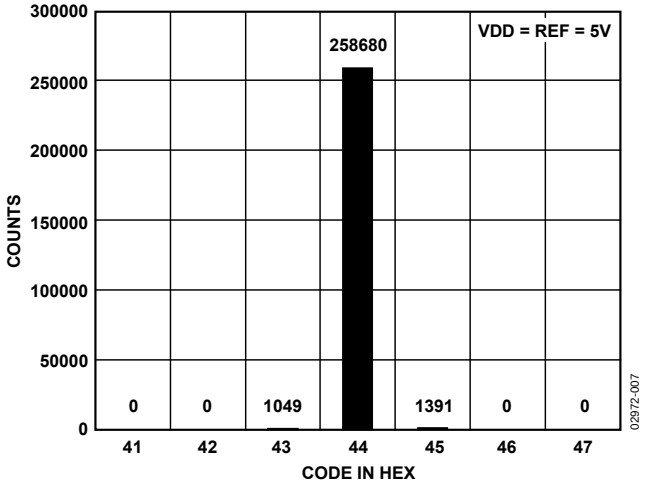

Figure 8. Histogram of a DC Input at the Code Center

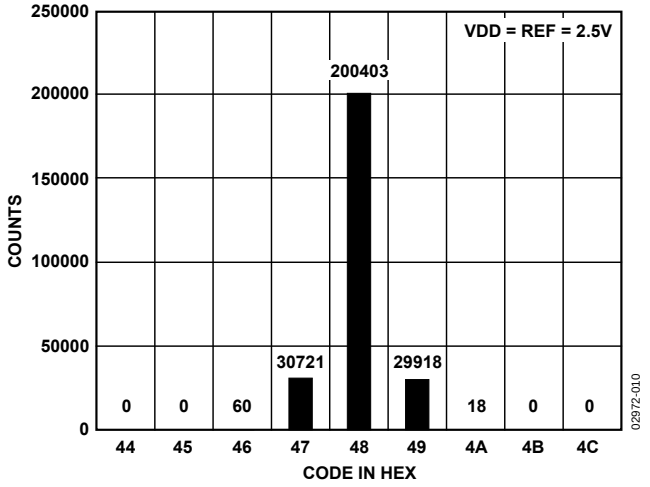

Figure 11. Histogram of a DC Input at the Code Center

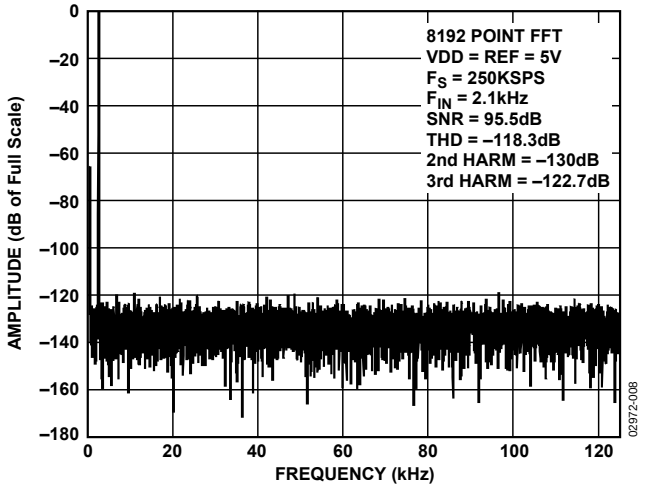

Figure 9. FFT Plot

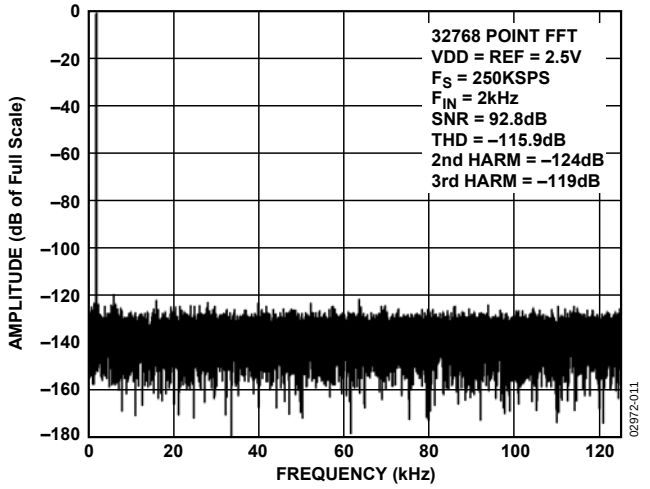

Figure 12. FFT Plot

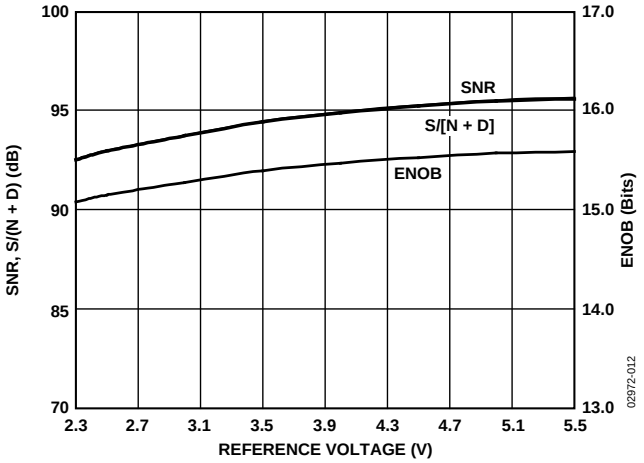

Figure 13. SNR, S/(N + D), and ENOB vs. Reference Voltage

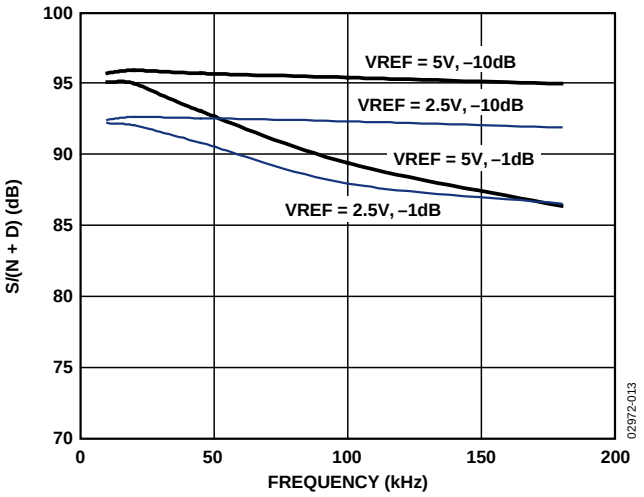

Figure 14. S/(N + D) vs. Frequency

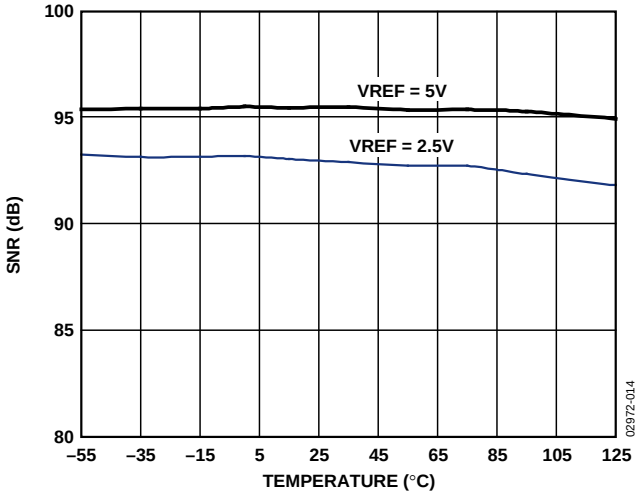

Figure 15. SNR vs. Temperature

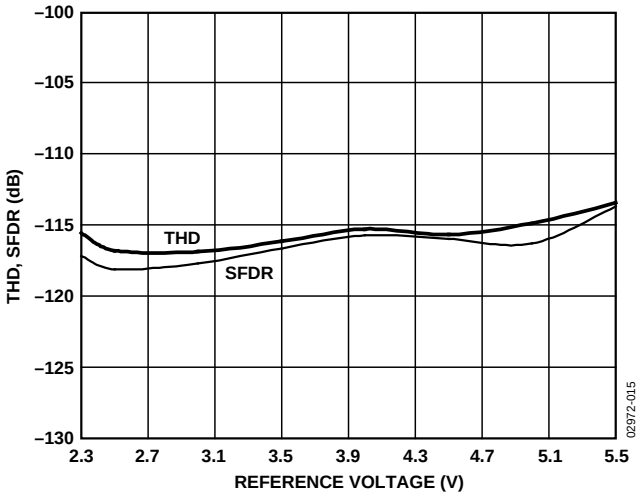

Figure 16. THD, SFDR vs. Reference Voltage

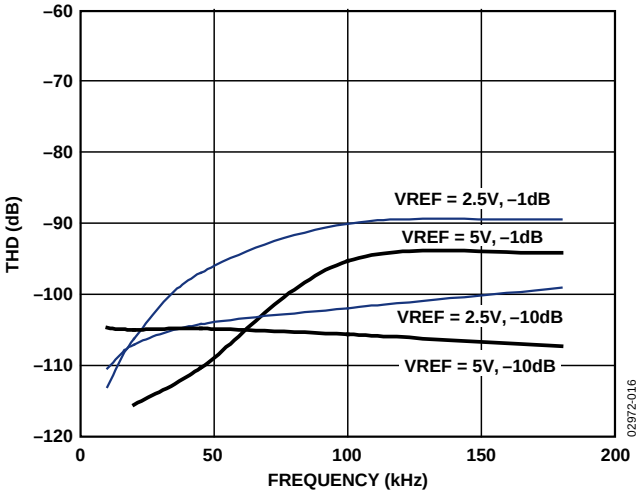

Figure 17. THD vs. Frequency

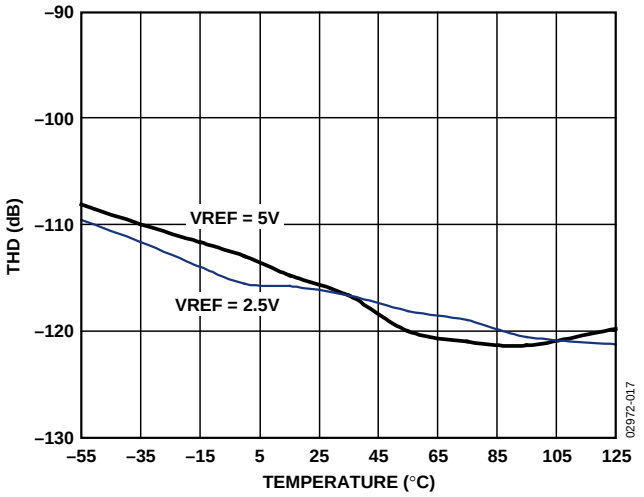

Figure 18. THD vs. Temperature

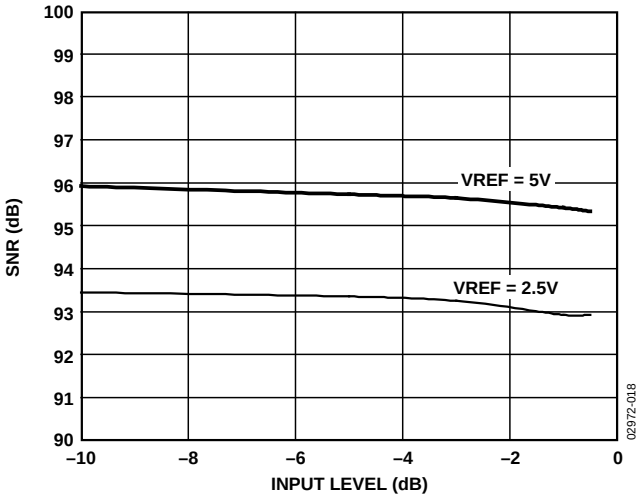

Figure 19. SNR vs. Input Level

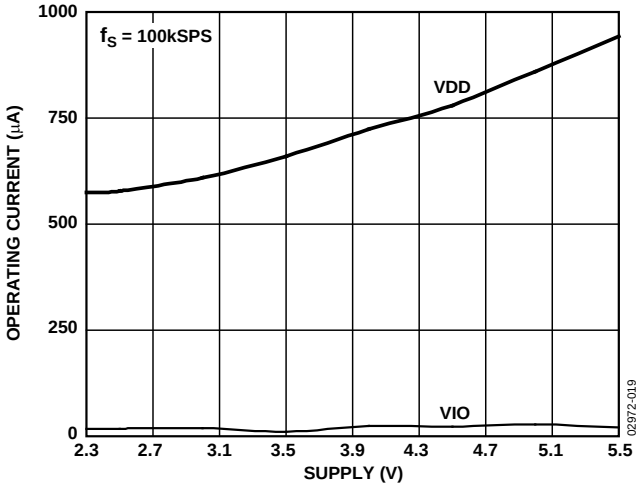

Figure 20. Operating Currents vs. Supply

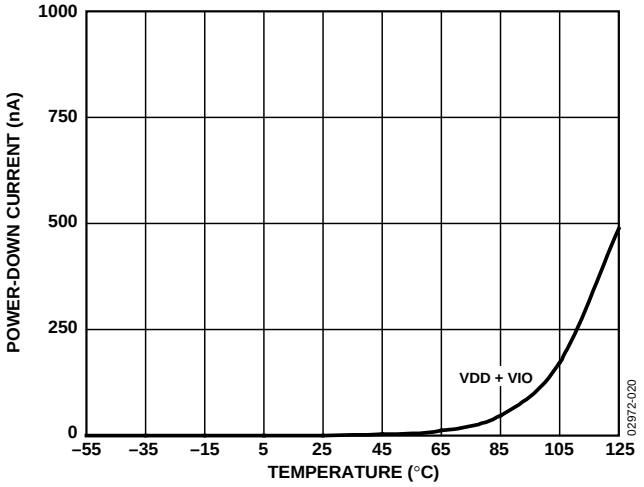

Figure 21. Power-Down Currents vs. Temperature

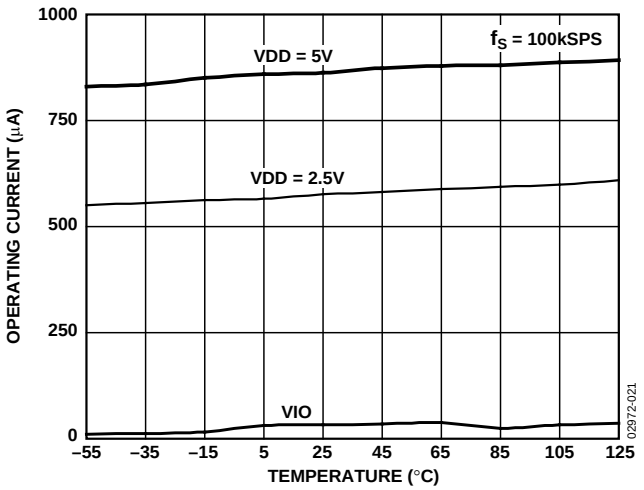

Figure 22. Operating Currents vs. Temperature

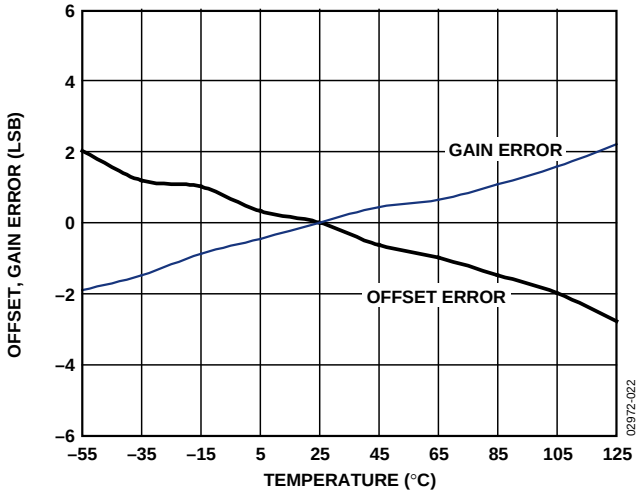

Figure 23. Offset and Gain Error vs. Temperature

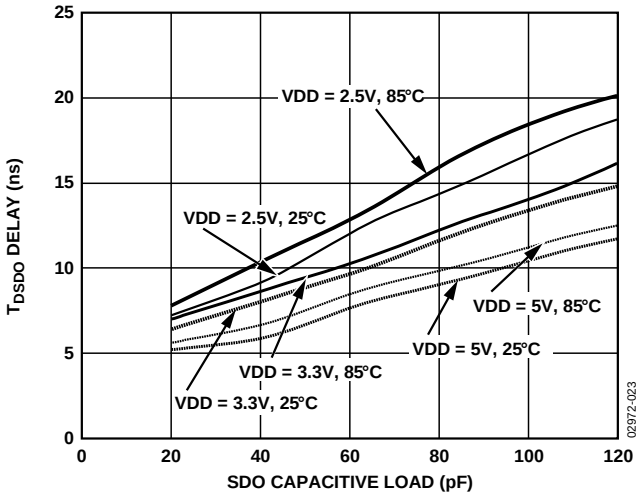

Figure 24. t_{DSDO} Delay vs. Capacitance Load and Supply

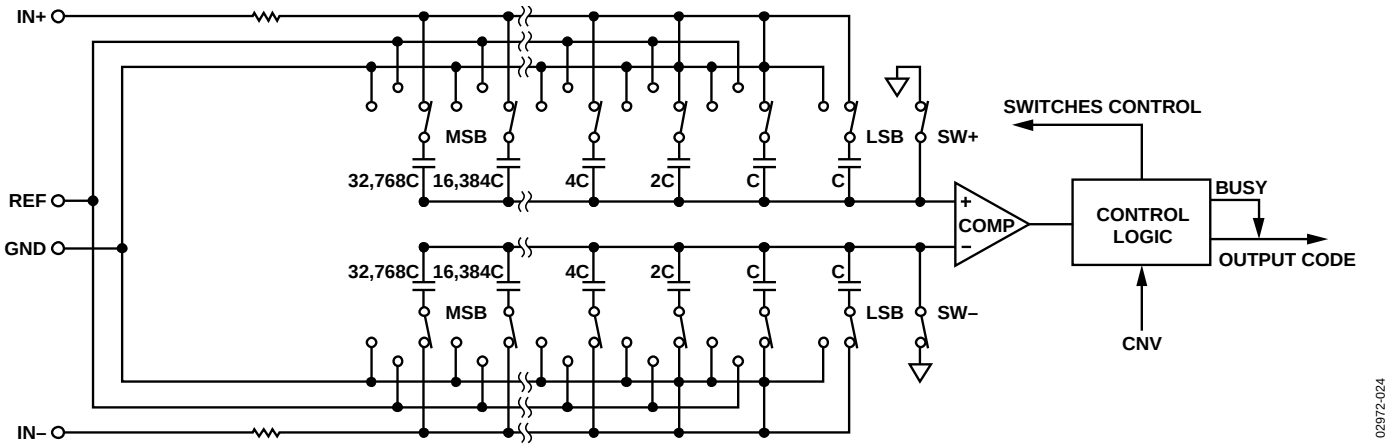

Figure 25. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7687 is a fast, low power, single-supply, precise 16-bit ADC using a successive approximation architecture.

The AD7687 is capable of converting 250,000 samples per second (250 kSPS) and powers down between conversions. When operating at 100 SPS, for example, it typically consumes 1.35 µW, which is ideal for battery-powered applications.

The AD7687 provides the user with an on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple multiplexed channel applications.

The AD7687 is specified from 2.3 V to 5.5 V and can be interfaced to any of the 1.8 V to 5 V digital logic family. It is housed in a 10-lead MSOP or a tiny 10-lead LFCSP that combines space savings and allows flexible configurations.

It is pin-for-pin-compatible with the AD7685, AD7686, and AD7688.

CONVERTER OPERATION

The AD7687 is a successive approximation ADC based on a charge redistribution DAC. Figure 25 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs IN+ and IN− captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ . . . $V_{REF}/65536$). The control logic toggles these switches, starting with the MSB, in order to bring the comparator back into a balanced condition. After the completion of this process, the part returns to the acquisition phase and the control logic generates the ADC output code and a BUSY signal indicator.

Because the AD7687 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

Transfer Functions

The ideal transfer characteristic for the AD7687 is shown in Figure 26 and Table 9.

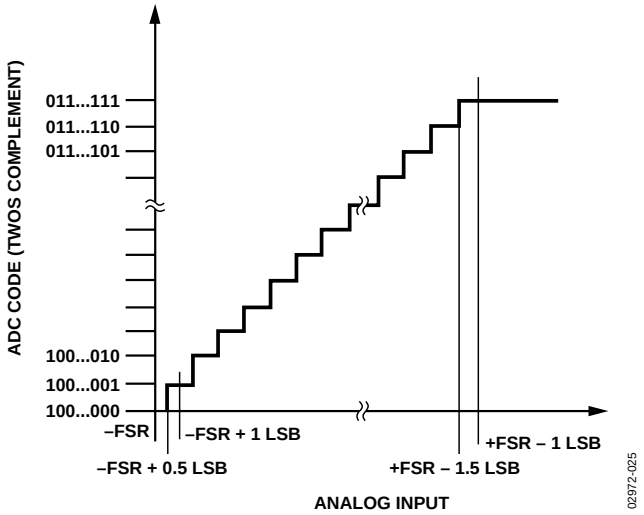

Figure 26. ADC Ideal Transfer Function

Table 9. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5 V	Digital Output Code Hexa
FSR – 1 LSB	+4.999847 V	7FFF[1]
Midscale + 1 LSB	+152.6 µV	0001
Midscale	0 V	0000
Midscale – 1 LSB	–152.6 µV	FFFF
–FSR + 1 LSB	–4.999847 V	8001
–FSR	–5 V	8000[2]

[1] This is also the code for an overranged analog input ($V_{IN+} - V_{IN-}$ above $V_{REF} - V_{GND}$).

[2] This is also the code for an underranged analog input ($V_{IN+} - V_{IN-}$ below $-V_{REF} + V_{GND}$).

TYPICAL CONNECTION DIAGRAM

Figure 27 shows an example of the recommended connection diagram for the AD7687 when multiple supplies are available.

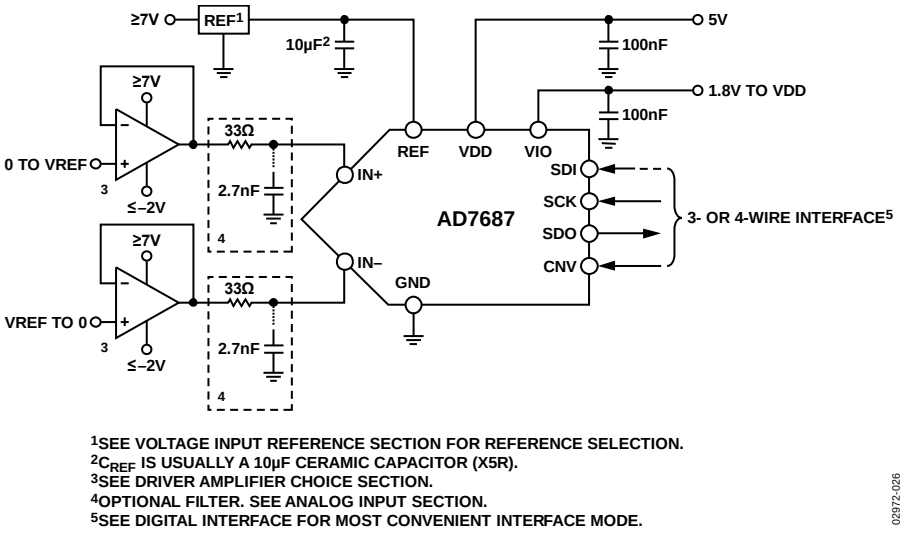

Figure 27. Typical Application Diagram with Multiple Supplies

ANALOG INPUT

Figure 28 shows an equivalent circuit of the input structure of the AD7687.

The two diodes, D1 and D2, provide ESD protection for the analog inputs IN+ and IN−. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V because this causes these diodes to begin to forward-bias and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions could eventually occur when the input buffer's (U1) supplies are different from VDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

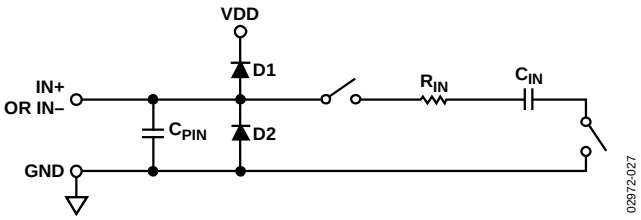

Figure 28. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected, as shown in Figure 29, which represents the typical CMRR over frequency.

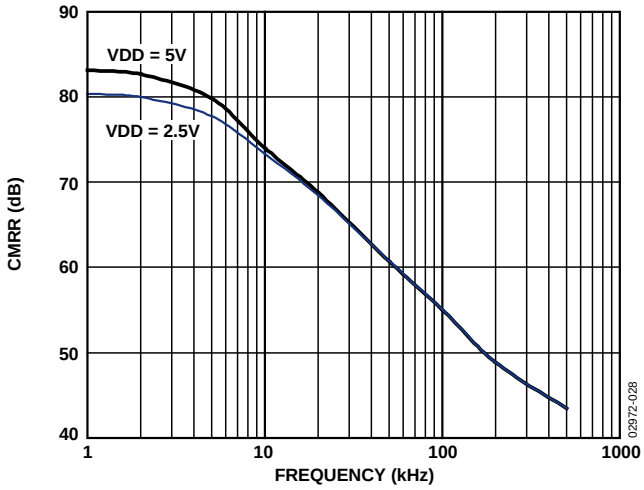

Figure 29. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog inputs (IN+ or IN−) can be modeled as a parallel combination of capacitor, C_{PIN}, and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 3 kΩ and is a lumped component made up of some serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor. During the conversion phase, where the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise.

When the source impedance of the driving circuit is low, the AD7687 can be driven directly. Large source impedances significantly affect the ac performance, especially total harmonic distortion (THD). The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency, as shown in Figure 30.

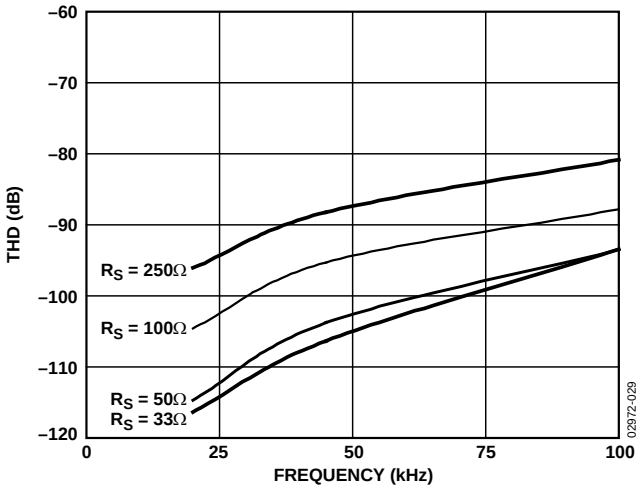

Figure 30. THD vs. Analog Input Frequency and Source Resistance

DRIVER AMPLIFIER CHOICE

Although the AD7687 is easy to drive, the driver amplifier needs to meet the following requirements:

- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7687. Note that the AD7687 has a noise much lower than most of the other 16-bit ADCs and, therefore, can be driven by a noisier op amp while preserving the same or better system performance. The noise coming from the driver is filtered by the AD7687 analog input circuit 1-pole, low-pass filter made by R_{IN} and C_{IN} or by the external filter, if one is used. Because the typical noise of the AD7687 is 53 µV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20\log\left(\frac{53}{\sqrt{53^2 + \frac{\pi}{2} f_{-3dB}(2Ne_N)^2}}\right)$$

  where:

  f_{-3dB} is the input bandwidth in MHz of the AD7687 (2 MHz) or the cutoff frequency of the input filter, if one is used.

  N is the noise gain of the amplifier (for example, +1 in buffer configuration).

  e_N is the equivalent input noise voltage of the op amp, in nV/√Hz.

- For ac applications, the driver should have a THD performance commensurate with the AD7687. Figure 17 shows the THD vs. frequency that the driver should exceed.
- For multichannel multiplexed applications, the driver amplifier and the AD7687 analog input circuit must settle a full-scale step onto the capacitor array at a 16-bit level (0.0015%, 15 ppm). In the amplifier's data sheet, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection.

Table 10. Recommended Driver Amplifiers.

Amplifier	Typical Application
AD8021	Very low noise and high frequency
AD8022	Low noise and high frequency
OP184	Low power, low noise, and low frequency
AD8605, AD8615	5 V single-supply, low power
AD8519	Small, low power and low frequency
AD8031	High frequency and low power

SINGLE-TO-DIFFERENTIAL DRIVER

For applications using a single-ended analog signal, either bipolar or unipolar, a single-ended-to-differential driver allows for a differential input into the part (see Figure 31 for the schematic). When provided a single-ended input signal, this configuration produces a differential $\pm V_{REF}$ with midscale at $V_{REF}/2$.

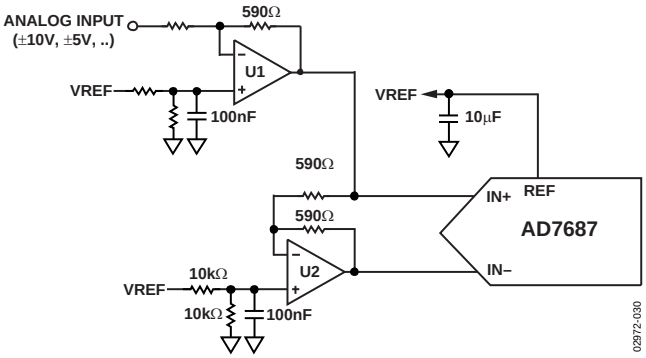

Figure 31. Single-Ended-to-Differential Driver Circuit

VOLTAGE REFERENCE INPUT

The AD7687 voltage reference input, REF, has a dynamic input impedance and should therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins, as explained in the Layout section.

When REF is driven by a very low impedance source, for example, a reference buffer using the AD8031 or the AD8605, a 10 µF (X5R, 0805 size) ceramic chip capacitor is appropriate for optimum performance.

If an unbuffered reference voltage is used, the decoupling value depends on the reference used. For instance, a 22 µF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance using a low temperature drift ADR435 reference.

If desired, smaller reference decoupling capacitor values down to 2.2 µF can be used with a minimal impact on performance, especially DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

POWER SUPPLY

The AD7687 is specified over a wide operating range of 2.3 V to 5.5 V. Unlike other low voltage converters, it has a low enough noise to design a 16-bit resolution system with low supply and respectable performance. It uses two power supply pins: a core supply VDD and a digital input/output interface supply VIO. VIO allows direct interface with any logic between 1.8 V and VDD. To reduce the supplies needed, the VIO and VDD can be tied together. The AD7687 is independent of power supply sequencing between VIO and VDD. Additionally, it is very

insensitive to power supply variations over a wide frequency range, as shown in Figure 32, which represents PSRR over frequency.

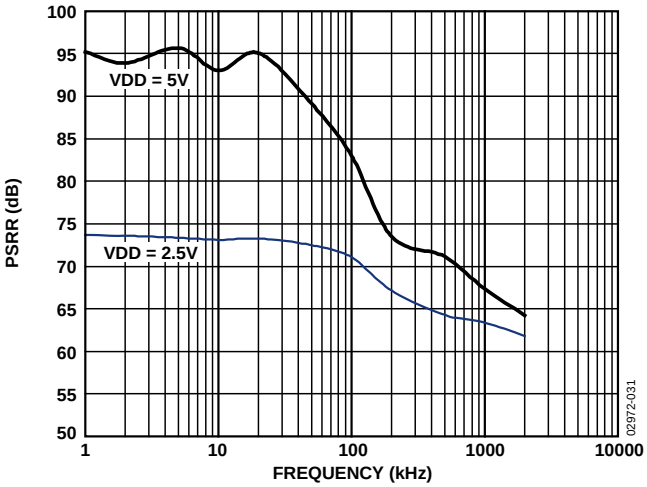

Figure 32. PSRR vs. Frequency

The AD7687 powers down automatically at the end of each conversion phase and, therefore, the power scales linearly with the sampling rate, as shown in Figure 33. This makes the part ideal for low sampling rate (even a few Hz) and low battery-powered applications.

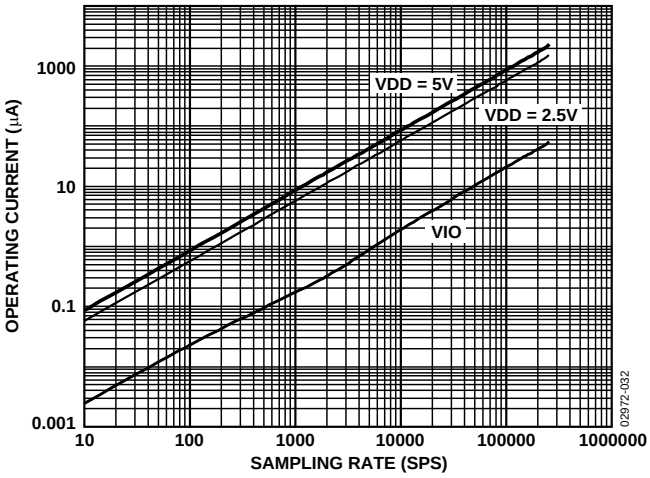

Figure 33. Operating Currents vs. Sampling Rate

SUPPLYING THE ADC FROM THE REFERENCE

For simplified applications, the AD7687, with its low operating current, can be supplied directly using the reference circuit shown in Figure 34. The reference line can be driven by either

- The system power supply directly.
- A reference voltage with enough current output capability, such as the ADR435.
- A reference buffer, such as the AD8031, which can also filter the system power supply, as shown in Figure 34.

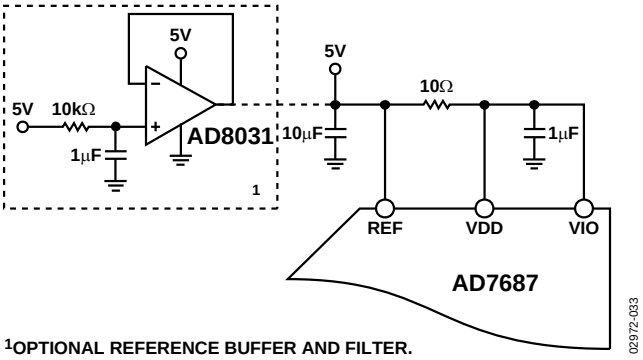

Figure 34. Example of Application Circuit

DIGITAL INTERFACE

Though the AD7687 has a reduced number of pins, it offers flexibility in its serial interface modes.

The AD7687, when in $\overline{CS}$ mode, is compatible with SPI, QSPI, digital hosts, and DSPs, for example, Blackfin® ADSP-BF53x or ADSP-219x. This interface can use either 3-wire or 4-wire. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). This is useful in low jitter sampling or simultaneous sampling applications.

The AD7687, when in chain mode, provides a daisy chain feature using the SDI input for cascading multiple ADCs on a single data line similar to a shift register.

The mode in which the part operates depends on the SDI level when the CNV rising edge occurs. The $\overline{CS}$ mode is selected if SDI is high and the chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, the chain mode is always selected.

In either mode, the AD7687 offers the flexibility to optionally force a start bit in front of the data bits. This start bit can be used as a BUSY signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a BUSY indicator, the user must time out the maximum conversion time prior to readback.

The BUSY indicator feature is enabled as

- In the $\overline{CS}$ mode, if CNV or SDI is low when the ADC conversion ends (Figure 38 and Figure 42).
- In the chain mode, if SCK is high during the CNV rising edge (Figure 46).

$\overline{CS}$ MODE 3-WIRE, NO BUSY INDICATOR

This mode is usually used when a single AD7687 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 35 and the corresponding timing is given in Figure 36.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. Once a conversion is initiated, it continues to completion irrespective of the state of CNV. For instance, it could be useful to bring CNV low to select other SPI devices, such as analog multiplexers, but CNV must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid the generation of the BUSY signal indicator. When the conversion is complete, the AD7687 enters the acquisition phase and powers down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate provided it has an acceptable hold time. After the 16th SCK falling edge or when CNV goes high, whichever is earlier, SDO returns to high impedance.

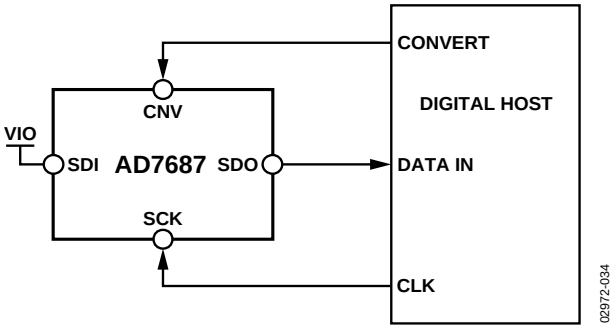

Figure 35. $\overline{CS}$ Mode 3-Wire, No BUSY Indicator Connection Diagram (SDI High)

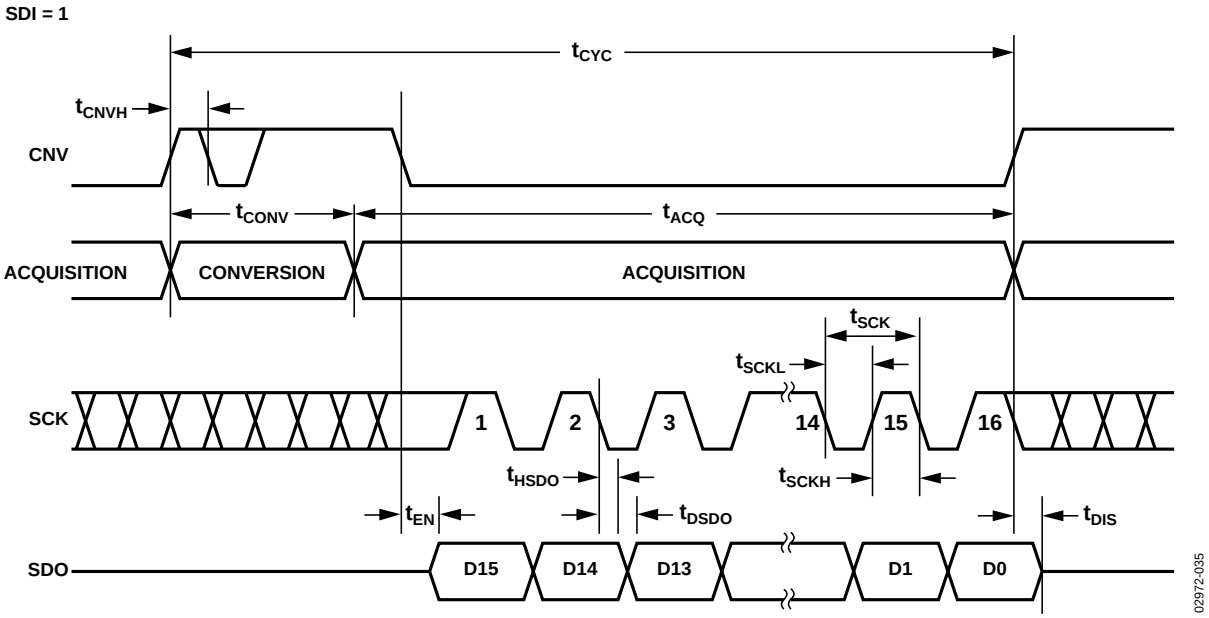

Figure 36. $\overline{CS}$ Mode 3-Wire, No BUSY Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE 3-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7687 is connected to an SPI-compatible digital host having an interrupt input.

The connection diagram is shown in Figure 37 and the corresponding timing is given in Figure 38.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion irrespective of the state of CNV. Prior to the minimum conversion time, CNV could be used to select other SPI devices, such as analog multiplexers, but CNV must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the BUSY signal indicator. When the conversion is complete, SDO goes from high impedance to low. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The AD7687 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate provided it has an acceptable hold time. After the optional 17th SCK falling edge, or when CNV goes high, whichever is earlier, SDO returns to high impedance.

If multiple AD7687s are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. Meanwhile, it is recommended to keep this contention as short as possible to limit extra power dissipation.

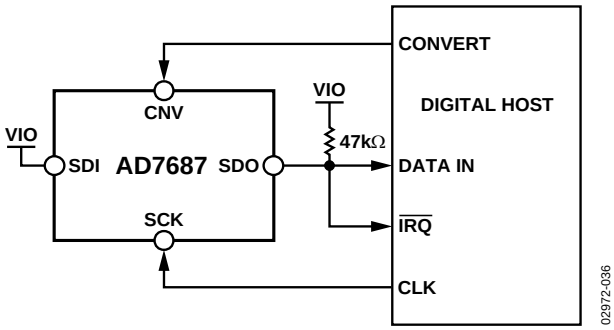

Figure 37. $\overline{CS}$ Mode 3-Wire with BUSY Indicator Connection Diagram (SDI High)

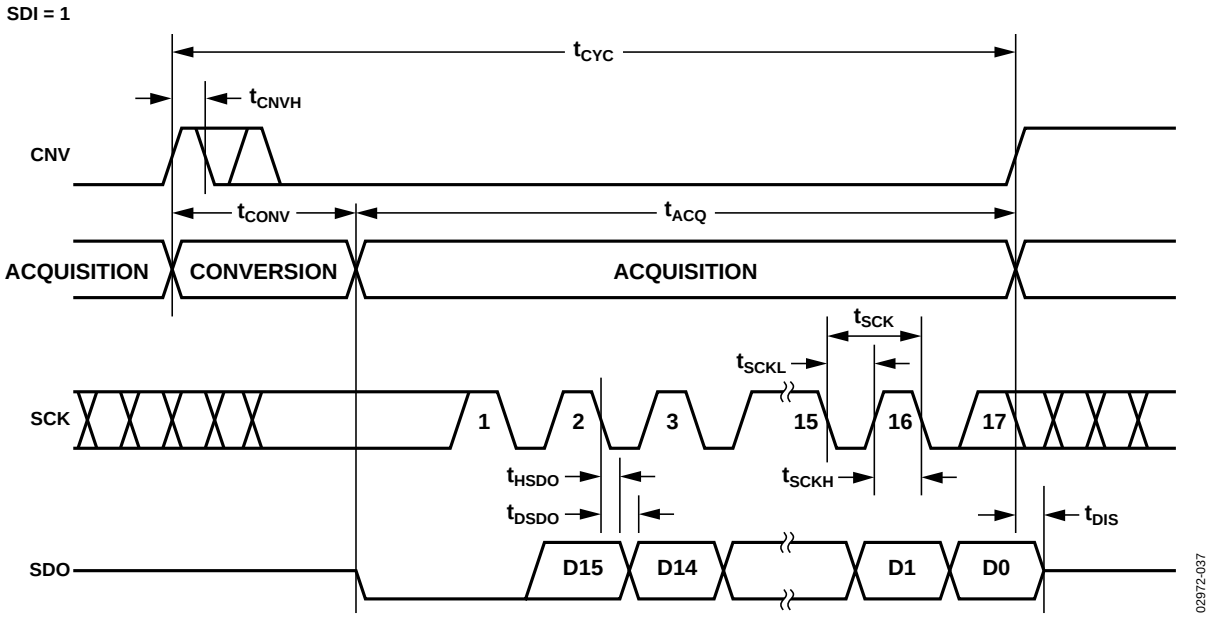

Figure 38. $\overline{CS}$ Mode 3-Wire with BUSY Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE 4-WIRE, NO BUSY INDICATOR

This mode is usually used when multiple AD7687s are connected to an SPI-compatible digital host.

A connection diagram example using two AD7687s is shown in Figure 39 and the corresponding timing is given in Figure 40.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI could be used to select other SPI devices, such as analog multiplexers, but SDI must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid the generation of the BUSY signal indicator. When the conversion is complete, the AD7687 enters the acquisition phase and powers down. Each ADC result can be read by bringing low its SDI input, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate provided it has an acceptable hold time. After the 16th SCK falling edge, or when SDI goes high, whichever is earlier, SDO returns to high impedance and another AD7687 can be read.

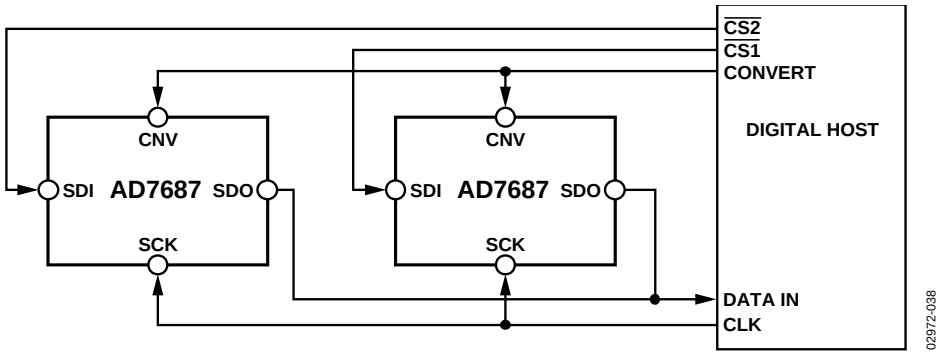

Figure 39. $\overline{CS}$ Mode 4-Wire, No BUSY Indicator Connection Diagram

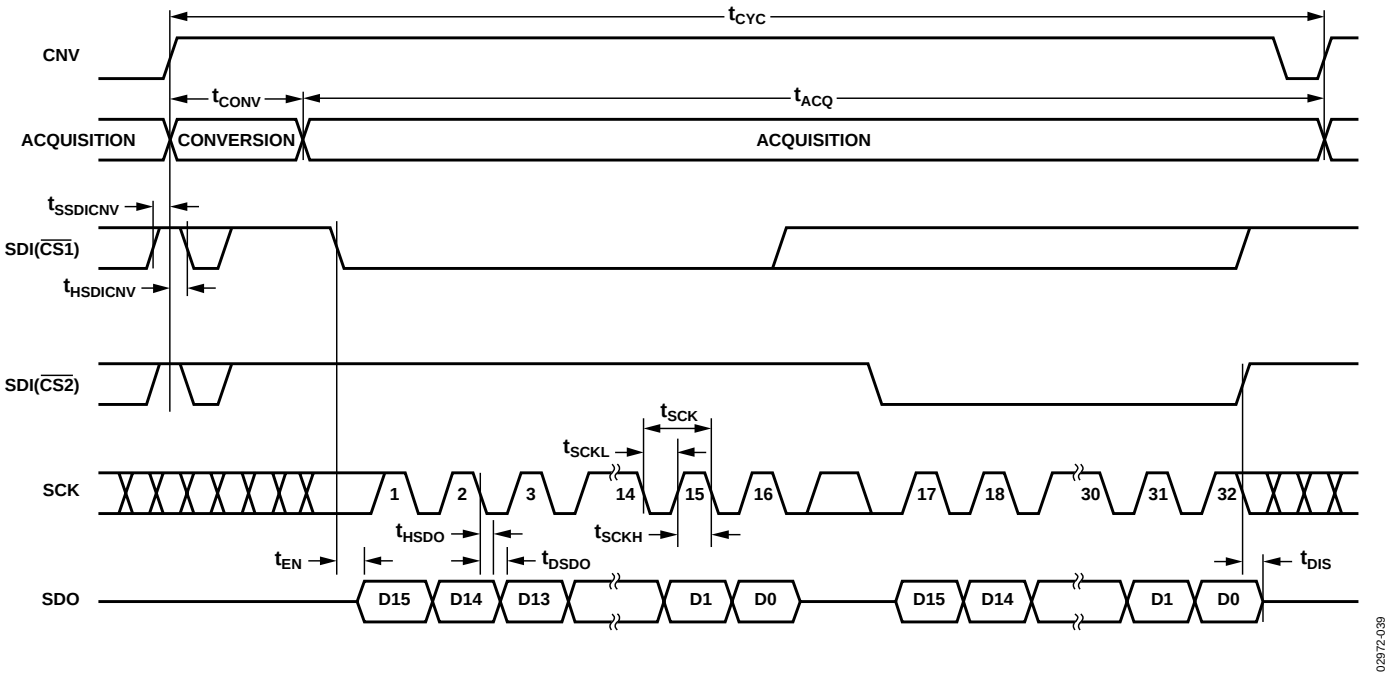

Figure 40. $\overline{CS}$ Mode 4-Wire, No BUSY Indicator Serial Interface Timing

$\overline{CS}$ MODE 4-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7687 is connected to an SPI-compatible digital host, which has an interrupt input, and it is desired to keep CNV, which is used to sample the analog input, independent of the signal used to select the data reading. This requirement is particularly important in applications where low jitter on CNV is desired.

The connection diagram is shown in Figure 41 and the corresponding timing is given in Figure 42.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI could be used to select other SPI devices, such as analog multiplexers, but SDI must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the BUSY signal indicator. When the conversion is complete, SDO goes from high impedance to low. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD7687 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate provided it has an acceptable hold time. After the optional 17th SCK falling edge, or SDI going high, whichever is earlier, the SDO returns to high impedance.

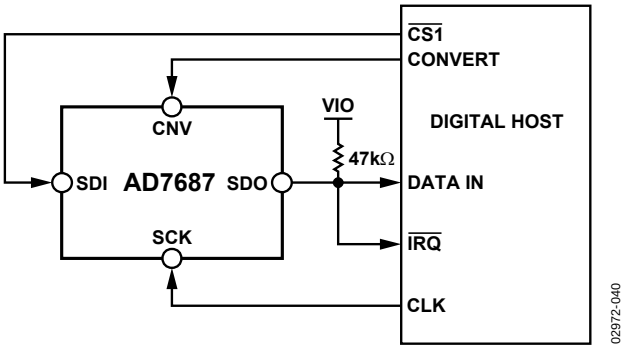

Figure 41. $\overline{CS}$ Mode 4-Wire with BUSY Indicator Connection Diagram

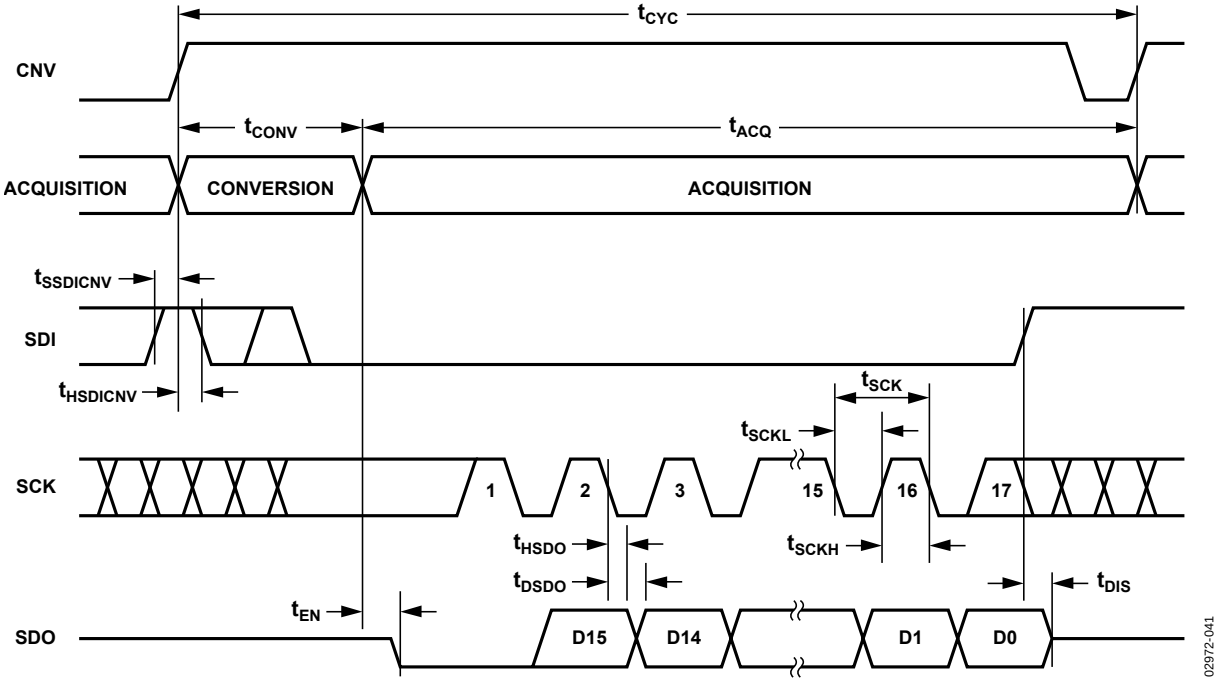

Figure 42. $\overline{CS}$ Mode 4-Wire with BUSY Indicator Serial Interface Timing

CHAIN MODE, NO BUSY INDICATOR

This mode can be used to daisy chain multiple AD7687s on a 3-wire serial interface. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using two AD7687s is shown in Figure 43 and the corresponding timing is given in Figure 44.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects the chain mode, and disables the BUSY indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO and the AD7687 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are then clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 16 × N clocks are required to readback the N ADCs. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate and, consequently more AD7687s in the chain, provided the digital host has an acceptable hold time. The maximum conversion rate may be reduced due to the total readback time. For instance, with a 3 ns digital host set-up time and 3 V interface, up to eight AD7687s running at a conversion rate of 220 kSPS can be daisy-chained on a 3-wire port.

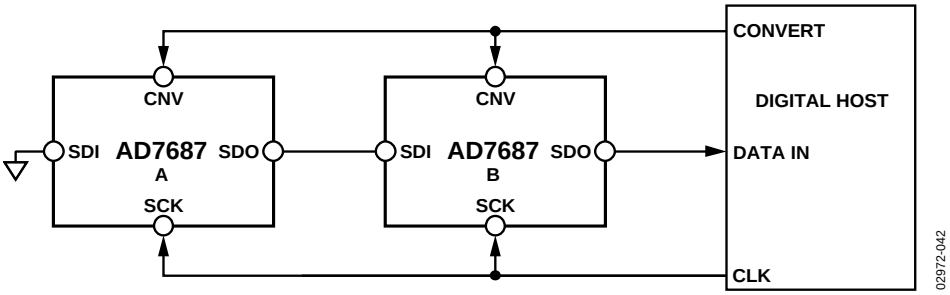

Figure 43. Chain Mode, No BUSY Indicator Connection Diagram

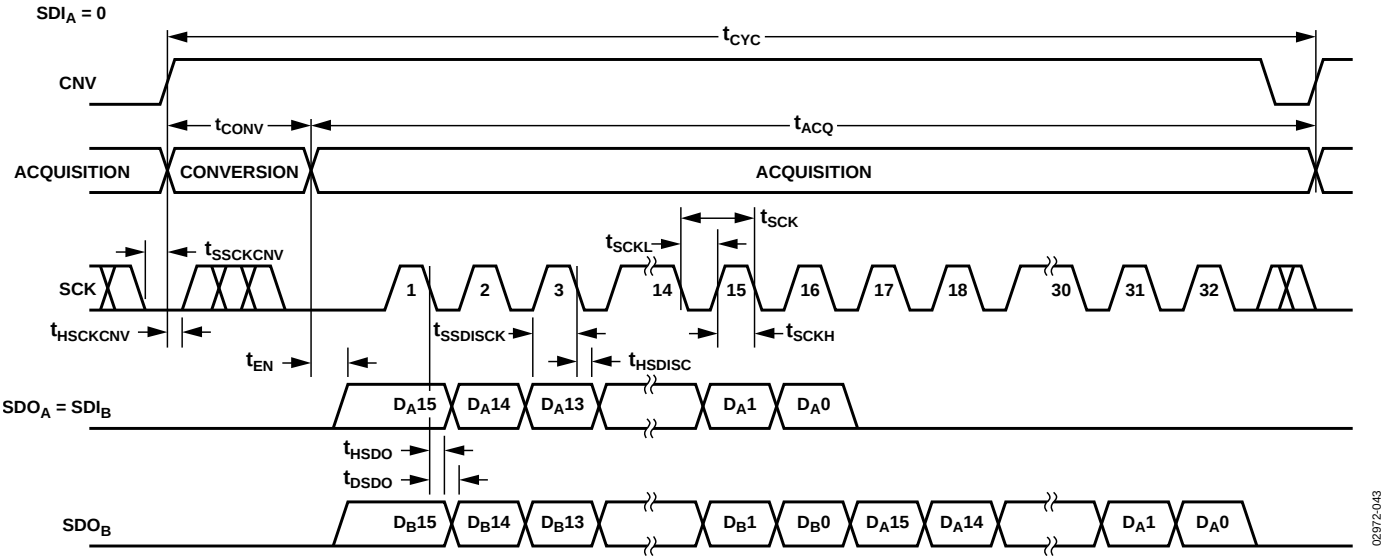

Figure 44. Chain Mode, No BUSY Indicator Serial Interface Timing

CHAIN MODE WITH BUSY INDICATOR

This mode can also be used to daisy-chain multiple AD7687s on a 3-wire serial interface while providing a BUSY indicator. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using three AD7687s is shown in Figure 45 and the corresponding timing is given in Figure 46.

When SDI and CNV are low, SDO is driven low. With SCK high, a rising edge on CNV initiates a conversion, selects the chain mode, and enables the BUSY indicator feature. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When all ADCs in the chain have completed their conversions, the near-end ADC (ADC C in Figure 45) SDO is driven high. This transition on SDO can be used as a BUSY indicator to trigger the data readback controlled by the digital host. The AD7687 then enters the acquisition phase and powers down. The data bits stored in the internal shift register are then clocked out, MSB first, by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 16 × N + 1 clocks are required to readback the N ADCs. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate and consequently more AD7687s in the chain, provided the digital host has an acceptable hold time. For instance, with a 3 ns digital host setup time and 3 V interface, up to eight AD7687s running at a conversion rate of 220 kSPS can be daisy-chained to a single 3-wire port.

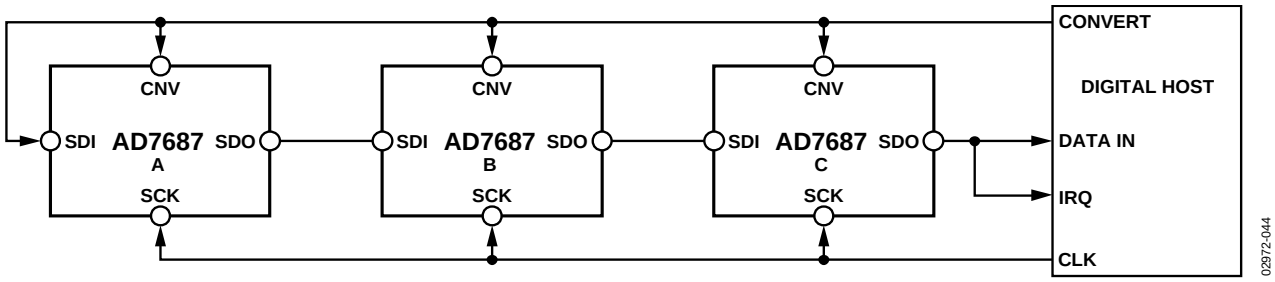

Figure 45. Chain Mode with BUSY Indicator Connection Diagram

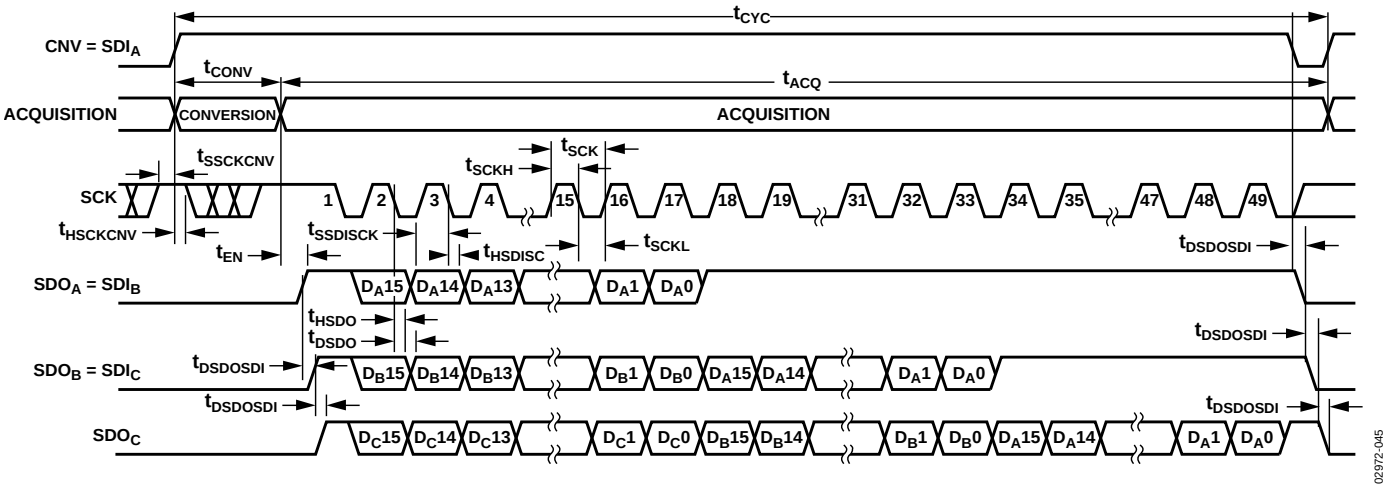

Figure 46. Chain Mode with BUSY Indicator Serial Interface Timing

APPLICATION HINTS

LAYOUT

The printed circuit board that houses the AD7687 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7687, with all its analog signals on the left side and all its digital signals on the right side, eases this task.

Avoid running digital lines under the device because these couple noise onto the die, unless a ground plane under the AD7687 is used as a shield. Fast switching signals, such as CNV or clocks, should never run near analog signal paths. Crossover of digital and analog signals should be avoided.

At least one ground plane should be used. It could be common or split between the digital and analog sections. In the latter case, the planes should be joined underneath the AD7687s.

The AD7687 voltage reference input REF has a dynamic input impedance and should be decoupled with minimal parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, and ideally right up against, the REF and GND pins and connecting it with wide, low impedance traces.

Finally, the power supplies VDD and VIO of the AD7687 should be decoupled with ceramic capacitors (typically 100 nF) placed close to the AD7687 and connected using short and wide traces to provide low impedance paths and reduce the effect of glitches on the power supply lines.

An example of layout following these rules is shown in Figure 47 and Figure 48.

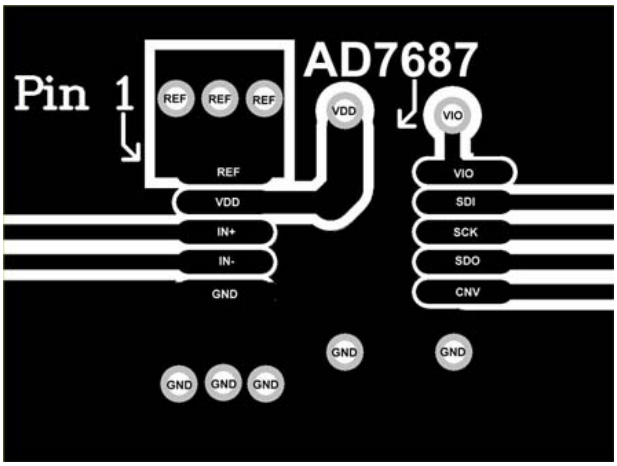

Figure 47. Example of Layout of the AD7687 (Top Layer)

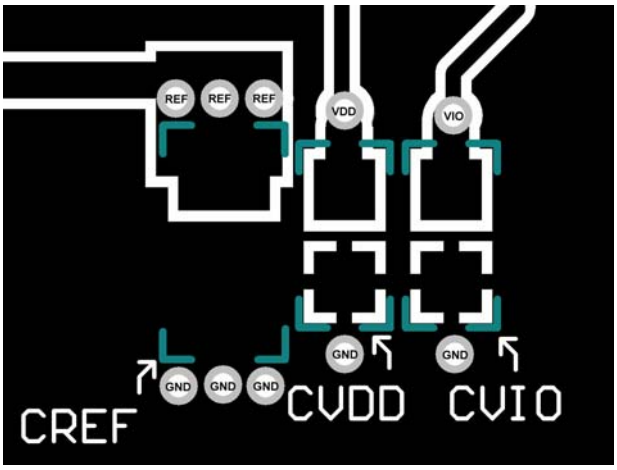

Figure 48. Example of Layout of the AD7687 (Bottom Layer)

EVALUATING THE PERFORMANCE OF THE AD7687

Other recommended layouts for the AD7687 are outlined in the documentation of the EVAL-AD7687SDZ evaluation board. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-SDP-CB1Z.

OUTLINE DIMENSIONS

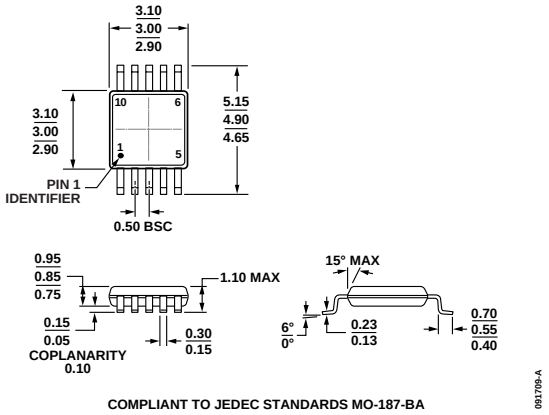

Figure 49. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

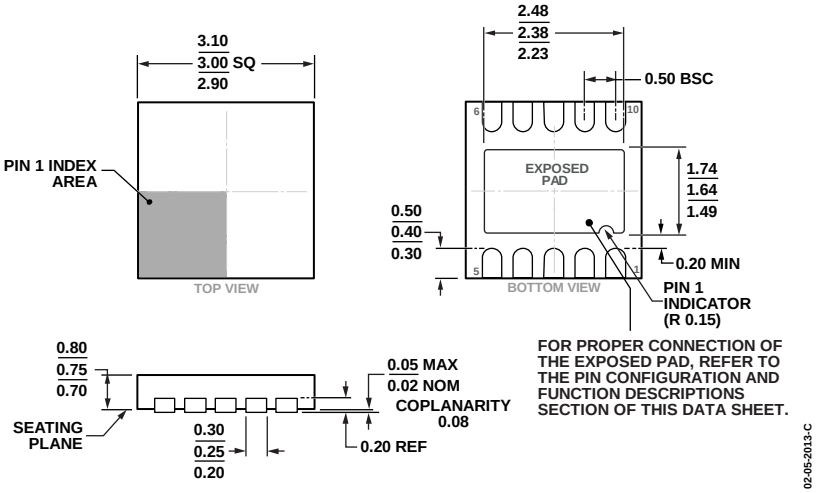

Figure 50. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Integral Nonlinearity	Temperature Range	Transport Media, Quantity	Package Description	Package Option	Branding
AD7687BRMZ	±1.5 LSB max	−40°C to +85°C	Tube, 50	10-Lead MSOP	RM-10	C3Q
AD7687BRMZRL7	±1.5 LSB max	−40°C to +85°C	Reel, 1,000	10-Lead MSOP	RM-10	C3Q
AD7687BCPZRL7	±1.5 LSB max	−40°C to +85°C	Reel, 1,500	10-Lead LFCSP_WD	CP-10-9	#C03
EVAL-AD7687SDZ				Evaluation Board		
EVAL-SDP-CB1Z				Controller Board		

[1] Z = RoHS Compliant Part, # denotes RoHS compliant product, may be top or bottom marked.
[2] The EVAL-AD7687SDZ can be used as a standalone evaluation board or in conjunction with the EVAL-SDP-CB1Z for evaluation and/or demonstration purposes.
[3] The EVAL-SDP-CB1Z allows a PC to control and communicate with all Analog Devices, Inc. evaluation boards ending in the SDZ designator.

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