FAIRCHILD SEMICONDUCTOR®

April 2014

FSBB10CH120D

Motion SPM® 3 Series

Features

- 1200 V - 10 A 3-Phase IGBT Inverter with Integral Gate Drivers and Protection
- Low-Loss, Short-Circuit Rated IGBTs
- Very Low Thermal Resistance Using Al_2O_3 DBC Substrate
- Dedicated Vs Pins Simplify PCB Layout
- Separate Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- Single-Grounded Power Supply
- Isolation Rating: 2500 V_{rms} / 1 min.

Applications

- Motion Control - Industrial Motor (AC 400V Class)

Related Resources

- *AN-9044 - Motion SPM® 3 Series Users Guide*

General Description

FSBB10CH120D is an advanced Motion SPM® 3 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, over-current shutdown, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

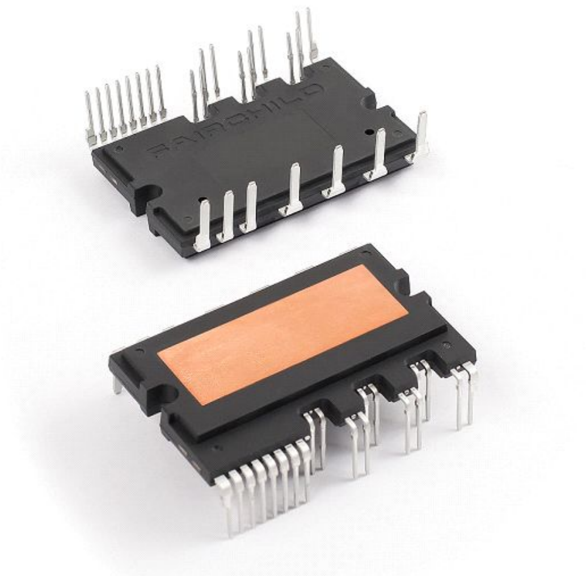


Figure 1. Package Overview

Package Marking and Ordering Information

Device	Device Marking	Package	Packing Type	Quantity
FSBB10CH120D	FSBB10CH120D	SPMMC-027	Rail	10

Integrated Power Functions

- 1200 V - 10 A IGBT inverter for three-phase DC / AC power conversion (*refer to Figure 3*)

Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: gate drive circuit, high-voltage isolated high-speed level shifting control circuit,
  Under-Voltage Lock-Out Protection (UVLO),
  Available bootstrap circuit example is given in Figures 5 and 14.
- For inverter low-side IGBTs: gate drive circuit, Short-Circuit Protection (SCP) control circuit,
  Under-Voltage Lock-Out Protection (UVLO)
- Fault signaling: corresponding to UVLO (low-side supply) and SC faults
- Input interface: active-HIGH interface, works with 3.3 / 5 V logic, Schmitt-trigger input

Pin Configuration

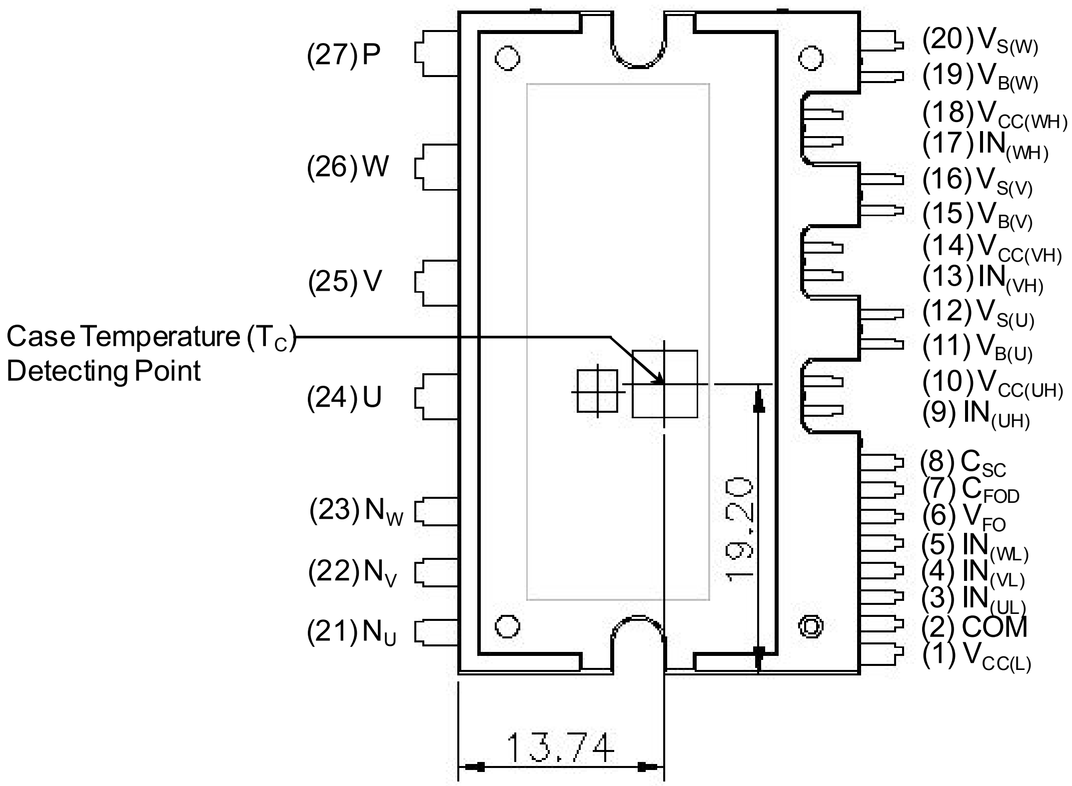


Figure 2. Top View

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	$V_{CC(L)}$	Low-Side Common Bias Voltage for IC and IGBTs Driving
2	COM	Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low-Side U Phase
4	$IN_{(VL)}$	Signal Input for Low-Side V Phase
5	$IN_{(WL)}$	Signal Input for Low-Side W Phase
6	V_{FO}	Fault Output
7	C_{FOD}	Capacitor for Fault Output Duration Time Selection
8	C_{SC}	Capacitor (Low-Pass Filter) for Short-Current Detection Input
9	$IN_{(UH)}$	Signal Input for High-Side U Phase
10	$V_{CC(UH)}$	High-Side Bias Voltage for U Phase IC
11	$V_{B(U)}$	High-Side Bias Voltage for U Phase IGBT Driving
12	$V_{S(U)}$	High-Side Bias Voltage Ground for U Phase IGBT Driving
13	$IN_{(VH)}$	Signal Input for High-Side V Phase
14	$V_{CC(VH)}$	High-Side Bias Voltage for V Phase IC
15	$V_{B(V)}$	High-Side Bias Voltage for V Phase IGBT Driving
16	$V_{S(V)}$	High-Side Bias Voltage Ground for V Phase IGBT Driving
17	$IN_{(WH)}$	Signal Input for High-Side W Phase
18	$V_{CC(WH)}$	High-Side Bias Voltage for W Phase IC
19	$V_{B(W)}$	High-Side Bias Voltage for W Phase IGBT Driving
20	$V_{S(W)}$	High-Side Bias Voltage Ground for W Phase IGBT Driving
21	N_U	Negative DC-Link Input for U Phase
22	N_V	Negative DC-Link Input for V Phase
23	N_W	Negative DC-Link Input for W Phase
24	U	Output for U Phase
25	V	Output for V Phase
26	W	Output for W Phase
27	P	Positive DC-Link Input

Internal Equivalent Circuit and Input/Output Pins

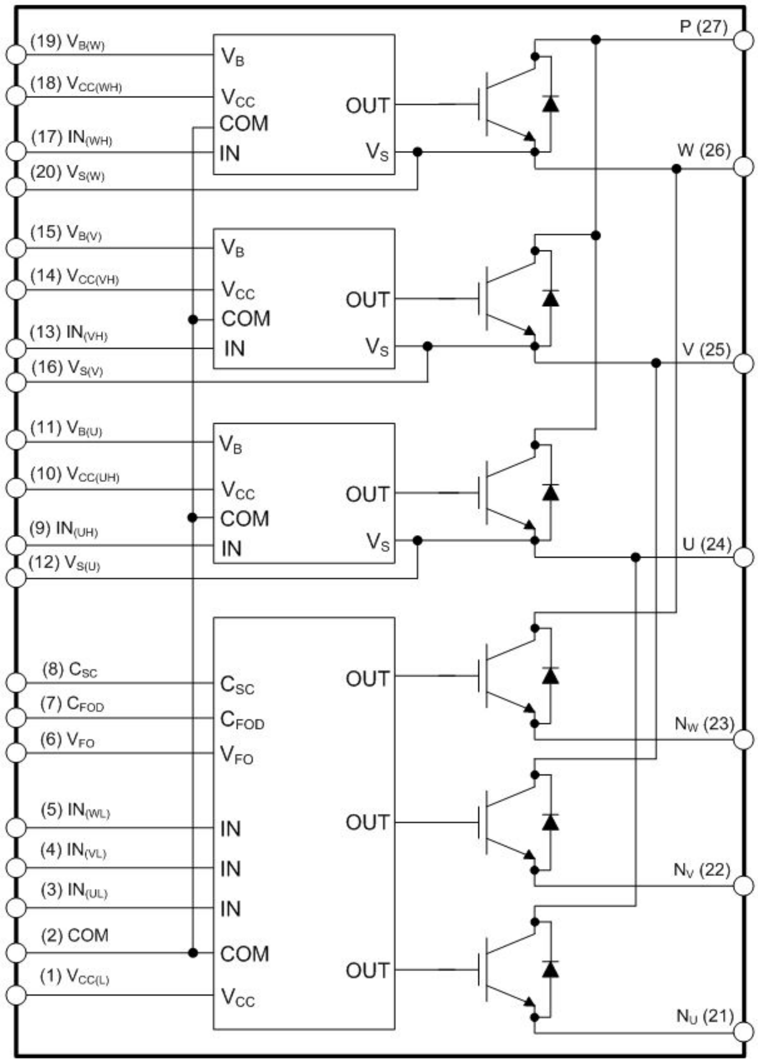


Figure 3. Internal Block Diagram

Notes:

1. Inverter low-side is composed of three IGBTs, freewheeling diodes for each IGBT, and one control IC. It has gate drive and protection functions.
2. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.
3. Inverter high-side is composed of three IGBTs, freewheeling diodes, and three drive ICs for each IGBT.

Absolute Maximum Ratings (T_J = 25°C, unless otherwise specified)

Inverter Part

Symbol	Parameter	Conditions	Rating	Unit
V_{PN}	Supply Voltage	Applied between P - N_U, N_V, N_W	900	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P - N_U, N_V, N_W	1000	V
V_{CES}	Collector - Emitter Voltage		1200	V
± I_C	Each IGBT Collector Current	T_C = 25°C, $T_J \leq$ 150°C (Note 4)	10	A
± I_{CP}	Each IGBT Collector Current (Peak)	T_C = 25°C, $T_J \leq$ 150°C, Under 1 ms Pulse Width (Note 4)	20	A
P_C	Collector Dissipation	T_C = 25°C per One Chip (Note 4)	69	W
T_J	Operating Junction Temperature		-40 ~ 150	°C

Control Part

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$, $V_{CC(L)}$ - COM	20	V
V_{BS}	High-Side Control Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM	-0.3 ~ V_{CC}+0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} - COM	-0.3 ~ V_{CC}+0.3	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} pin	2	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC} - COM	-0.3 ~ V_{CC}+0.3	V

Total System

Symbol	Parameter	Conditions	Rating	Unit
$V_{PN(PROT)}$	Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	V_{CC} = V_{BS} = 13.5 ~ 16.5 V, T_J = 150°C, Non-repetitive, < 2 μs	800	V
T_C	Module Case Operation Temperature	*See Figure 2*	-40 ~ 125	°C
T_{STG}	Storage Temperature		-40 ~ 125	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate	2500	V_{rms}

Thermal Resistance

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$R_{th(j-c)Q}$	Junction-to-Case Thermal Resistance (Note 5)	Inverter IGBT part (per 1 / 6 module)	-	-	1.80	°C / W
$R_{th(j-c)F}$		Inverter FWD part (per 1 / 6 module)	-	-	2.75	°C / W

Notes:

4. These values had been made an acquisition by the calculation considered to design factor.
5. For the measurement point of case temperature (T_C), *please refer to Figure 2.*

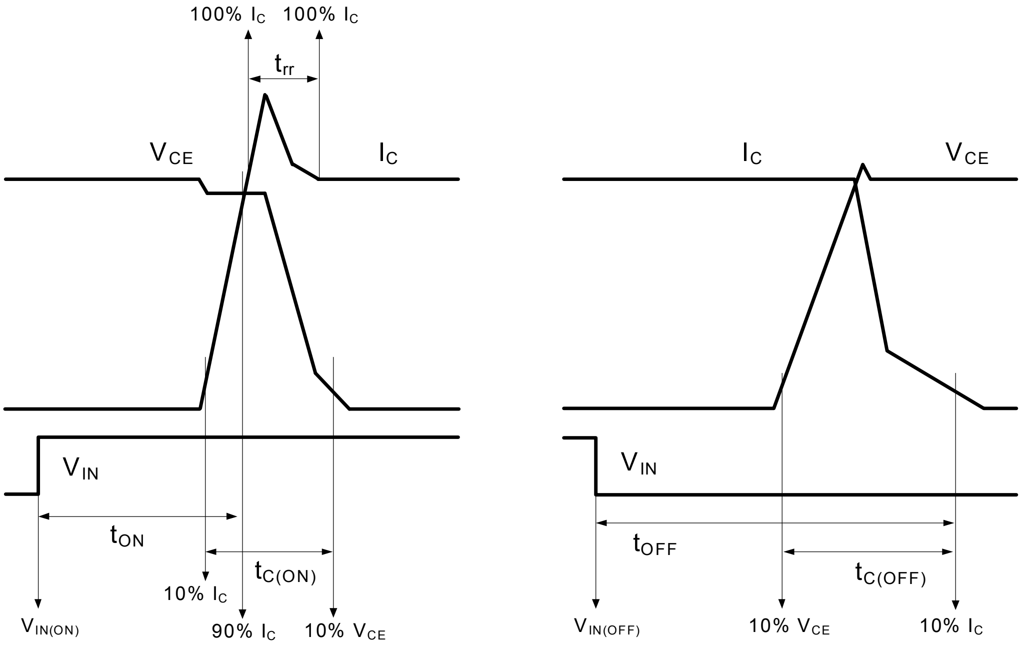
Electrical Characteristics (T_J = 25°C, unless otherwise specified)

Inverter Part

Symbol		Parameter	Conditions		Min.	Typ.	Max.	Unit
$V_{CE(SAT)}$		Collector - Emitter Saturation Voltage	V_{CC} = V_{BS} = 15 V V_{IN} = 5 V	I_C = 10 A, T_J = 25°C	-	2.20	2.80	V
V_F		FWDi Forward Voltage	V_{IN} = 0 V	I_F = 10 A, T_J = 25°C	-	2.20	2.80	V
HS	t_{ON}	Switching Times	V_{PN} = 600 V, V_{CC} = 15 V, I_C = 10 A T_J = 25°C V_{IN} = 0 V ↔ 5 V, Inductive Load *See Figure 5* (Note 6)		0.45	0.85	1.35	μs
	$t_{C(ON)}$				-	0.25	0.60	μs
	t_{OFF}				-	0.95	1.50	μs
	$t_{C(OFF)}$				-	0.10	0.45	μs
	t_{rr}				-	0.25	-	μs
LS	t_{ON}		V_{PN} = 600 V, V_{CC} = 15 V, I_C = 10 A T_J = 25°C V_{IN} = 0 V ↔ 5 V, Inductive Load *See Figure 5* (Note 6)		0.35	0.75	1.25	μs
	$t_{C(ON)}$				-	0.20	0.55	μs
	t_{OFF}				-	0.95	1.50	μs
	$t_{C(OFF)}$				-	0.10	0.45	μs
	t_{rr}				-	0.20	-	μs
I_{CES}		Collector - Emitter Leakage Current	V_{CE} = V_{CES}		-	-	5	mA

Note:

6. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, *please see Figure 4.*



(a) turn-on **(b) turn-off**

Figure 4. Switching Time Definition

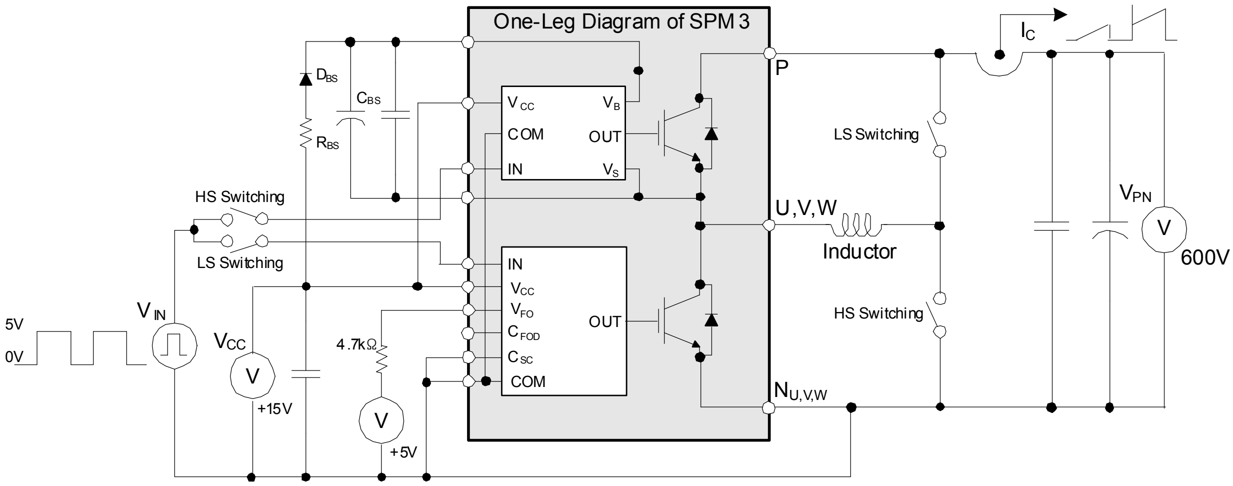


Figure 5. Example Circuit for Switching Test

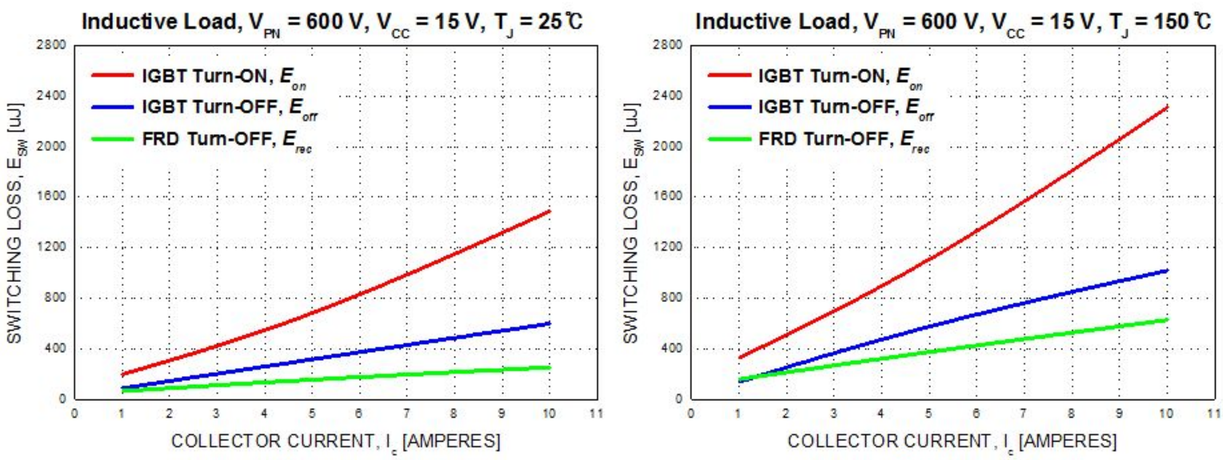


Figure 6. Switching Loss Characteristics (Typical)

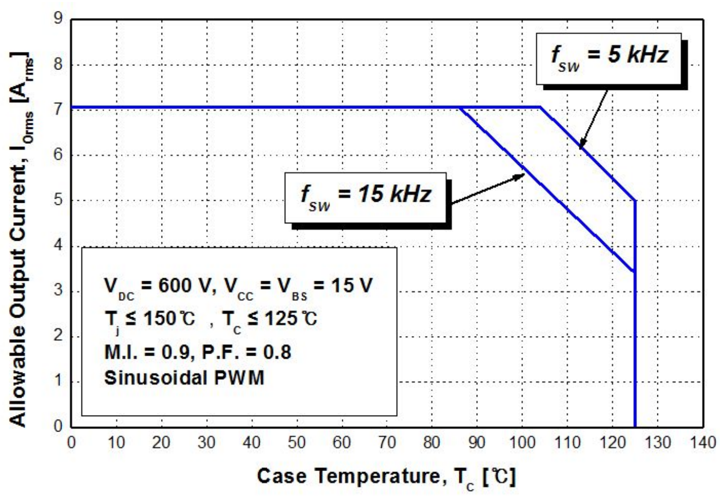


Figure 7. Allowable Maximum Output Current

Note:

7. This allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating condition.

Control Part

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{QCCH}	Quiescent V_{CC} Supply Current	$V_{CC(UH,VH,WH)}$ = 15 V, $IN_{(UH,VH,WH)}$ = 0 V	$V_{CC(UH)}$ - COM, $V_{CC(VH)}$ - COM, $V_{CC(WH)}$ - COM	-	-	0.15	mA
I_{QCCL}		$V_{CC(L)}$ = 15 V, $IN_{(UL,VL,WL)}$ = 0 V	$V_{CC(L)}$ - COM	-	-	5.00	mA
I_{PCCH}	Operating V_{CC} Supply Current	$V_{CC(UH,VH,WH)}$ = 15 V, f_{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for High-Side	$V_{CC(UH)}$ - COM, $V_{CC(VH)}$ - COM, $V_{CC(WH)}$ - COM	-	-	0.30	mA
I_{PCCL}		$V_{CC(L)}$ = 15V, f_{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for Low-Side	$V_{CC(L)}$ - COM	-	-	8.50	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS} = 15 V, $IN_{(UH, VH, WH)}$ = 0 V	$V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	-	-	0.30	mA
I_{PBS}	Operating V_{BS} Supply Current	V_{CC} = V_{BS} = 15 V, f_{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for High-Side	$V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	-	-	4.50	mA
V_{FOH}	Fault Output Voltage	V_{CC} = 15 V, V_{SC} = 0 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-up		4.5	-	-	V
V_{FOL}		V_{CC} = 15 V, V_{SC} = 1 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-up		-	-	0.5	V
$V_{SC(ref)}$	Short Circuit Trip Level	V_{CC} = 15 V (Note 8)	C_{SC} - COM	0.43	0.50	0.57	V
UV_{CCD}	Supply Circuit Under-Voltage Protection	Detection Level		10.3	-	12.8	V
UV_{CCR}		Reset Level		10.8	-	13.3	V
UV_{BSD}		Detection Level		9.5	-	12.0	V
UV_{BSR}		Reset Level		10.0	-	12.5	V
t_{FOD}	Fault-Out Pulse Width	C_{FOD} = open	(Note 9)	50	-	-	μs
		C_{FOD} = 2.2 nF		1.7	-	-	ms
$V_{IN(ON)}$	ON Threshold Voltage	Applied between $IN_{(UH, VH, WH)}$ - COM, $IN_{(UL, VL, WL)}$ - COM		-	-	2.6	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.8	-	-	V

Notes:

8. Short-circuit current protection is functioning only at the low-sides.

9. The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation : $t_{FOD} = 0.8 \times 10^6 \times C_{FOD}$ [s].

Recommended Operating Conditions

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied between P - N_U, N_V, N_W	300	600	800	V
V_{CC}	Control Supply Voltage	Applied between $V_{CC(UH, VH, WH)}$ - COM, $V_{CC(L)}$ - COM	13.5	15.0	16.5	V
V_{BS}	High-Side Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	13.0	15.0	18.5	V
dV_{CC} / dt, dV_{BS} / dt	Control Supply Variation		-1	-	1	V / μs
t_{dead}	Blanking Time for Preventing Arm - Short	For Each Input Signal	2.0	-	-	μs
f_{PWM}	PWM Input Signal	-40°C ≤ T_C ≤ 125°C, -40°C ≤ T_J ≤ 150°C	-	-	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W - COM (Including Surge Voltage)	-5		5	V
$PW_{IN(ON)}$	Minimun Input Pulse Width	I_C ≤ 20 A, Wiring Inductance between $N_{U, V, W}$ and DC Link N < 10nH (Note 10)	1.5	-	-	μs
$PW_{IN(OFF)}$			1.5	-	-	
T_J	Junction Temperature		-40	-	150	°C

Note:

10. This product might not make output response if input pulse width is less than the recommanded value.

Mechanical Characteristics and Ratings

Parameter	Conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
Device Flatness	*See Figure 8*		0	-	+150	µm
Mounting Torque	Mounting Screw: M3	Recommended 0.7 N • m	0.6	0.7	0.8	N • m
	See Figure 9	Recommended 7.1 kg • cm	6.2	7.1	8.1	kg • cm
Terminal Pulling Strength	Load 19.6 N		10	-	-	s
Terminal Bending Strength	Load 9.8 N, 90 deg. bend		2	-	-	times
Weight			-	15	-	g

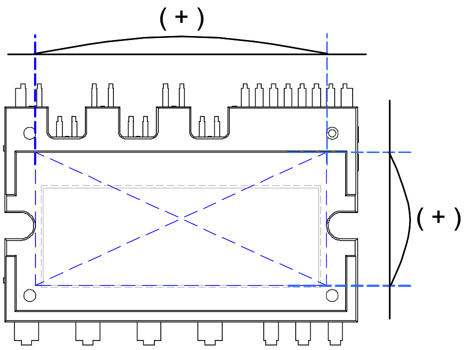


Figure 8. Flatness Measurement Position

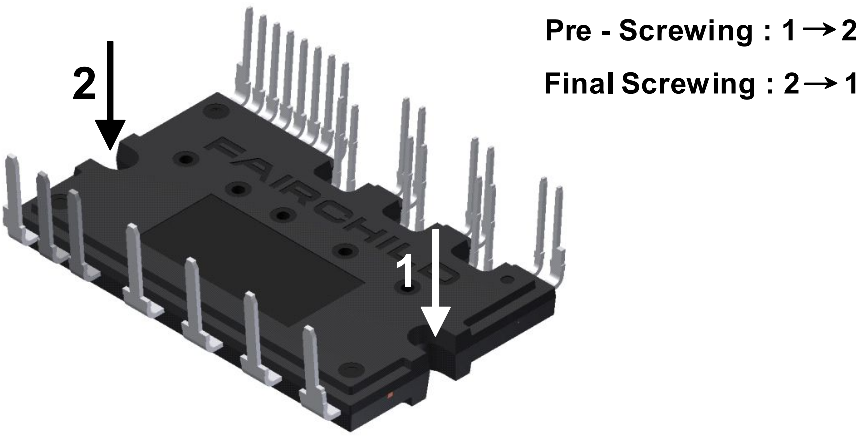


Figure 9. Mounting Screws Torque Order

Note:

11. Do not make over torque when mounting screws. Much mounting torque may cause DBC cracks, as well as bolts and Al heat-sink destruction.

12. Avoid one-side tightening stress. Figure 9 shows the recommended torque order for mounting screws. Uneven mounting can cause the ceramic substrate of package to be damaged. The pre-screwing torque is set to 20 ~ 30% of maximum torque rating.

Time Charts of SPMs Protective Function

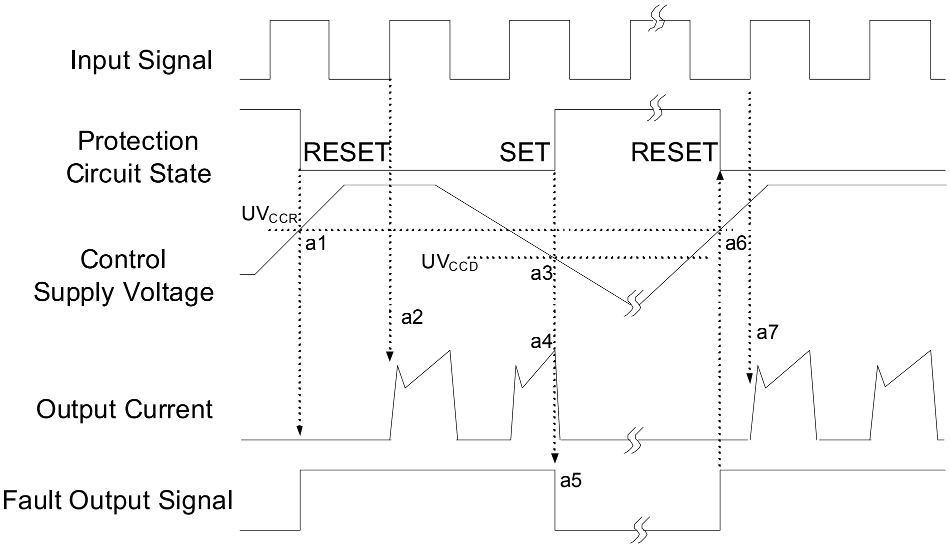


Figure 10. Under-Voltage Protection (Low-Side)

a1 : Control supply voltage rises: After the voltage rises UV_{CCR}, the circuits start to operate when next input is applied.

a2 : Normal operation: IGBT ON and carrying current.

a3 : Under-voltage detection (UV_{CCD}).

a4 : IGBT OFF in spite of control input condition.

a5 : Fault output operation starts with a fixed pulse width according to the condition of the external capacitor C_{FOD}.

a6 : Under-voltage reset (UV_{CCR}).

a7 : Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

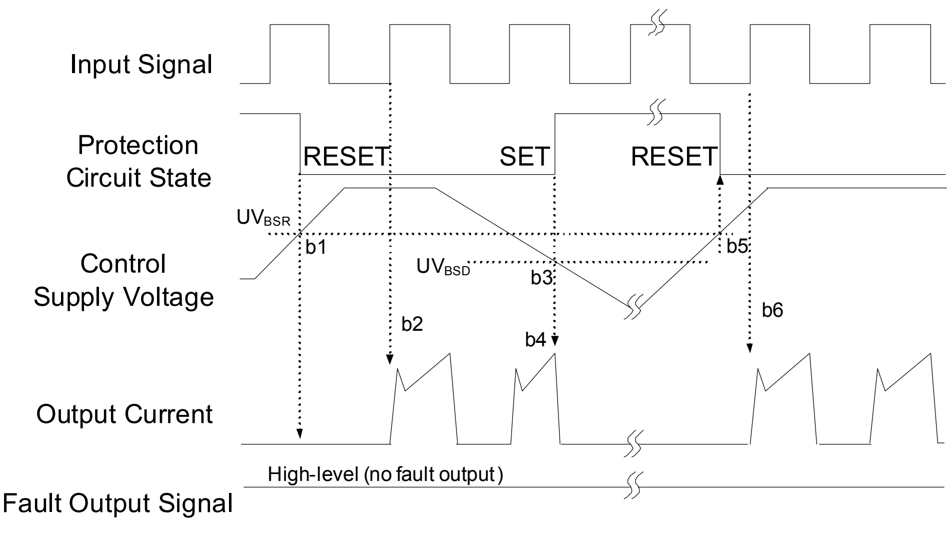


Figure 11. Under-Voltage Protection (High-Side)

b1 : Control supply voltage rises: After the voltage reaches UV_{BSR}, the circuits start to operate when next input is applied.

b2 : Normal operation: IGBT ON and carrying current.

b3 : Under-voltage detection (UV_{BSD}).

b4 : IGBT OFF in spite of control input condition, but there is no fault output signal.

b5 : Under-voltage reset (UV_{BSR}).

b6 : Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

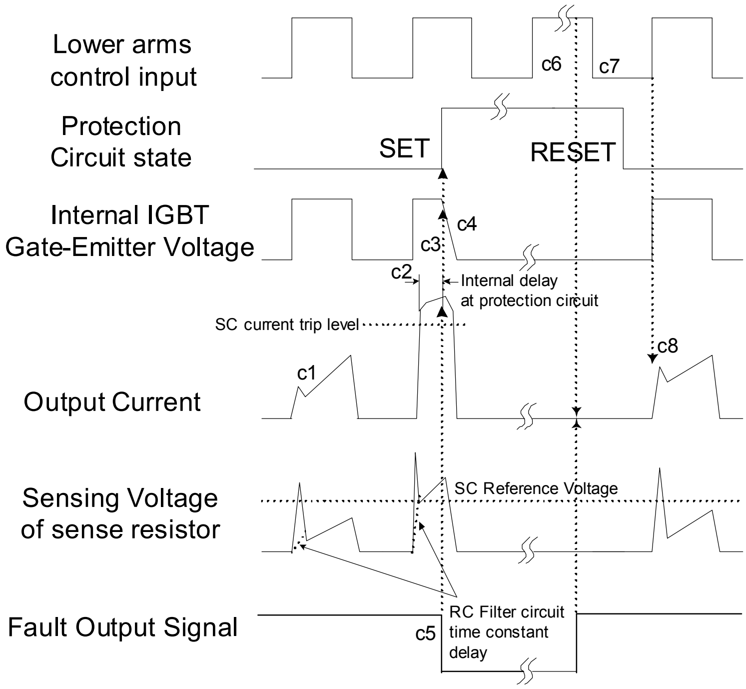


Figure 12. Short-Circuit Current Protection (Low-Side Operation only)

(with the external sense resistance and RC filter connection)

c1 : Normal operation: IGBT ON and carrying current.

c2 : Short circuit current detection (SC trigger).

c3 : All low-side IGBT's gate are hard interrupted.

c4 : All low-side IGBTs turn OFF.

c5 : Fault output operation starts with a fixed pulse width.

c6 : Input HIGH: IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.

c7 : Fault output operation finishes, but IGBT doesn't turn on until triggering next signal from LOW to HIGH.

c8 : Normal operation: IGBT ON and carrying current.

Input/Output Interface Circuit

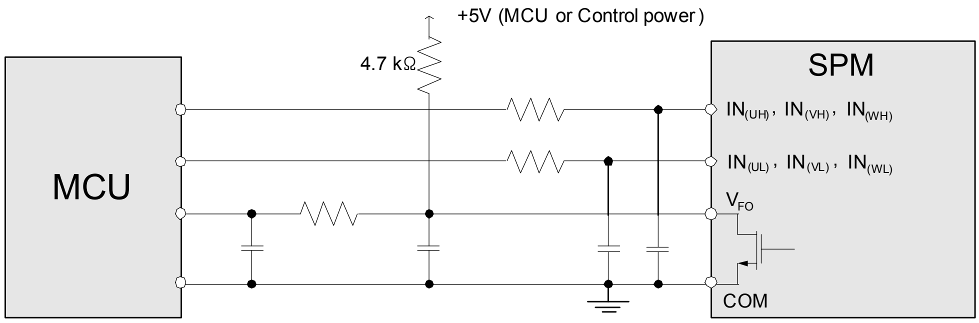


Figure 13. Recommended MCU I/O Interface Circuit

Note:

13. RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section of the Motion SPM 3 product integrates 5 kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

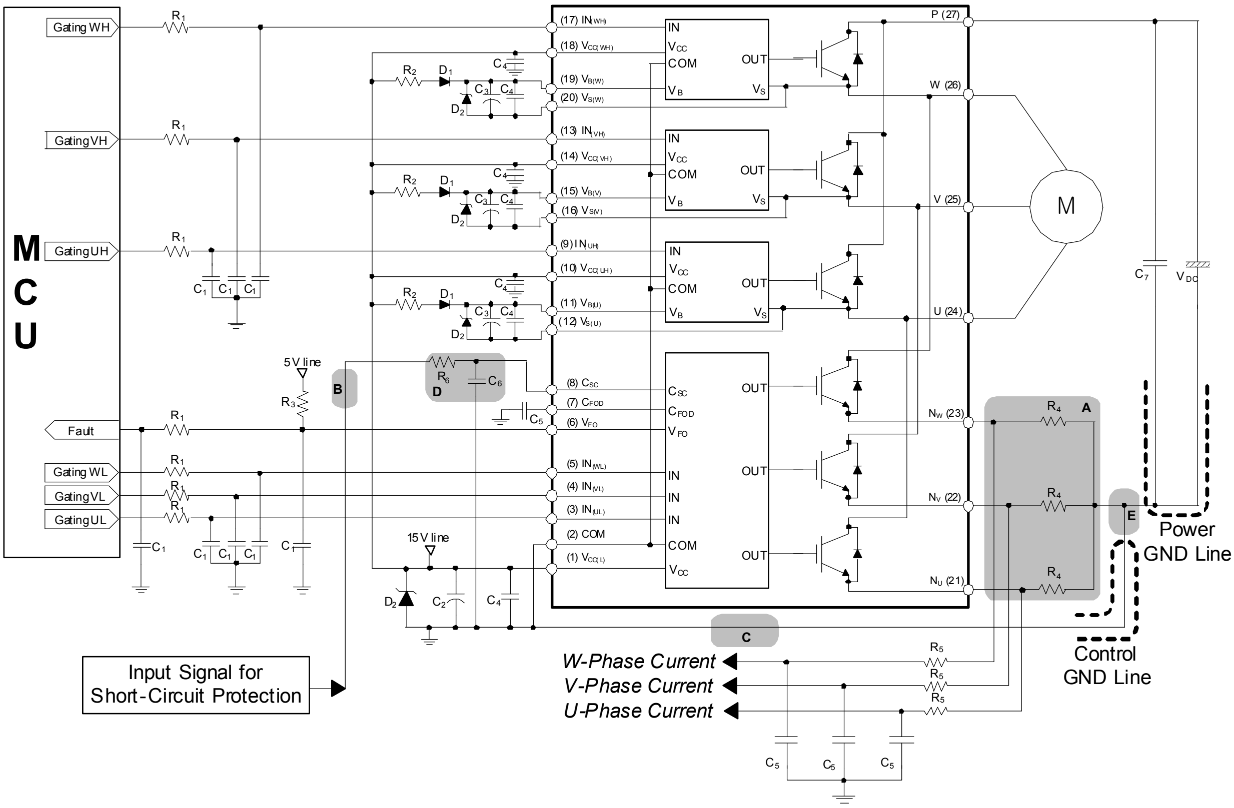


Figure 14. Typical Application Circuit

Notes:

14. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2 - 3 cm)

15. V_{FO} output is open-drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes I_{FO} up to 2 mA. *Please refer to Figure 14.*

16. Fault out pulse width can be adjust by capacitor C_5 connected to the C_{FOD} terminal.

17. Input signal is active-HIGH type. There is a 5 kΩ resistor inside the IC to pull-down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. R_1C_1 time constant should be selected in the range 50 ~ 150 ns. (recommended R_1 = 100 Ω, C_1 = 1 nF)

18. Each wiring pattern inductance of point A should be minimized (recommend less than 10 nH). Use the shunt resistor R_4 of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring of point E should be connected to the terminal of the shunt resistor R_4 as close as possible.

19. To prevent errors of the protection function, the wiring of B, C, and D point should be as short as possible.

20. In the short-circuit protection circuit, select the R_6C_6 time constant in the range 1.0 ~ 1.5 μs. Do enough evaluaiton on the real system because short-circuit protection time may vary wiring pattern layout and value of the R_6C_6 time constant.

21. Each capacitor should be mounted as close to the pins of the Motion SPM® 3 product as possible.

22. To prevent surge destruction, the wiring between the smoothing capacitor C_7 and the P & GND pins should be as short as possible. The use of a high-frequency non-inductive capacitor of around 0.1 ~ 0.22 μF between the P & GND pins is recommended.

23. Relays are used in most systems of electrical equipments in industrial application. In these cases, there should be sufficient distance between the MCU and the relays.

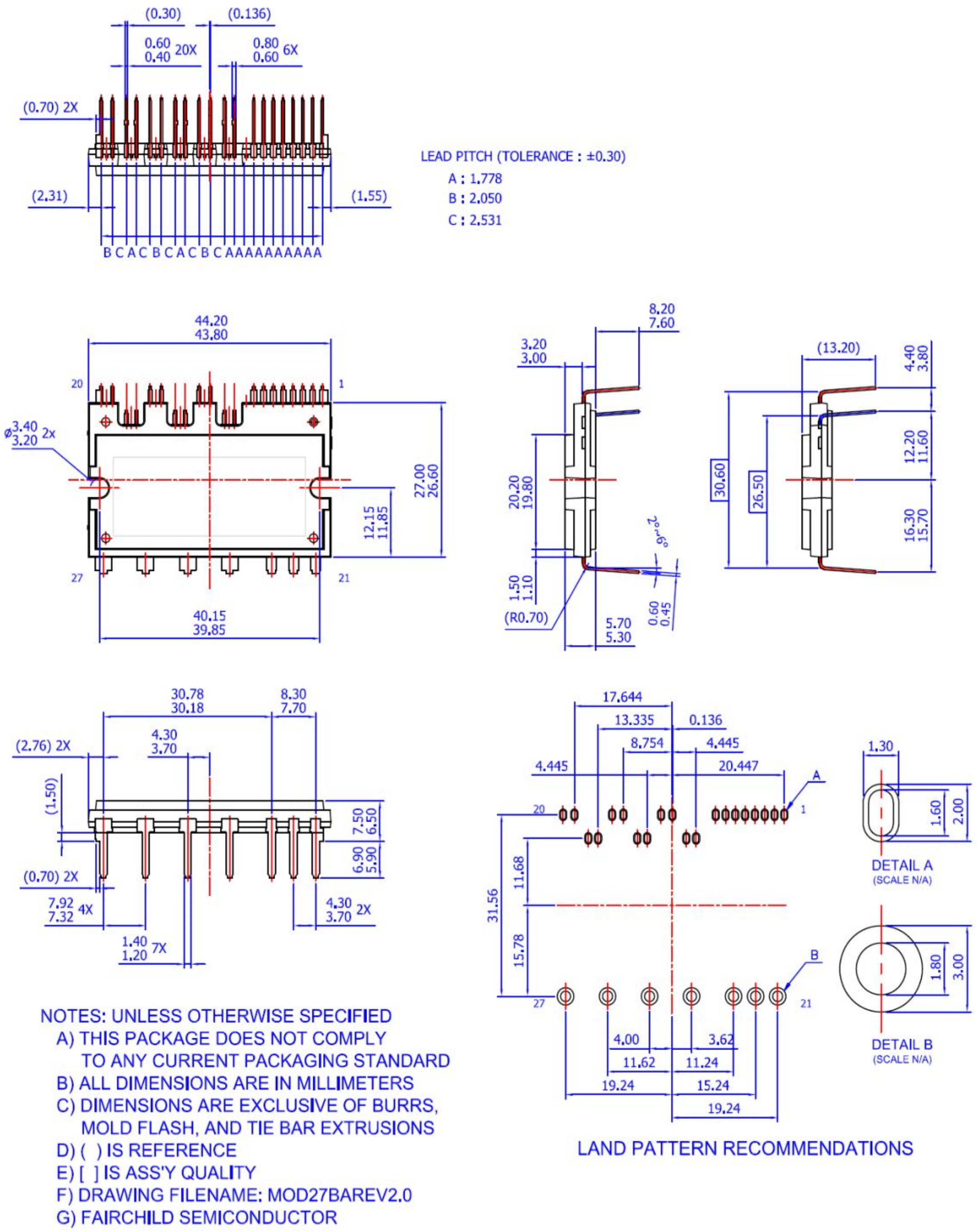
24. The Zener diode or transient voltage suppressor D_2 should be adapted for the protection of ICs from the surge destruction between each pair of control supply terminals (recommanded Zener diode is 22 V / 1 W, which has the lower Zener impedance characteristic than about 15 Ω).

25. Boostrap capacitor C_3 and Bootstrap resistor R_2 values depend on PWM control algorithm. And, C_2 of around seven times larger than bootstrap capacitor C_3 is recommended.

26. Please choose the electrolytic capacitor with good temperature characteristic in C_3. Choose 0.1 ~ 0.2 μF R-category ceramic capacitors with good temperature and frequency characteristics in C_4.

27. Use the bootstrap diode D_1 which has high voltage(V_{RRM} = 1200 V or more), soft, and fast recovery(t_{RR} = less than 100 ns) characteristics.

Detailed Package Outline Drawings (FSBB10CH120D)



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SuperSOT™-8
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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I66

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