Single Channel, Ultra-Low Resistance Load Switch

Check for Samples: TPS22967

FEATURES

- **Integrated Single Channel Load Switch**
- **Input Voltage Range: 0.8V to 5.5V**
- **Ultra low R_{ON} Resistance**
  - **R_{ON} = 22mΩ at V_{IN} = 5V (V_{BIAS} = 5V)**
  - **R_{ON} = 22mΩ at V_{IN} = 3.6V (V_{BIAS} = 5V)**
  - **R_{ON} = 22mΩ at V_{IN} = 1.8V (V_{BIAS} = 5V)**
- **4A Maximum Continuous Switch Current**
- **Low Quiescent Current (50µA)**
- **Low Control Input Threshold Enables Use of 1.2V/1.8V/2.5V/3.3V Logic**
- **Configurable Rise Time**
- **Quick Output Discharge (QOD)**
- **SON 8-pin Package With Thermal Pad**
- **ESD Performance Tested per JESD 22**
  - **2KV HBM and 1KV CDM**

APPLICATIONS

- **Ultrabook™**
- **Notebooks/Netbooks**
- **Tablet PC**
- **Consumer Electronics**
- **Set-top Boxes/Residental Gateways**
- **Telecom Systems**
- **Solid State Drives (SSD)**

DESCRIPTION

The TPS22967 is a small, ultra-low R_{ON}, single channel load switch with controlled turn on. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.8V to 5.5V and can support a maximum continuous current of 4A. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. In the TPS22967, a 225-Ω pull-down resistor is added for quick output discharge when switch is turned off.

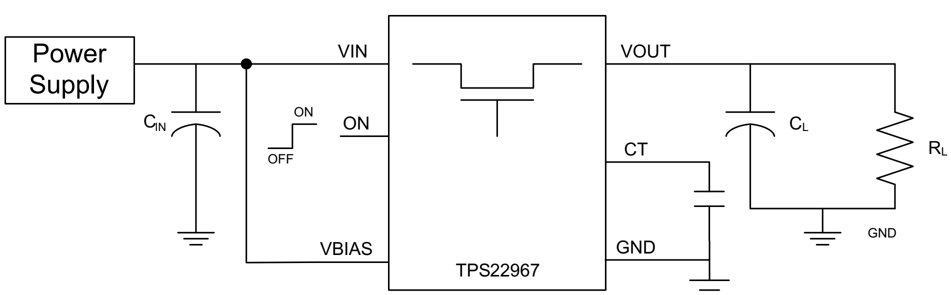
The TPS22967 is available in a small, space-saving 2mm x 2mm 8-pin SON package (DSG) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

Feature List

R_{ON} Typical at 3.6 V (V_{BIAS} = 5V)	22 mΩ
Rise Time(1)	Adjustable
Quick Output Discharge(2)	Yes
Maximum Output Current	4 A
GPIO Enable	Active High
Operating Temperature	–40°C to 85°C

(1) See Application Information section for CT cap value vs. rise time.

(2) This feature discharges the output of the switch to GND through a 225-Ω resistor, preventing the output from floating.



Typical Application

ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum at the end of this document.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)(2)

			VALUE	UNIT(2)
V_{IN}	Input voltage range		–0.3 to 6	V
V_{OUT}	Output voltage range		–0.3 to 6	V
V_{BIAS}	Bias voltage range		–0.3 to 6	V
V_{ON}	ON voltage range		–0.3 to 6	V
I_{MAX}	Maximum continuous switch current		4	A
I_{PLS}	Maximum pulsed switch current, pulse <300 µs, 2% duty cycle		6	A
T_A	Operating free-air temperature range(3)		–40 to 85	°C
T_J	Maximum junction temperature		125	°C
T_{STG}	Storage temperature range		–65 to 150	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)	2000	V
		Charged-Device Model (CDM)	1000	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $TA_{(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$

THERMAL INFORMATION

THERMAL METRIC(1)		TPS22967	UNITS
		DSG (8 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	65.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	74.2	
θ_{JB}	Junction-to-board thermal resistance	35.4	
ψ_{JT}	Junction-to-top characterization parameter	2.2	
ψ_{JB}	Junction-to-board characterization parameter	36.0	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	12.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{IN}	Input voltage range		0.8	V_{BIAS}	V
V_{BIAS}	Bias voltage range		2.5	5.5	V
V_{ON}	ON voltage range		0	5.5	V
V_{OUT}	Output voltage range			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	1.2	5.5	V
V_{IL}	Low-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	0	0.5	V
C_{IN}	Input capacitor		1 (1)		µF

(1) Refer to Application Information section.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature **–40°C ≤ T_A ≤ 85°C** (Full) and **V_{BIAS} = 5.0 V**. Typical values are for T_A = 25°C.

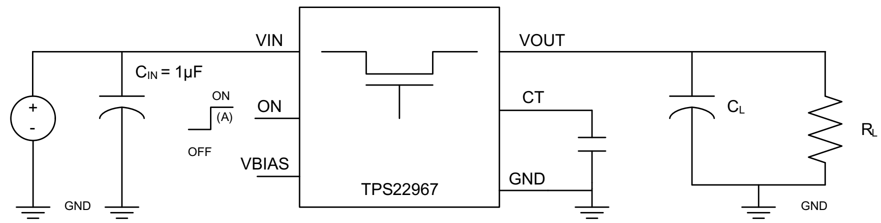
PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = V_{ON} = V_{BIAS} = 5.0 V		Full		50	75	µA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		Full			2	µA
$I_{IN(VIN-OFF)}$	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 5.0 V	Full		0.2	8	µA
			V_{IN} = 3.3 V			0.02	3	
			V_{IN} = 1.8 V			0.01	2	
			V_{IN} = 0.8 V			0.005	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		Full			0.5	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 5.0 V	V_{IN} = 5.0 V	25°C		22	33	mΩ
				Full			35	
			V_{IN} = 3.3 V	25°C		22	33	mΩ
				Full			35	
			V_{IN} = 1.8 V	25°C		22	33	mΩ
				Full			35	
			V_{IN} = 1.5 V	25°C		22	33	mΩ
				Full			35	
			V_{IN} = 1.2 V	25°C		22	33	mΩ
				Full			35	
			V_{IN} = 0.8 V	25°C		22	33	mΩ
				Full			35	
R_{PD}	Output pulldown resistance	V_{IN} = 5.0 V, V_{ON} = 0V, I_{OUT} = 15 mA		Full		225	300	Ω

ELECTRICAL CHARACTERISTICS

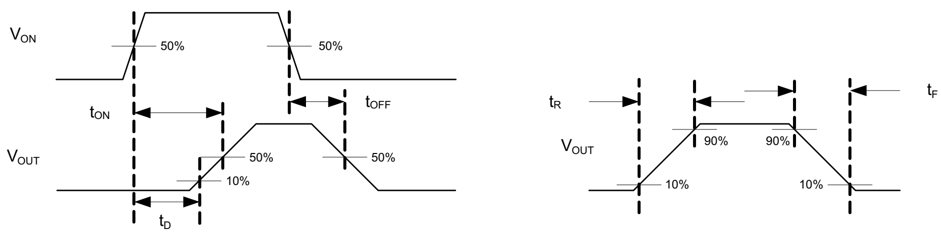
Unless otherwise noted, the specification in the following table applies over the operating ambient temperature **–40°C ≤ T_A ≤ 85°C** (Full) and **V_{BIAS} = 2.5 V**. Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = V_{ON} = V_{BIAS} = 2.5 V		Full		20	30	µA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		Full			2	µA
$I_{IN(VIN-OFF)}$	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 2.5 V	Full		0.01	3	µA
			V_{IN} = 1.8 V			0.01	2	
			V_{IN} = 1.2 V			0.005	2	
			V_{IN} = 0.8 V			0.003	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		Full			0.5	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 2.5 V	V_{IN} = 2.5 V	25°C		26	38	mΩ
				Full			40	
			V_{IN} = 1.8 V	25°C		26	38	mΩ
				Full			40	
			V_{IN} = 1.5 V	25°C		25	38	mΩ
				Full			40	
			V_{IN} = 1.2 V	25°C		24	38	mΩ
				Full			40	
			V_{IN} = 0.8 V	25°C		24	38	mΩ
				Full			40	
R_{PD}	Output pulldown resistance	V_{IN} = 2.5 V, V_{ON} = 0V, I_{OUT} = 1 mA		Full		275	325	Ω

SWITCHING CHARACTERISTIC MEASUREMENT INFORMATION



TEST CIRCUIT



t_{ON}/t_{OFF} WAVEFORMS

(A) Rise and fall times of the control signal is 100ns.

Figure 1. Test Circuit and Timing Waveforms

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{IN} = V_{ON} = V_{BIAS} = 5$ V, $T_A = 25$ºC (unless otherwise noted)						
t_{ON}	Turn-on time	$R_L = 10$-Ω, $C_L = 0.1$ µF, $C_T = 1000$ pF		1325		µs
t_{OFF}	Turn-off time			10		
t_R	V_{OUT} rise time			1625		
t_F	V_{OUT} fall time			3.5		
t_D	ON delay time			500		
$V_{IN} = 0.8$ V, $V_{ON} = V_{BIAS} = 5$V, $T_A = 25$ºC (unless otherwise noted)						
t_{ON}	Turn-on time	$R_L = 10$-Ω, $C_L = 0.1$ µF, $C_T = 1000$ pF		600		µs
t_{OFF}	Turn-off time			80		
t_R	V_{OUT} rise time			300		
t_F	V_{OUT} fall time			5.5		
t_D	ON delay time			460		
$V_{IN} = 2.5$V, $V_{ON} = 5$ V, $V_{BIAS} = 2.5$V, $T_A = 25$ºC (unless otherwise noted)						
t_{ON}	Turn-on time	$R_L = 10$-Ω, $C_L = 0.1$ µF, $C_T = 1000$ pF		2200		µs
t_{OFF}	Turn-off time			9		
t_R	V_{OUT} rise time			2275		
t_F	V_{OUT} fall time			3.1		
t_D	ON delay time			1075		
$V_{IN} = 0.8$ V, $V_{ON} = 5$ V, $V_{BIAS} = 2.5$ V, $T_A = 25$ºC (unless otherwise noted)						
t_{ON}	Turn-on time	$R_L = 10$-Ω, $C_L = 0.1$ µF, $C_T = 1000$ pF		1450		µs
t_{OFF}	Turn-off time			60		
t_R	V_{OUT} rise time			875		
t_F	V_{OUT} fall time			5.5		
t_D	ON delay time			1010		

FUNCTIONAL BLOCK DIAGRAM

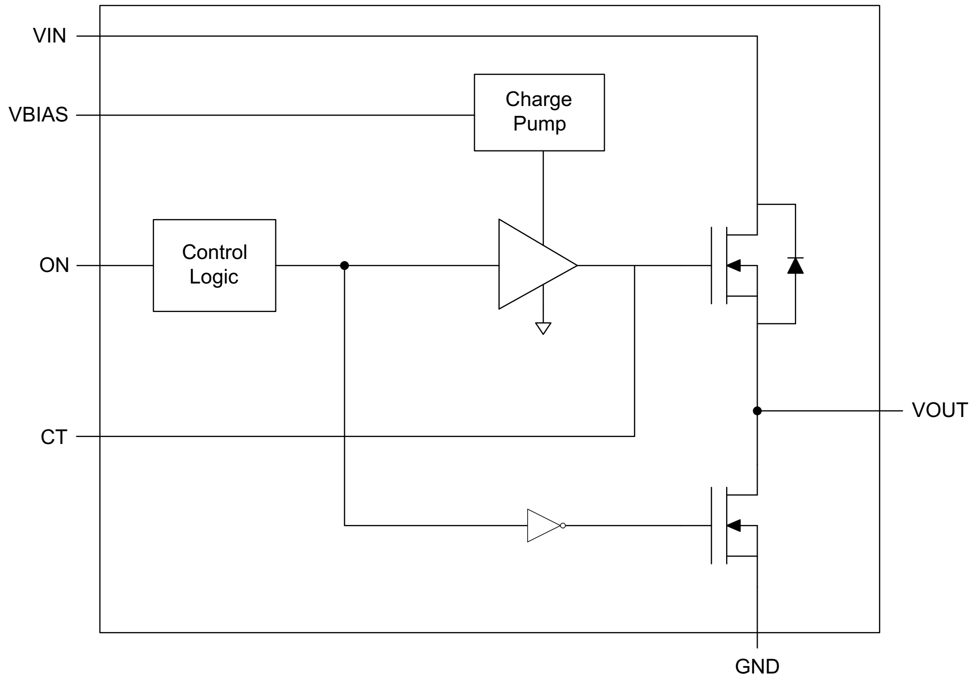
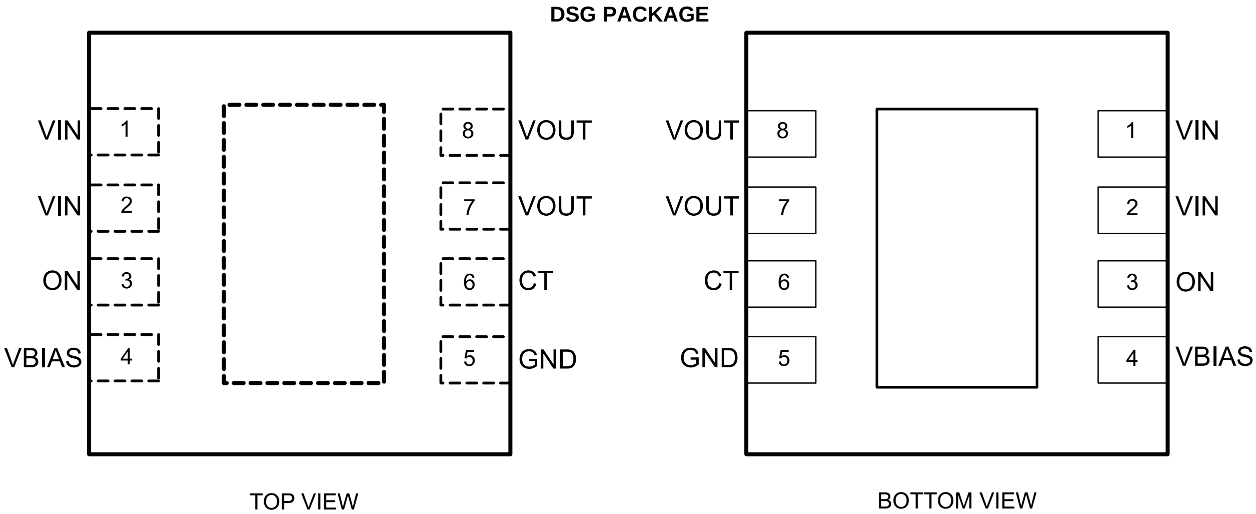


Figure 2. Functional Block Diagram

Table 1. FUNCTIONAL TABLE

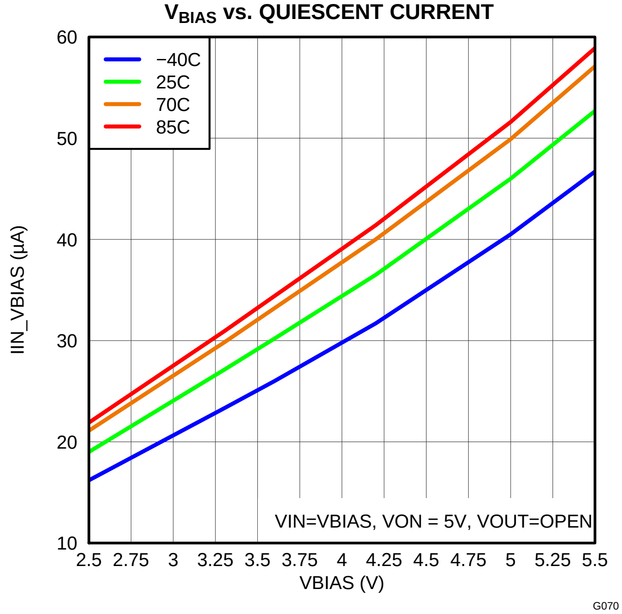
ON	VIN to VOUT	VOUT to GND
L	Off	On
H	On	Off

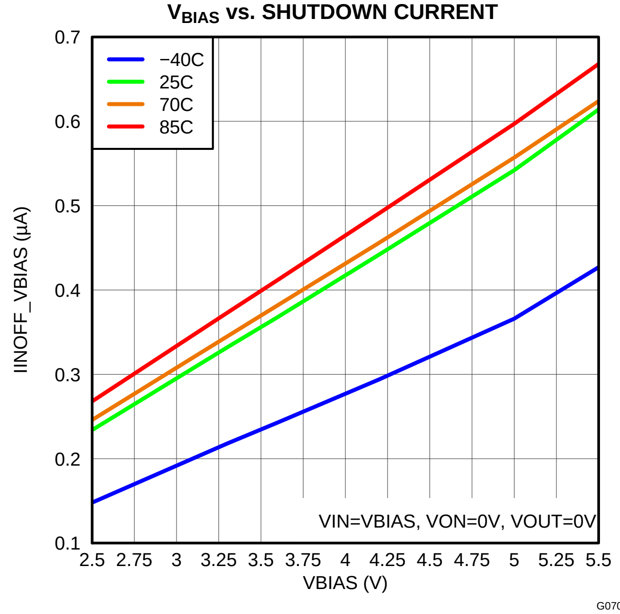


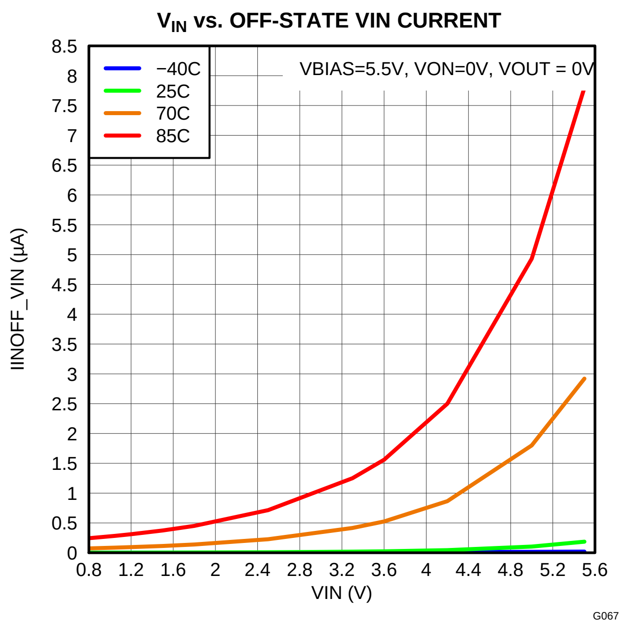
PIN DESCRIPTIONS

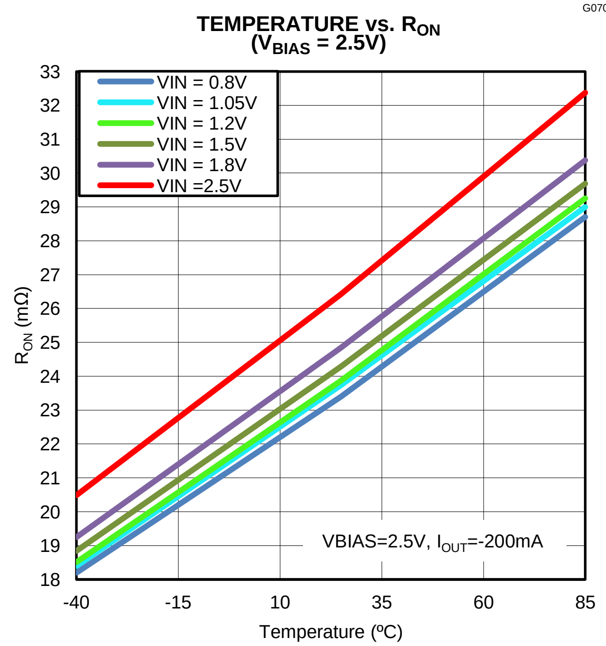
TPS22967 DSG	PIN NAME	I/O	DESCRIPTION
1	VIN	I	Switch input. Input capacitor recommended for minimizing V_{IN} dip. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8V to V_{BIAS}.
2	VIN	I	Switch input. Input capacitor recommended for minimizing V_{IN} dip. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8V to V_{BIAS}.
3	ON	I	Active high switch control input. Do not leave floating.
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5V to 5.5V. See Application Information section for more information.
5	GND	-	Device ground.
6	CT	O	Switch slew rate control. Can be left floating. See Application Information section for more information.
7	VOUT	O	Switch output.
8	VOUT	O	Switch output.
	Thermal Pad	-	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See Application Information for layout guidelines.

TYPICAL CHARACTERISTICS



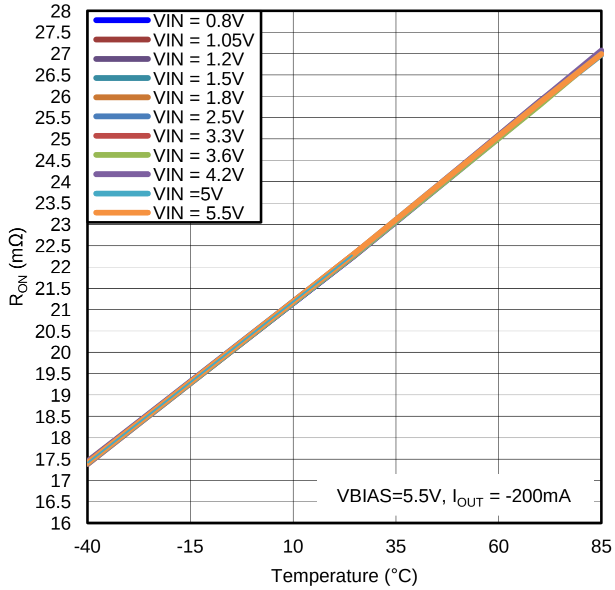




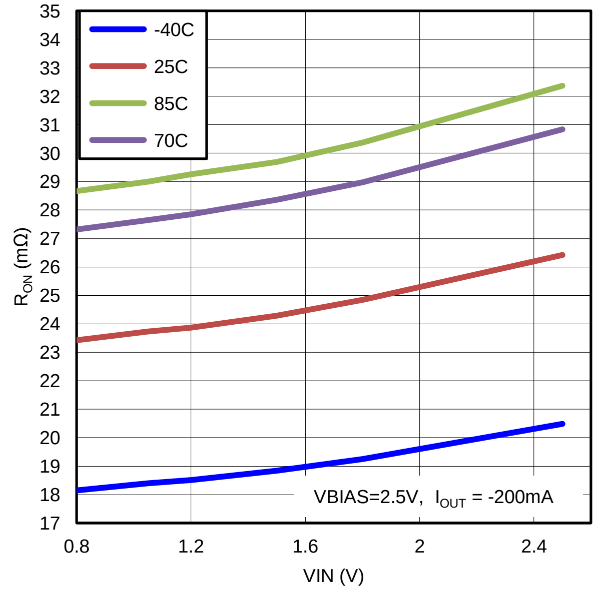


TYPICAL CHARACTERISTICS (continued)

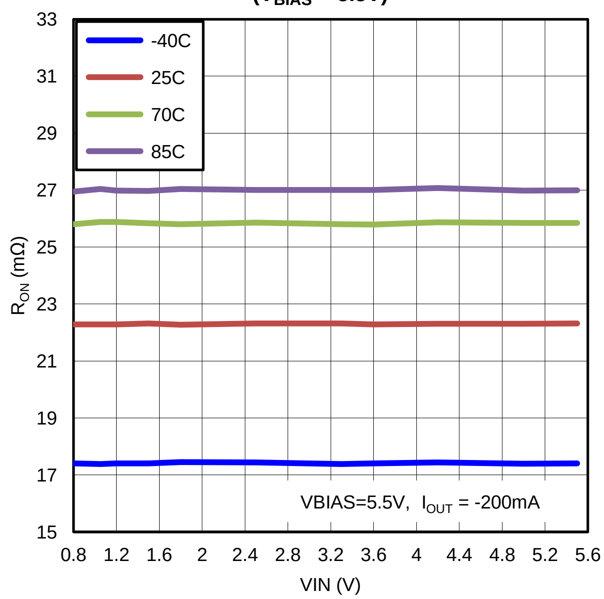
TEMPERATURE vs. R_{ON} (V_{BIAS} = 5.5V)



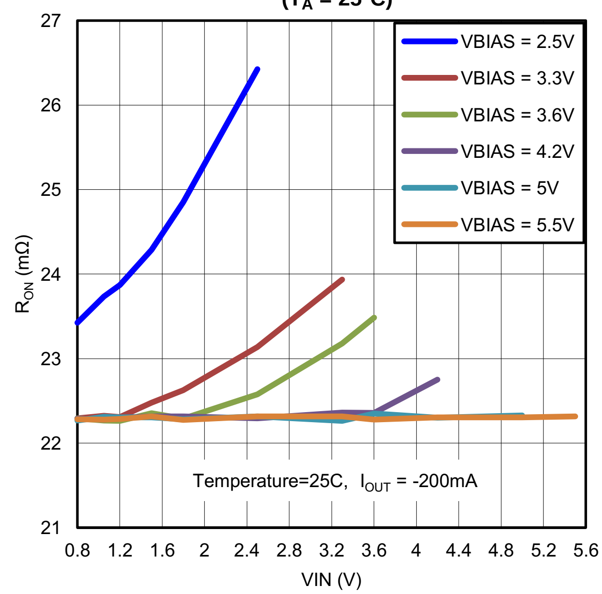
V_{IN} vs. R_{ON} (V_{BIAS} = 2.5V)



V_{IN} vs. R_{ON} (V_{BIAS} = 5.5V)

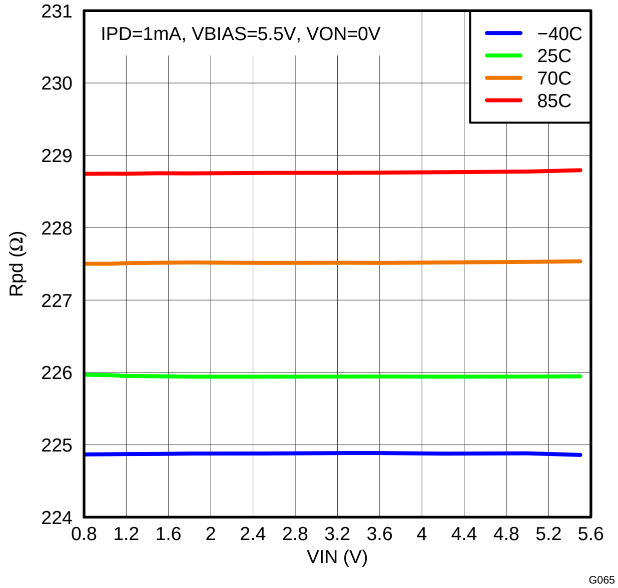


V_{IN} vs. R_{ON} (T_A = 25°C)

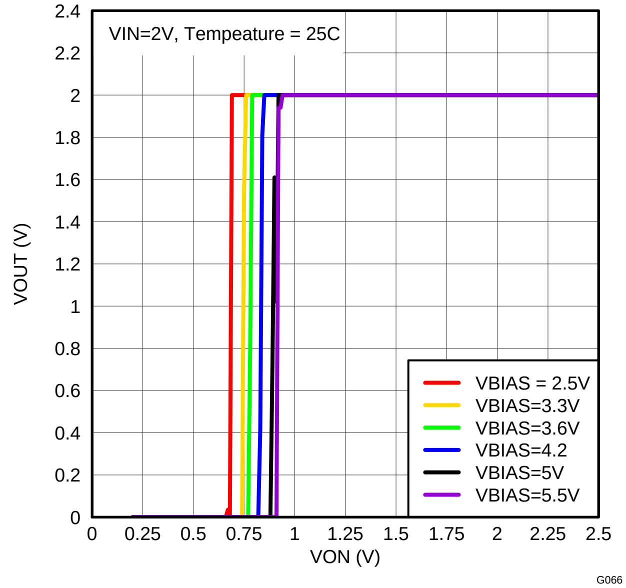


TYPICAL CHARACTERISTICS (continued)

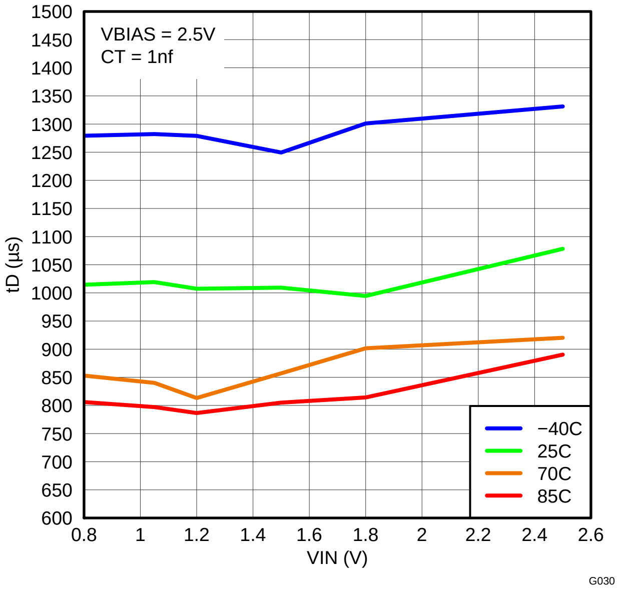
VIN vs. R_{PD} (V_{BIAS} = 5.5V)



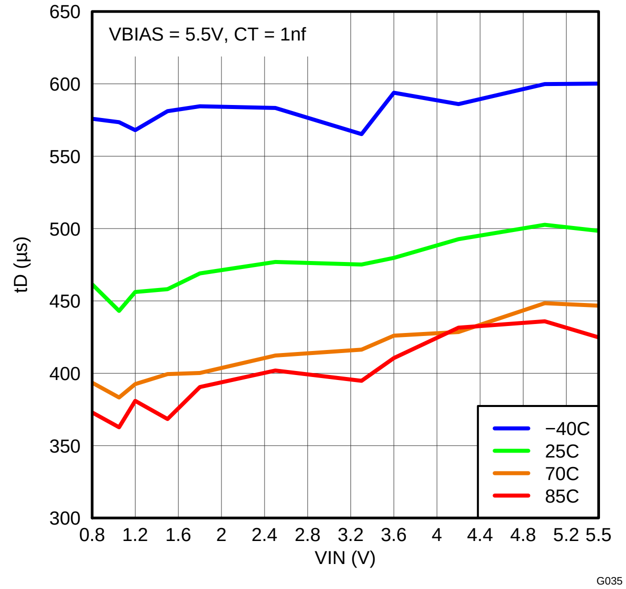
V_{ON} vs. V_{OUT} (T_A = 25°C)



V_{IN} vs. t_D (V_{BIAS} = 2.5V, CT = 1nF)

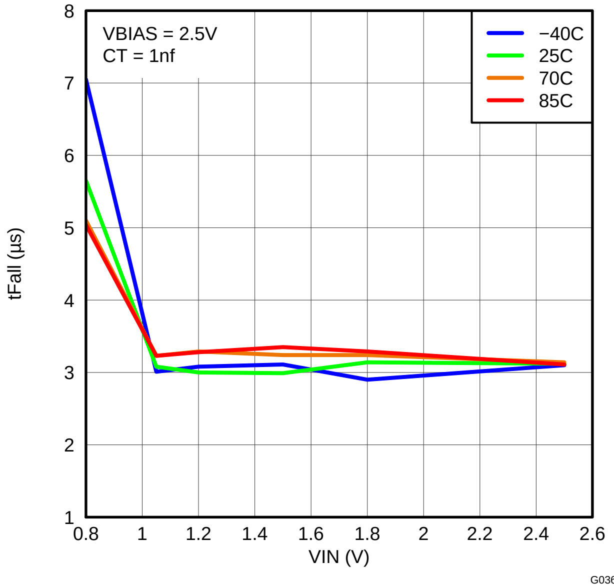


V_{IN} vs. t_D (V_{BIAS} = 5.5V, CT = 1nF)

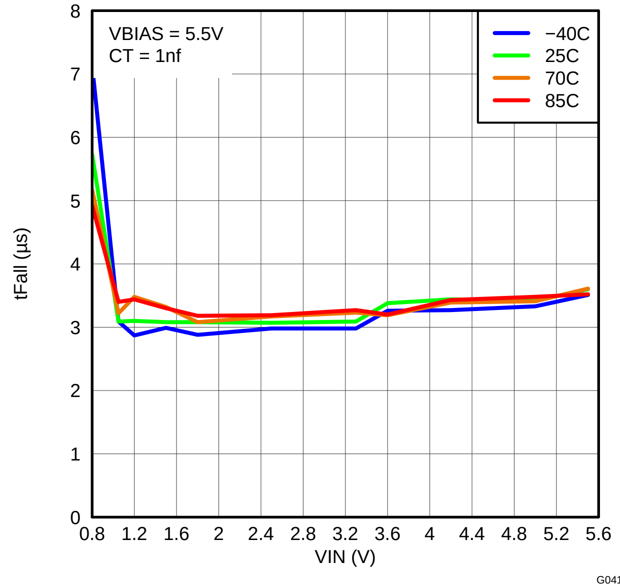


TYPICAL CHARACTERISTICS (continued)

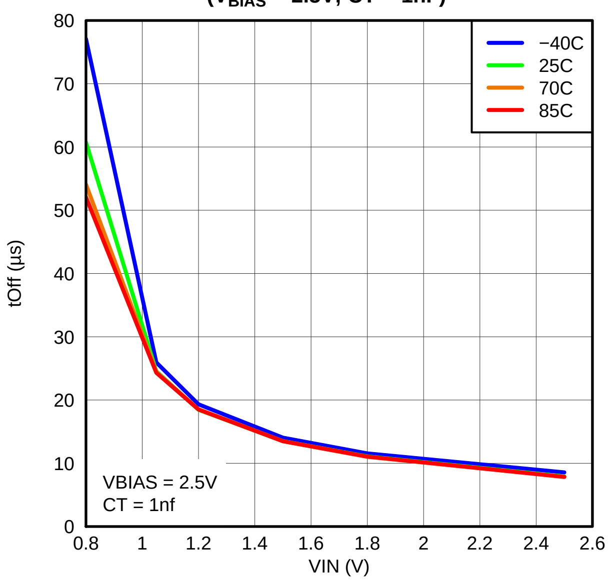
V_{IN} vs. t_F (V_{BIAS} = 2.5V, CT = 1nF)



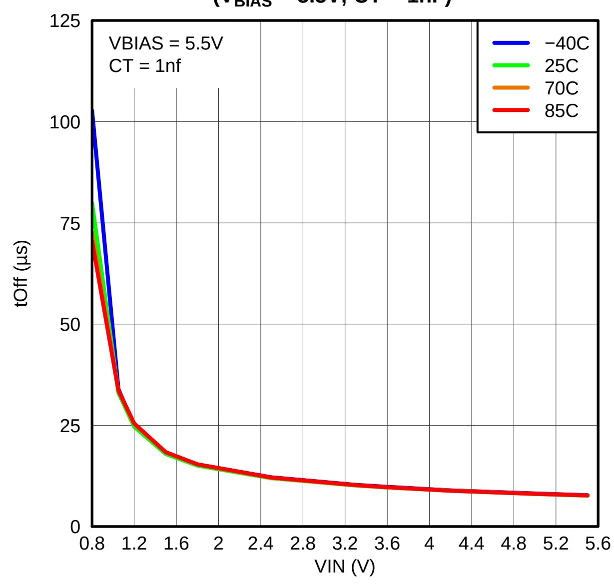
V_{IN} vs. t_F (V_{BIAS} = 5.5V, CT = 1nF)



V_{IN} vs. t_{OFF} (V_{BIAS} = 2.5V, CT = 1nF)

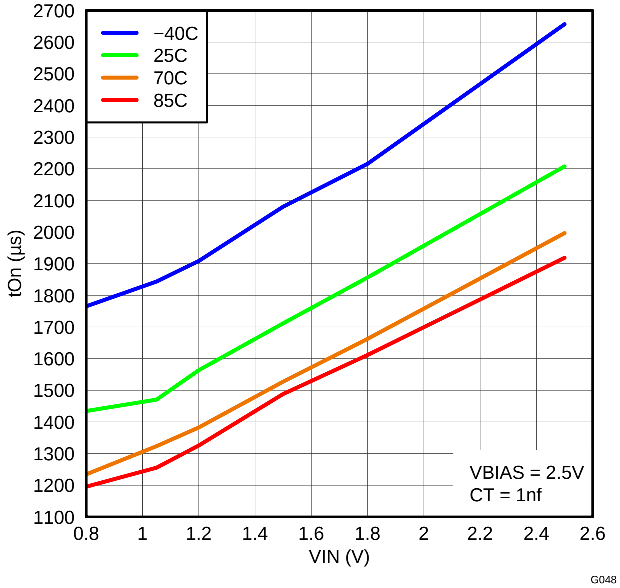


V_{IN} vs. t_{OFF} (V_{BIAS} = 5.5V, CT = 1nF)

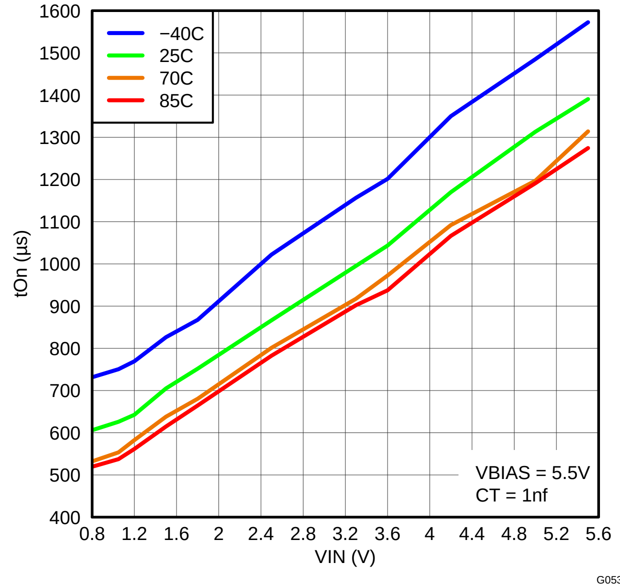


TYPICAL CHARACTERISTICS (continued)

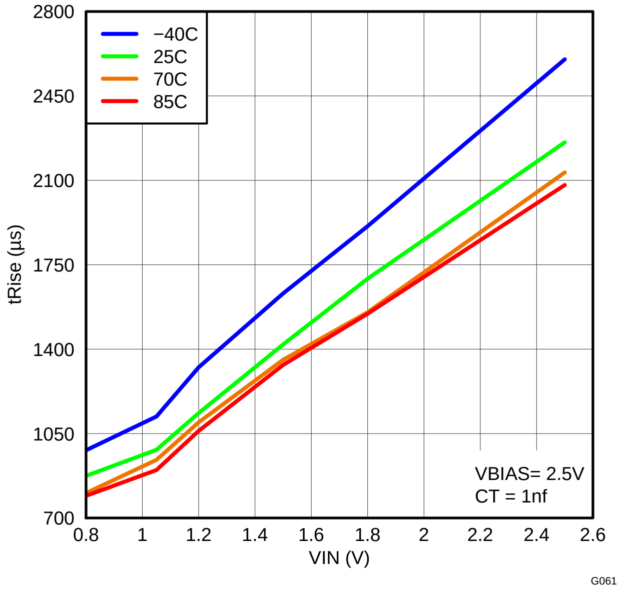
V_{IN} vs. t_{ON} (V_{BIAS} = 2.5V, CT = 1nF)



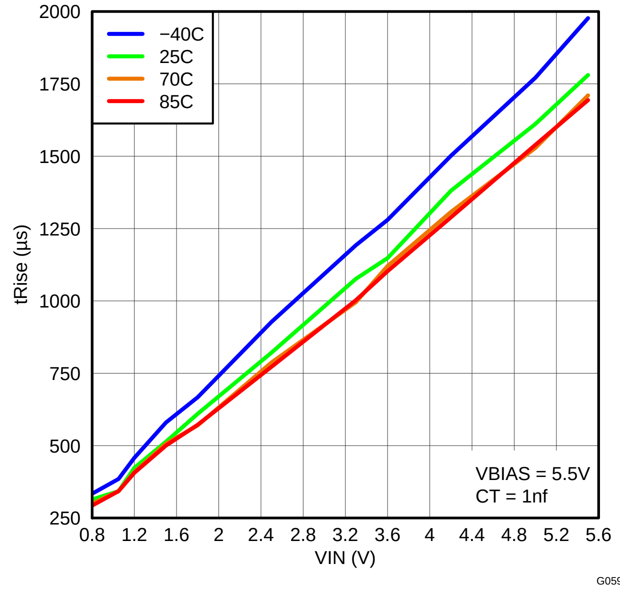
V_{IN} vs. t_{ON} (V_{BIAS} = 5.5V, CT = 1nF)



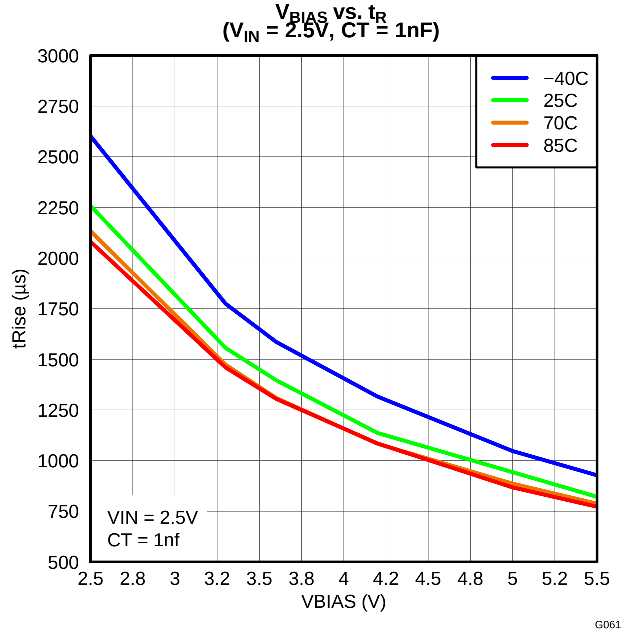
V_{IN} vs. t_R (V_{BIAS} = 2.5V, CT = 1nF)



V_{IN} vs. t_R (V_{BIAS} = 5.5V, CT = 1nF)

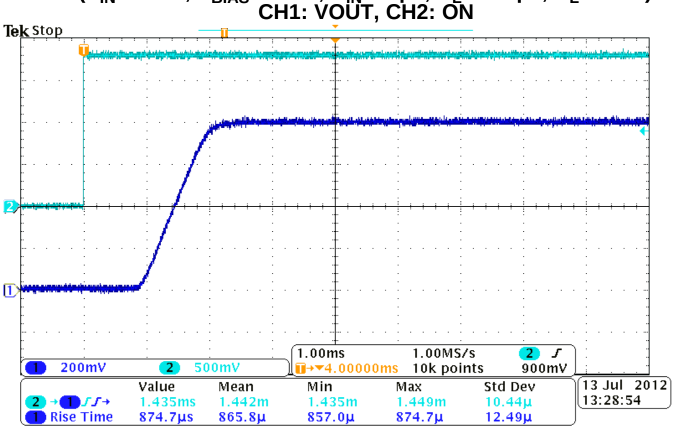


TYPICAL CHARACTERISTICS (continued)

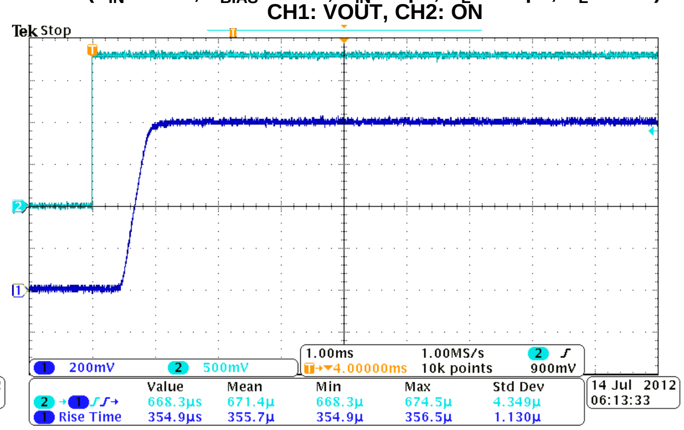


TYPICAL AC SCOPE CAPTURES at T_A = 25ºC, CT = 1nF

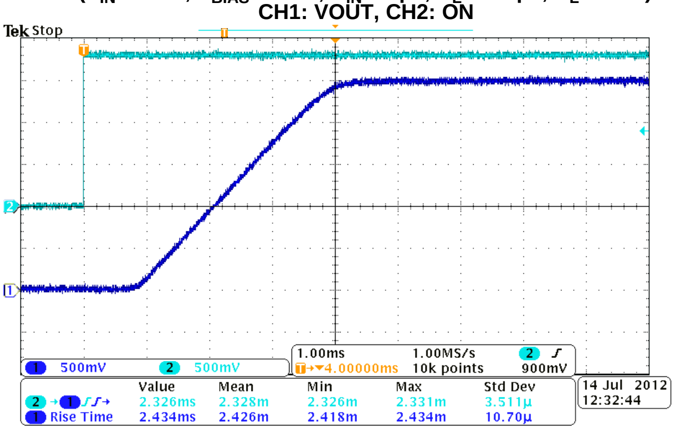
TURN-ON RESPONSE TIME
(V_{IN} = 0.8V, V_{BIAS} = 2.5V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON



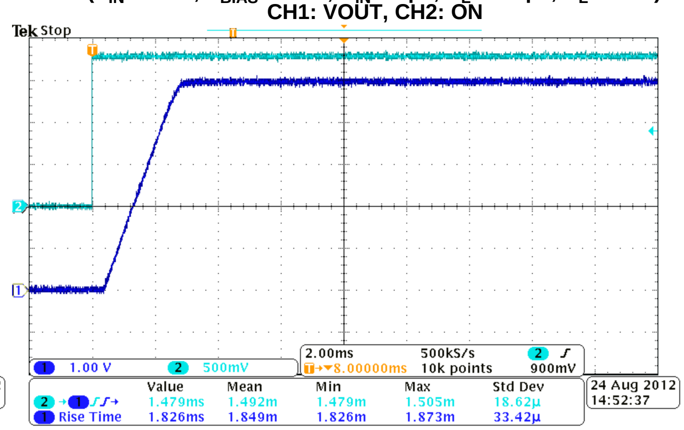
TURN-ON RESPONSE TIME
(V_{IN} = 0.8V, V_{BIAS} = 5.0V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON



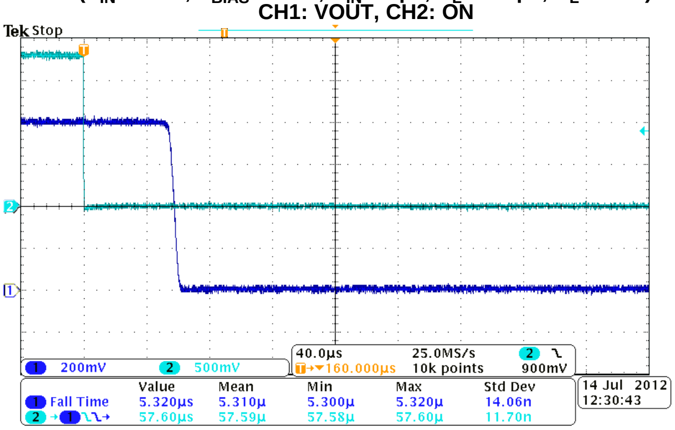
TURN-ON RESPONSE TIME
(V_{IN} = 2.5V, V_{BIAS} = 2.5V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON



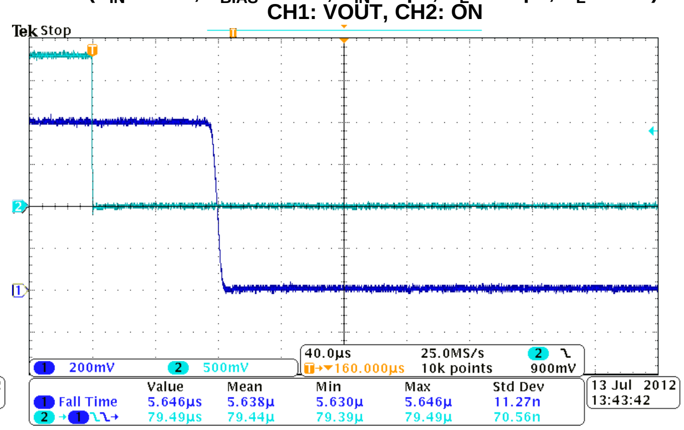
TURN-ON RESPONSE TIME
(V_{IN} = 5.0V, V_{BIAS} = 5.0V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON



TURN-OFF RESPONSE TIME
(V_{IN} = 0.8V, V_{BIAS} = 2.5V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON

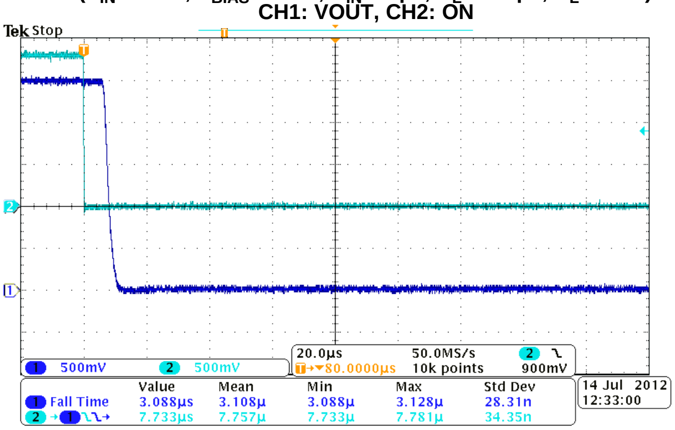


TURN-OFF RESPONSE TIME
(V_{IN} = 0.8V, V_{BIAS} = 5.0V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON

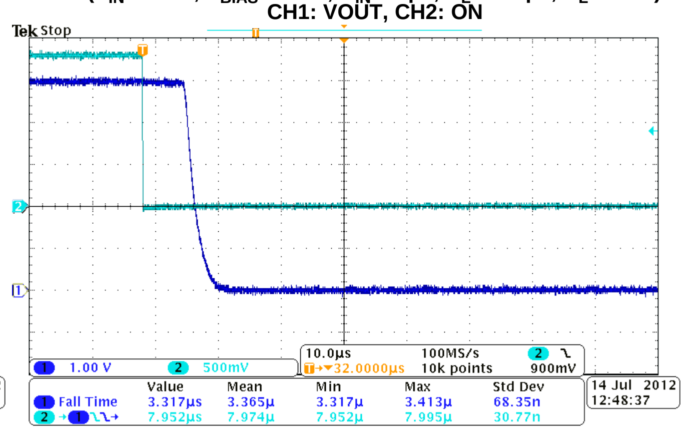


TYPICAL AC SCOPE CAPTURES at T_A = 25ºC, CT = 1nF (continued)

TURN-OFF RESPONSE TIME
(V_{IN} = 2.5V, V_{BIAS} = 2.5V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON



TURN-OFF RESPONSE TIME
(V_{IN} = 5.0V, V_{BIAS} = 5.0V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON



APPLICATION INFORMATION

ON/OFF CONTROL

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

INPUT CAPACITOR (OPTIONAL)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

OUTPUT CAPACITOR (OPTIONAL)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn-on due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see below).

V_{IN} and V_{BIAS} VOLTAGE RANGE

For optimal R_{ON} performance, make sure $V_{IN} \le V_{BIAS}$. The device will still be functional if $V_{IN} > V_{BIAS}$ but it will exhibit R_{ON} greater than what is listed in the ELECTRICAL CHARACTERISTICS table. See Figure 3 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Be sure to never exceed the maximum voltage rating for VIN and VBIAS.

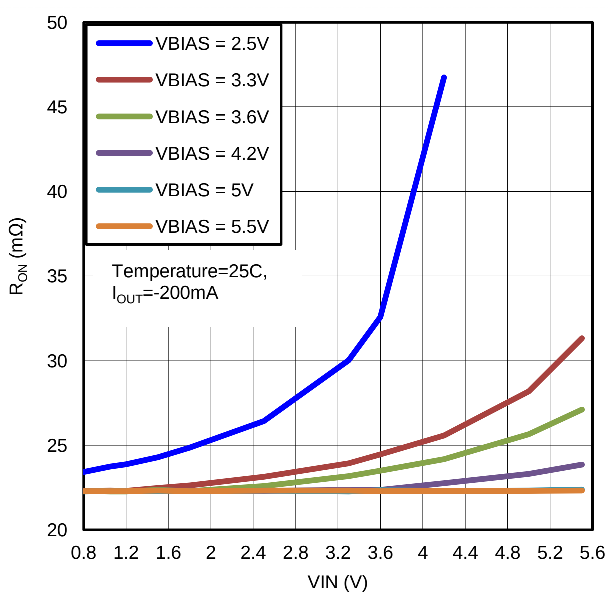


Figure 3. R_{ON} vs. V_{IN} ($V_{IN} > V_{BIAS}$)

ADJUSTABLE RISE TIME

A capacitor to GND on the CT pin sets the VOUT slew rate. The voltage on the CT pin can be as high as 12V. Therefore, the minimum voltage rating for the CT cap should be 25V for optimal performance. An approximate formula for the relationship between CT and slew rate is (the equation below accounts for 10% to 90% measurement on V_{OUT} and does **NOT** apply for CT = 0pF. Use table below to determine rise times for when CT = 0pF):

$$SR = 0.39 \times CT + 13.4 \tag{1}$$

Where,

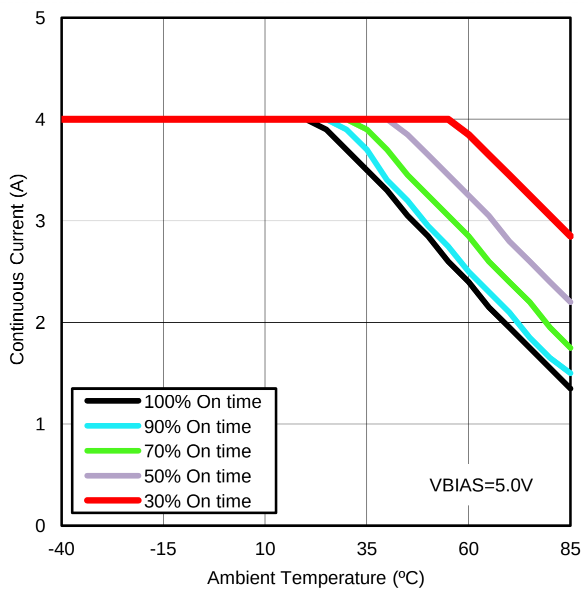
SR = slew rate (in µs/V)
CT = the capacitance value on the CT pin (in pF)
The units for the constant 13.4 is in µs/V. The units for the constant 0.39 are in µs/(V*pF).

Rise time can be calculated by multiplying the input voltage by the slew rate. The table below contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition, and the ON pin is asserted high.

CTx (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1µF, C_{IN} = 1µF, R_L = 10Ω TYPICAL VALUES at 25°C, 25V X7R 10% CERAMIC CAP						
	5V	**3.3V**	**1.8V**	**1.5V**	**1.2V**	**1.05V**	**0.8V**
0	127	93	62	55	51	46	42
220	475	314	188	162	141	125	103
470	939	637	359	304	255	218	188
1000	1869	1229	684	567	476	414	344
2200	4020	2614	1469	1211	1024	876	681
4700	8690	5746	3167	2703	2139	1877	1568
10000	18360	12550	6849	5836	4782	4089	3449

SAFE OPERATING AREA (SOA)

The SOA curves show the continuous current carrying capability of the device versus ambient temperature (T_A) to ensure reliable operation over 70,000 hours of device lifetime. The different curves represent the *percentage On time* over device lifetime and can be used as a reference to understand the current carrying capability of TPS22967 under different use cases. It is recommended to maintain continuous current at or below the SOA curves shown in Figure 4.



"On time" is the duration of time that the device is enabled (ON ≥ V_{IH}) over 70,000 hour lifetime.

Figure 4. Safe Operating Area

BOARD LAYOUT AND THERMAL CONSIDERATIONS

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

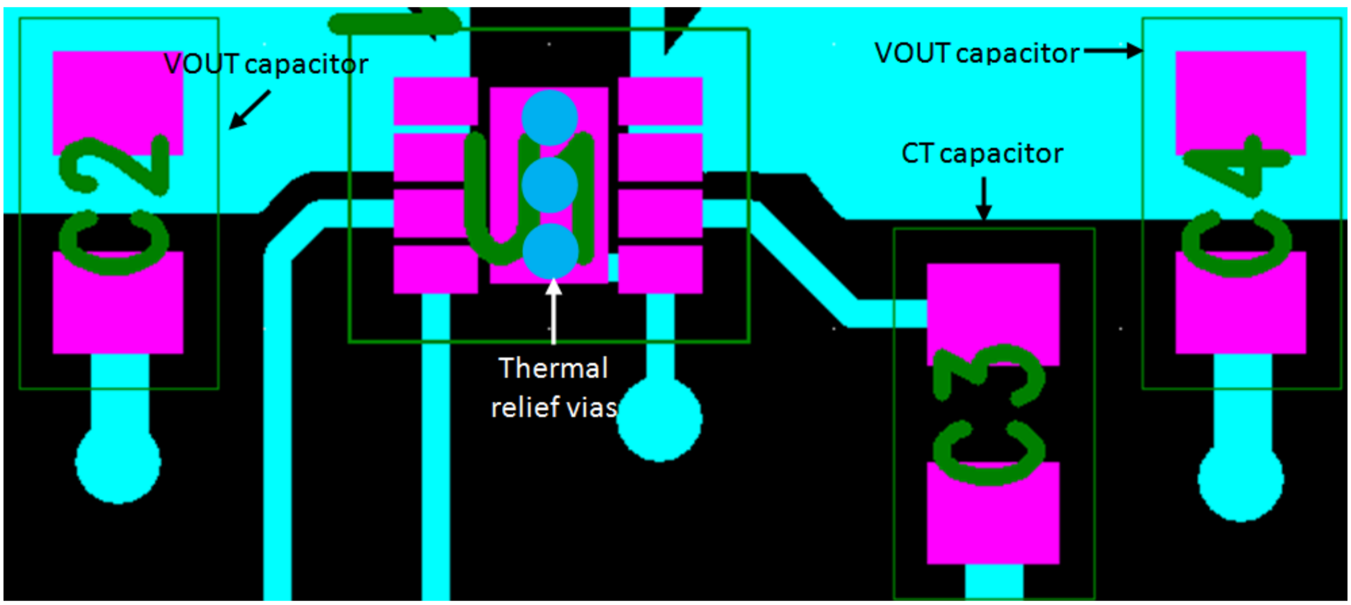
The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation as a guideline:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\Theta_{JA}} \tag{2}$$

Where:

$P_{D(max)}$ = maximum allowable power dissipation
$T_{J(max)}$ = maximum allowable junction temperature (125°C for the TPS22967)
T_A = ambient temperature of the device
Θ_{JA} = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

The figure below shows an example of a layout. Notice the thermal vias located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22967DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ZTU	Samples
TPS22967DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ZTU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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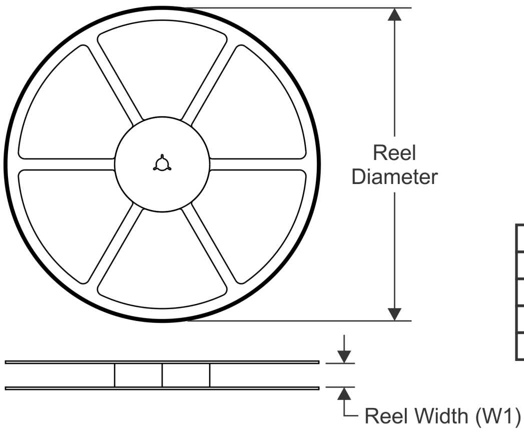
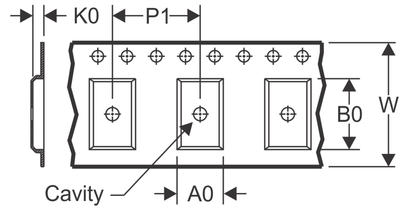
TAPE AND REEL INFORMATION

REEL DIMENSIONS

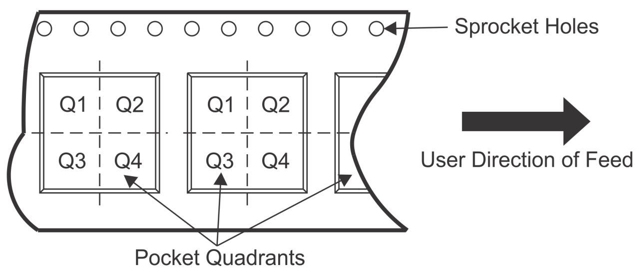


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

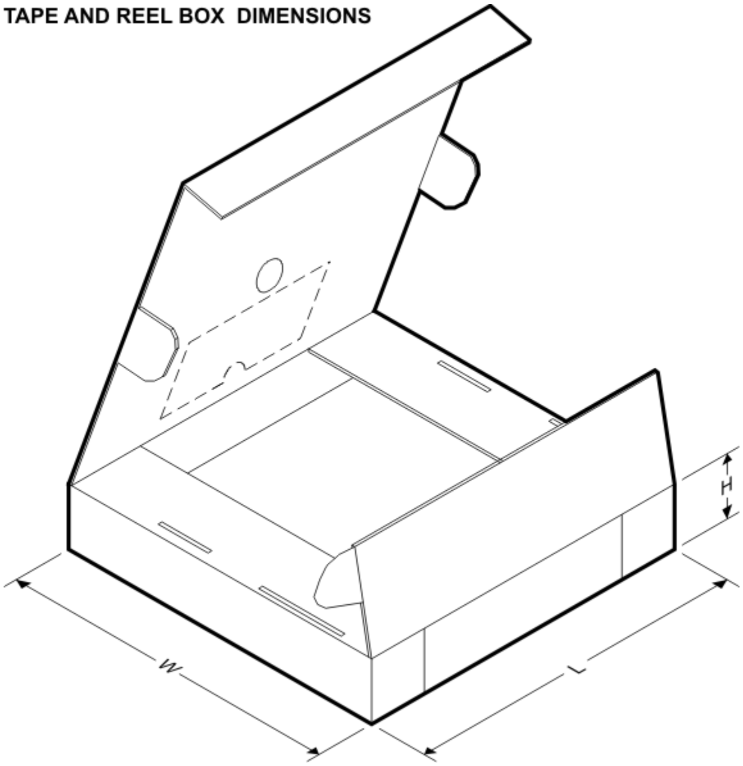
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22967DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22967DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

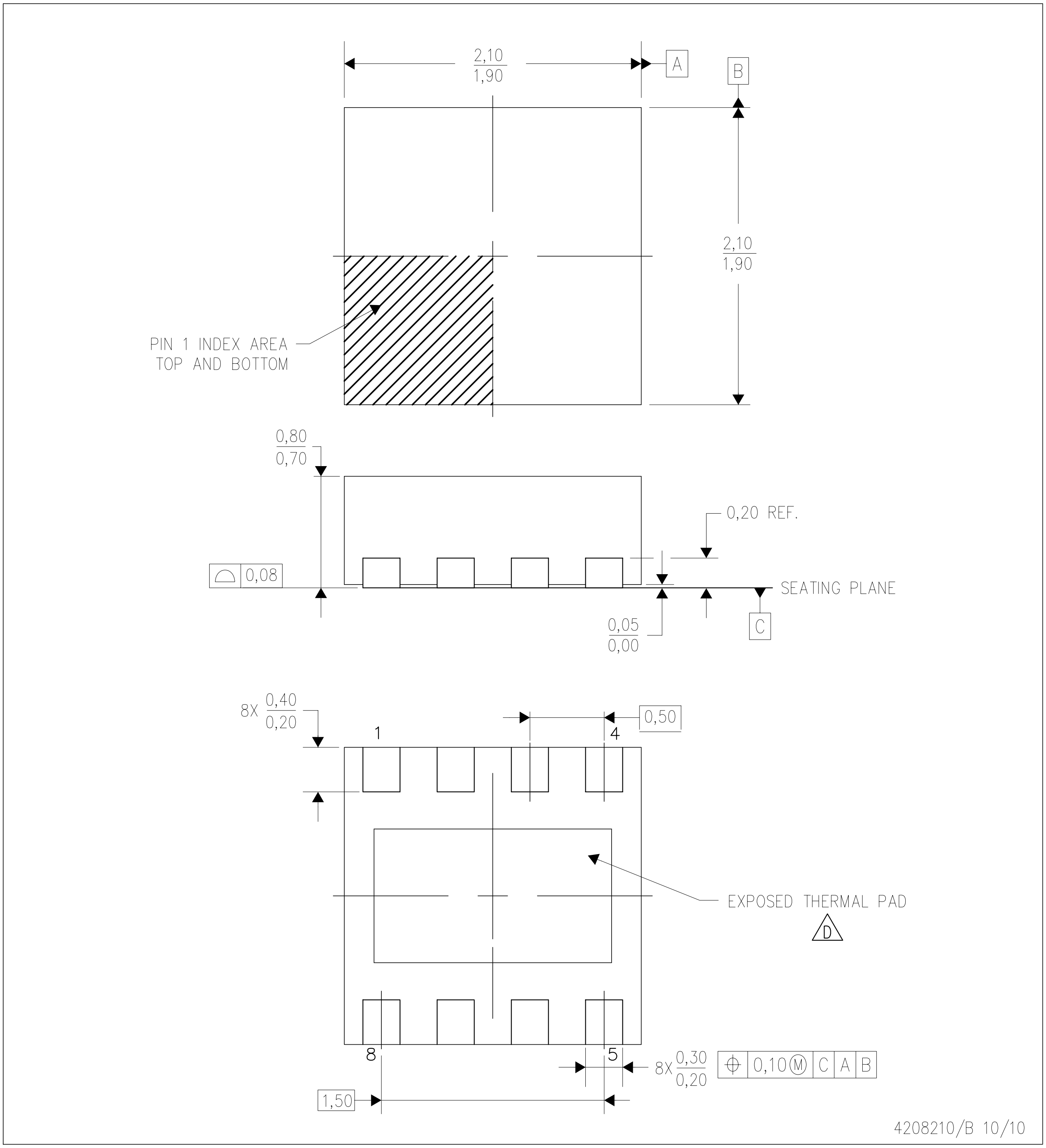
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22967DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22967DSGT	WSON	DSG	8	250	210.0	185.0	35.0

DSG (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–Leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO–229.

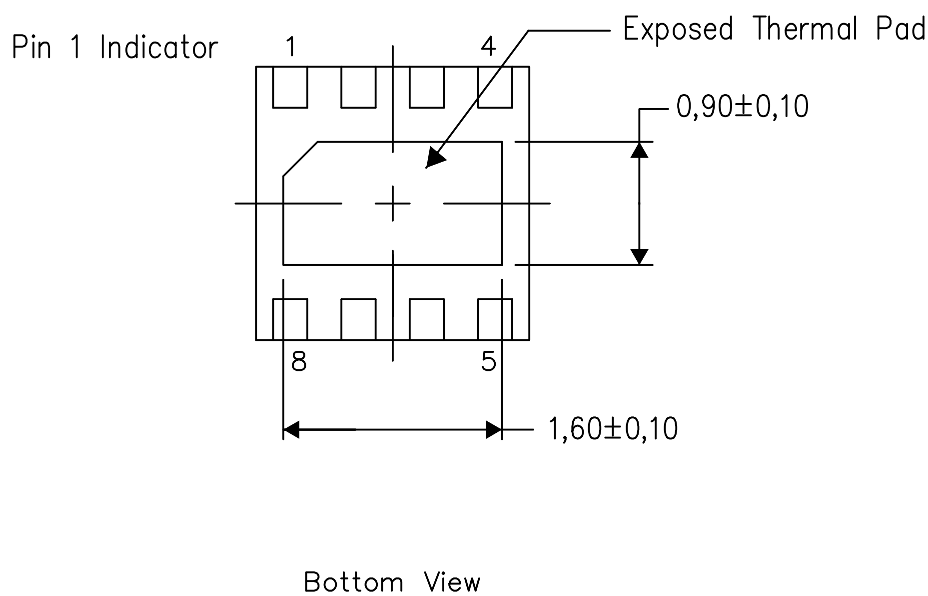
DSG (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

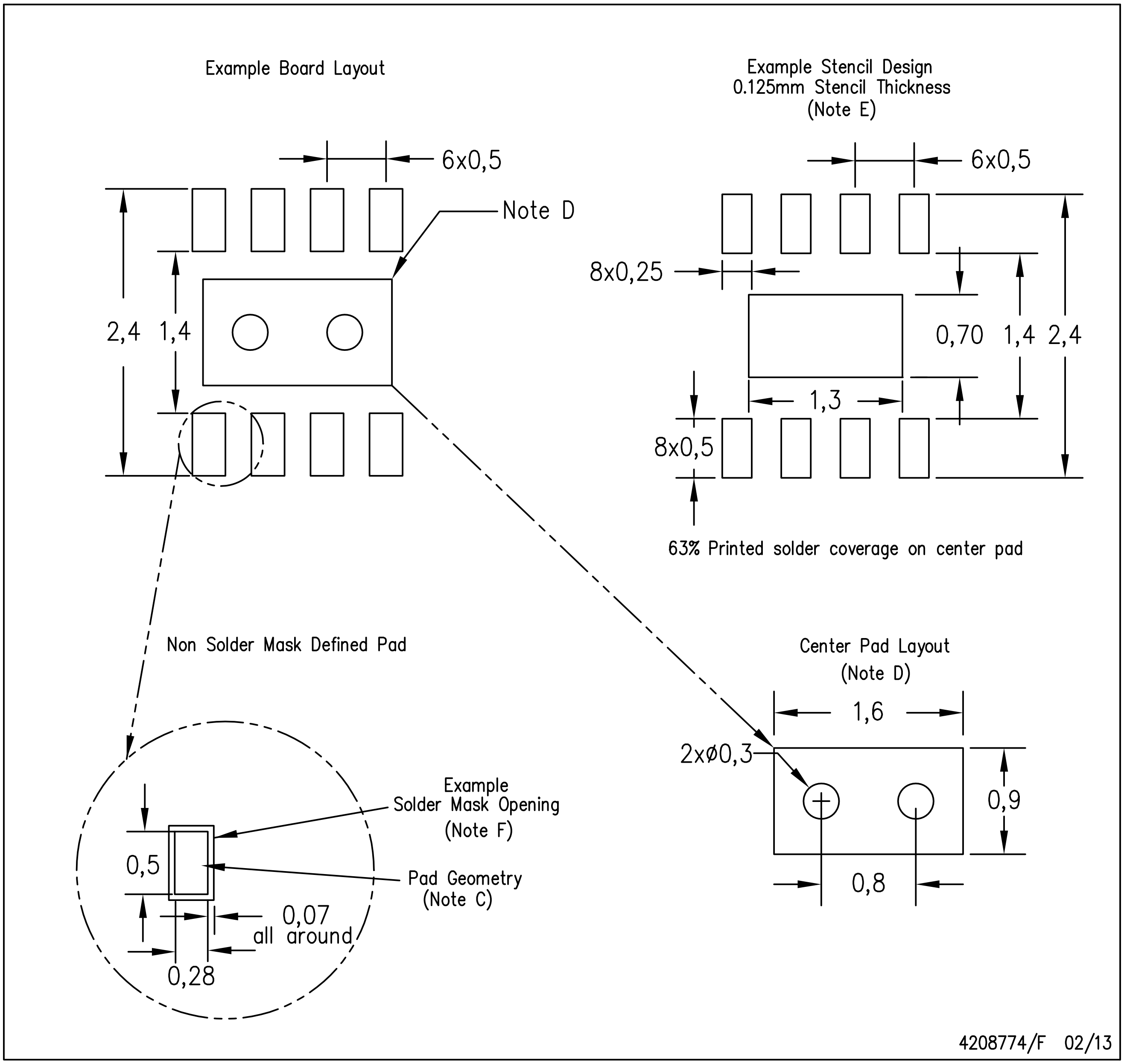


Exposed Thermal Pad Dimensions

4208347/G 08/13

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

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