Blackfin® A-V EZ-Extender® Manual

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Analog Devices, Inc.
One Technology Way
Norwood, Mass. 02062-9106

ANALOG DEVICES

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Regulatory Compliance

The Blackfin A-V EZ-Extender is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The Blackfin A-V EZ-Extender has been certified to comply with the essential requirements of the European EMC directive 2004/108/EC and therefore carries the **"CE" mark**.

The Blackfin A-V EZ-Extender has been appended to Analog Devices, Inc. EMC Technical File (EMC TF) referenced **DSPTOOLS1**, issue 2 dated June 4, 2008 and was declared CE compliant by an appointed Notified Body (No.0673) as listed below.

Notified Body Statement of Compliance: Z600ANA1.023 dated December 2, 2004.

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The Blackfin A-V EZ-Extender contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused extender boards in the protective shipping package.

CONTENTS

Contents

PREFACE

Thank you for purchasing the Blackfin® A-V EZ-Extender®, Analog Devices, Inc. daughter board to the EZ-KIT Lite® evaluation system for the ADSP-BF533, ADSP-BF537, and ADSP-BF561 Blackfin processors.

Blackfin processors are embedded processors that support a Media Instruction Set Computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing characteristics towards delivering signal processing performance in a microprocessor-like environment.

EZ-KIT Lites and A-V EZ-Extenders are designed to be used in conjunction with the CrossCore® Embedded Studio (CCES) and VisualDSP++® software development environments. The development environment facilitates advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and A-V EZ-Extender assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

To learn more about Analog Devices development software, go to http://www.analog.com/processors/tools.

Product Overview

The Blackfin A-V EZ-Extender is a separately sold daughter board that plugs onto the expansion interface of the ADSP-BF533, ADSP-BF537, or ADSP-BF561 EZ-KIT Lite evaluation system. The extender board aids the design and prototyping phases of the ADSP-BF533, ADSP-BF537, or ADSP-BF561 processor targeted applications.

The board extends the evaluation system capabilities by providing a connection to a video decoder; video encoder; multiple camera evaluation boards; flat panel display; and 3-stereo input channel, 2-stereo output channel audio codec.

Please visit www.analog.com/EX1-AV for additional information, including CCES support.

The board features:

- Analog audio interface
    - AD1836A Analog Devices 96 kHz audio codec
    - Five 3.5 mm audio jacks, stacked in one connector
- Analog video interface
    - ADV7183B video decoder with three input RCA phono jacks
    - ADV7179 video encoder with three output RCA phono jacks
- OmniVision camera module interface
    - Connection to OmniVision camera evaluation modules; for example, OV6630AA (this part is no longer available)
    - 32-pin, right-angle, 0.1 in. spacing, female socket

- Micron camera module interface
    - Connection to Micron camera evaluation modules; for example, MT9V022 (this part is no longer available)
    - 26-pin, right-angle, 0.1 in. spacing, female socket
- Kodak camera module interface
    - Connection to Kodak camera evaluation modules; for example, KAC-9628 (this part is no longer available)
    - 28-pin, right- angle, 0.1 in. spacing, female socket
- Flat panel display interface (FPDI)
    - Connection to flat panel displays; for example, NL6448BC20-08E
    - DF9B-31S-1V connector

Before using any of the interfaces, follow the procedure in "A-V EZ-Extender Interfaces" on page 1-1.

Example programs are available to demonstrate the Blackfin A-V EZ-Extender capabilities.

Purpose of This Manual

The *Blackfin A-V EZ-Extender Manual* provides instructions for installing the product hardware (board). The text describes operation and configuration of the board components and provides guidelines for running your own code on the A-V EZ-Extender. Finally, a schematic and a bill of materials are provided for reference.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set.

Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts that describe your target architecture. For the locations of these documents, see "Related Documents".

Programmers who are unfamiliar with CCES or VisualDSP++ should refer to the online help and user's manuals.

Manual Contents

The manual consists of:

- Chapter 1, "A-V EZ-Extender Interfaces" on page 1-1
  Provides basic board information.
- Chapter 2, "A-V EZ-Extender Hardware Reference" on page 2-1
  Provides information on the hardware aspects of the board.
- Appendix A, "A-V EZ-Extender Bill of Materials" on page A-1
  Provides a list of components used to manufacture the board.
- Appendix B, "A-V EZ-Extender Schematic" on page B-1
  Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design. Appendix B is part of the online help.

What's New in This Manual

This is revision 2.1 of the *Blackfin A-V EZ-Extender Manual*. The manual has been updated to include CCES information. In addition, modifications and corrections based on errata reports against the previous manual revision have been made.

For the latest version of this manual, please refer to the Analog Devices Web site.

Technical Support

You can reach Analog Devices processors and DSP technical support in the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:
  `http://ez.analog.com/community/dsp`
- Submit your questions to technical support directly at:
  `http://www.analog.com/support`
- E-mail your questions about processors, DSPs, and tools development software from **CrossCore Embedded Studio** or **VisualDSP++**:

  Choose **Help > Email Support**. This creates an e-mail to `processor.tools.support@analog.com` and automatically attaches your **CrossCore Embedded Studio** or **VisualDSP++** version information and `license.dat` file.
- E-mail your questions about processors and processor applications to:
  `processor.support@analog.com` or
  `processor.china@analog.com` (Greater China support)

- In the **USA only**, call **1-800-ANALOGD** (1-800-262-5643)
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- Send questions by mail to:
  Processors and DSP Technical Support
  Analog Devices, Inc.
  Three Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

This extender board supports Analog Devices ADSP-BF533, ADSP-BF537, and ADSP-BF561 Blackfin embedded processors.

Product Information

Product information can be obtained from the Analog Devices Web site and the online help.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a

link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, MyAnalog is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. MyAnalog provides access to books, application notes, data sheets, code examples, and more.

Visit MyAnalog to sign up. If you are a registered user, just log on. Your user name is your e-mail address.

EngineerZone

EngineerZone is a technical support forum from Analog Devices. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

Related Documents

For additional information about the product, refer to the following publications.

Table 1. Related Processor Publications

Title	Description
• *ADSP-BF531/ADSP-BF532/ADSP-BF533 Blackfin Embedded Processor Data Sheet* • *ADSP-BF534/ADSP-BF536/ADSP-BF537 Blackfin Embedded Processor Data Sheet* • *ADSP-BF561 Blackfin Embedded Symmetric Multiprocessor Data Sheet*	General functional description, pinout, and timing of the processor
• *ADSP-BF533 Blackfin Processor Hardware Reference* • *ADSP-BF537 Blackfin Processor Hardware Reference* • *ADSP-BF561 Blackfin Processor Hardware Reference*	Description of the internal processor architecture and all register functions
Blackfin Processor Programming Reference	Description of all allowed processor assembly instructions

1 A-V EZ-EXTENDER INTERFACES

This chapter provides a setup procedure for the Blackfin A-V EZ-Extender and EZ-KIT Lite (ADSP-BF533, ADSP-BF537, or ADSP-BF561). The chapter also describes each evaluation interface the extender supports.

The information is presented in the following order.

A-V EZ-Extender Setup

It is very important to set up all components of the system containing the Blackfin A-V EZ-Extender, then apply power to the system.

Power your system after these steps are completed:

1. Read the applicable design interface section in this chapter—the text provides an overview of the interface capabilities.
2. Read "System Architecture" on page 2-2 to understand the physical connections of the extender board. For more detailed information, refer to "A-V EZ-Extender Schematic" on page B-1.
3. Set the jumpers on the extender board. Use the block diagram in Figure 2-1 on page 2-3 in conjunction with "Jumpers" on page 2-7.
4. Set the switches and jumpers on the EZ-KIT Lite board. If not already, familiarize yourself with the documentation and schematic drawing of the EZ-KIT Lite (see "Related Documents"). Compare the expansion interface signals of the extender with the EZ-KIT Lite signals to ensure there is no contention. For example, it may be necessary to disable other devices connected to the parallel peripheral interface (PPI) of the processor, change the routing of the PPI clocks, and disable the push buttons.
5. Configure any other interfacing boards; for example, another EZ-Extender or a camera evaluation board.

Analog Audio Interface

The Blackfin A-V EZ-Extender supports audio applications with the on-board AD1836A multichannel 96 kHz audio codec. The AD1836A codec is a high-performance single-chip device that provides three stereo digital-to-analog converters (outputs) and two stereo analog-to-digital converters (inputs), using Analog Devices patented multibit sigma-delta architecture. The board includes a serial peripheral interface (SPI) port, enabling the processor to adjust volume and other parameters. For a general overview of the audio interface connections, see Figure 2-1 on page 2-3; for details, see "A-V EZ-Extender Schematic" on page B-1.

SPORT0 of the expansion interface connects to the serial port of the AD1836A codec. The processor is capable of transferring data to the audio codec in time-division multiplexed (TDM) mode or I^2S mode. In I^2S mode, the codec can operate at a 96 kHz sample rate and allows two channels of output. In TDM mode, the codec can operate at a maximum of 48 kHz sample rate and allows simultaneous use of all input and output channels. To operate in I^2S mode, install the JP7.1/2 jumper. For more information, see "I2S Enable Jumper (JP7.1/2)" on page 2-13.

Internal registers of the AD1836A audio codec can be programmed via the SPI port of the processor. (For information on how to program the configuration registers, refer to the AD1836A data sheet.) The AD1836A codec reset comes from a flag pin located at PPI1_D11 of the expansion interface or from the reset signal on the EZ-KIT Lite. For information on how to configure the reset, see "AV_RESET Source Jumper (JP9.1/3/5)" on page 2-14.

Before using the interface, follow the procedure in "A-V EZ-Extender Setup" on page 1-2.

For more information about the codec, go to www.analog.com/AD1836A.

Analog Video Interface

The Blackfin A-V EZ-Extender supports video input and output applications with an on-board video encoder and decoder. The ADV7179 video encoder provides up to three output channels of analog video, while the ADV7183B video decoder provides up to three input channels of analog video. Both the encoder and decoder connect to PPI0 of the expansion interface, while the encoder also can connect to PPI1 (if the processor has two PPI ports). For a general overview of the analog video interface connectors, see Figure 2-1 on page 2-3; for details, see "AV_RESET Source Jumper (JP9.1/3/5)" on page 2-14.

To use ADV7179 and ADV7183B, set up all of the jumpers related to the PPI data signals, frame sync signals, and clock signal. To program the internal register of video devices, configure the 2-wire interface signals (see "TWI Source Selection Jumpers (JP3.3/5/7, JP3.4/6/8)" on page 2-8). Finally, determine the source of encoder or decoder reset, as described in "AV_RESET Source Jumper (JP9.1/3/5)" on page 2-14.

Before using the interface, follow the procedure in "A-V EZ-Extender Setup" on page 1-2.

For more information about ADV7179 and ADV7183B, go to www.analog.com/ADV7179 and www.analog.com/ADV7183B.

Camera Module Interfaces

The Blackfin A-V EZ-Extender has three right-angle connectors (J4, J6, and P4) with control signals necessary to interface with three camera evaluation modules from different manufactures. For a general overview of the camera interface connections, see Figure 2-1 on page 2-3; for details, see "A-V EZ-Extender Schematic" on page B-1. Figure 1-1 shows the orientation of the camera modules as each camera connects to the board.

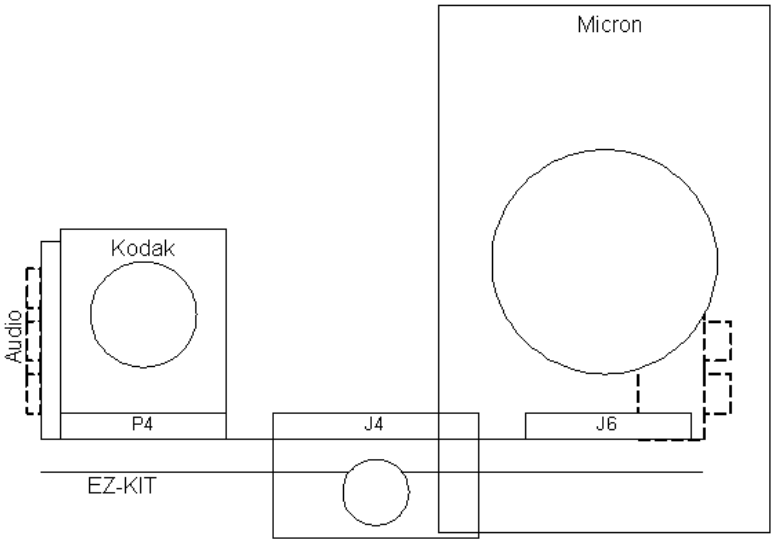

Figure 1-1. Camera Orientation

J6 is a connector designated for a Micron camera sensor evaluation module. The interface has been tested with the Micron MT9V022 camera. For information about Micron camera sensors and evaluation boards, go to http://www.micron.com.

J4 is a connector designated for an OmniVision camera sensor evaluation module. The interface has been tested with the OmniVision OV6630AA camera. For information about OmniVision camera sensors and evaluation boards, go to http://www.ovt.com.

P4 is a connector designated for a Kodak camera sensor evaluation module. The interface has been tested with the Kodak KAC-9628 camera. For information about Kodak camera sensors and evaluation boards, go to http://www.kodak.com.

To connect the Blackfin A-V EZ-Extender to a camera module, first determine the source of the PPI clock. To learn about possible clock settings, refer to "PPI Clock Setup Jumpers (JP4.1/2, JP4.3/4, JP4.5/6,

JP4.7/8)" on page 2-11. Then set the direction of the data and frame sync signals, which depend on the camera's configuration. The data must be set as input to the PPI port; refer to "System Architecture" on page 2-2 and "Jumpers" on page 2-7 for details.

Before using the camera interfaces, follow the procedure in "A-V EZ-Extender Setup" on page 1-2.

Flat Panel Display Interface

The flat panel display interface (FPDI) consists of a 31-pin DB9 connector linked to the PPI port and frame sync signals of the processor. For a general overview of the display interface connections, see Figure 2-1 on page 2-3; for details, see the "A-V EZ-Extender Schematic" on page B-1.

A timing and functional analysis is required to determine whether a specific LCD module can connect to the Blackfin A-V EZ-Extender. An example of display that can connect to the extender is the NEC NL6448BC20-08 display.

The power for the backlight feature of the LCD module must be provided by the customer (use the backlight inverter recommended by the manufacturer). In addition, it is necessary to purchase a cable to connect the Blackfin A-V EZ-Extender to the display; for example, FDC31/xxxxAFF03 from Axon Cable (`www.axon-cable.com`, part number `FDC31/xxxxAFF03`). Different length cables are available.

Before using the interface, follow the procedure in "A-V EZ-Extender Setup" on page 1-2.

Example Programs

Example programs are provided with the A-V EZ-Extender EZ-KIT Lite to demonstrate various capabilities of the product. The programs are included in the product installation kit and can be found in the `Examples` folder of the installation. Refer to a readme file provided with each example for more information.

CCES users are encouraged to use the example browser to find examples included with the EZ-KIT Lite Board Support Package.

2 A-V EZ-EXTENDER HARDWARE REFERENCE

This chapter describes the hardware design of the Blackfin A-V EZ-Extender.

The following topics are covered.

- "System Architecture" on page 2-2
  Describes the extender board configuration and explains how the board components interface with the processor and EZ-KIT Lite.
- "Jumpers" on page 2-7
  Describes the configuration jumpers.

System Architecture

A block diagram of the Blackfin A-V EZ-Extender is shown in Figure 2-1.

Not shown in the diagram is the analog audio interface, which is a simple connection between the serial port of the processor and AD1836A audio codec. The audio interface connects directly to SPORT0 of the expansion interface.

In Figure 2-1, unidirectional buffers are show as triangle symbols, while bidirectional buffers are shown as two overlapping triangles. For both types of buffers, an output-enable signal comes out of the top and is active LOW. For bidirectional buffers, a second signal for the direction is shown. When this net is pulled HIGH, the buffer is driving in the direction of the arrow in the center; when LOW, the buffer is driving in the opposite direction.

Before applying power to the system, follow the procedure in "A-V EZ-Extender Setup" on page 1-2.

The video interface can be split into two main signal sets: VID_IN and VID_OUT. Both signal sets consist of a 16-bit data bus, two frame sync signals, and a data clock. VID_IN connects to the video decoder and all camera interfaces. VID_IN connects only to the PPI0 of the EZ-KIT Lite. VID_OUT connects to the video encoder and flat panel display interface. On the expansion interface, VID_OUT connects to either PPI0 or PPI1 of the EZ-KIT Lite.

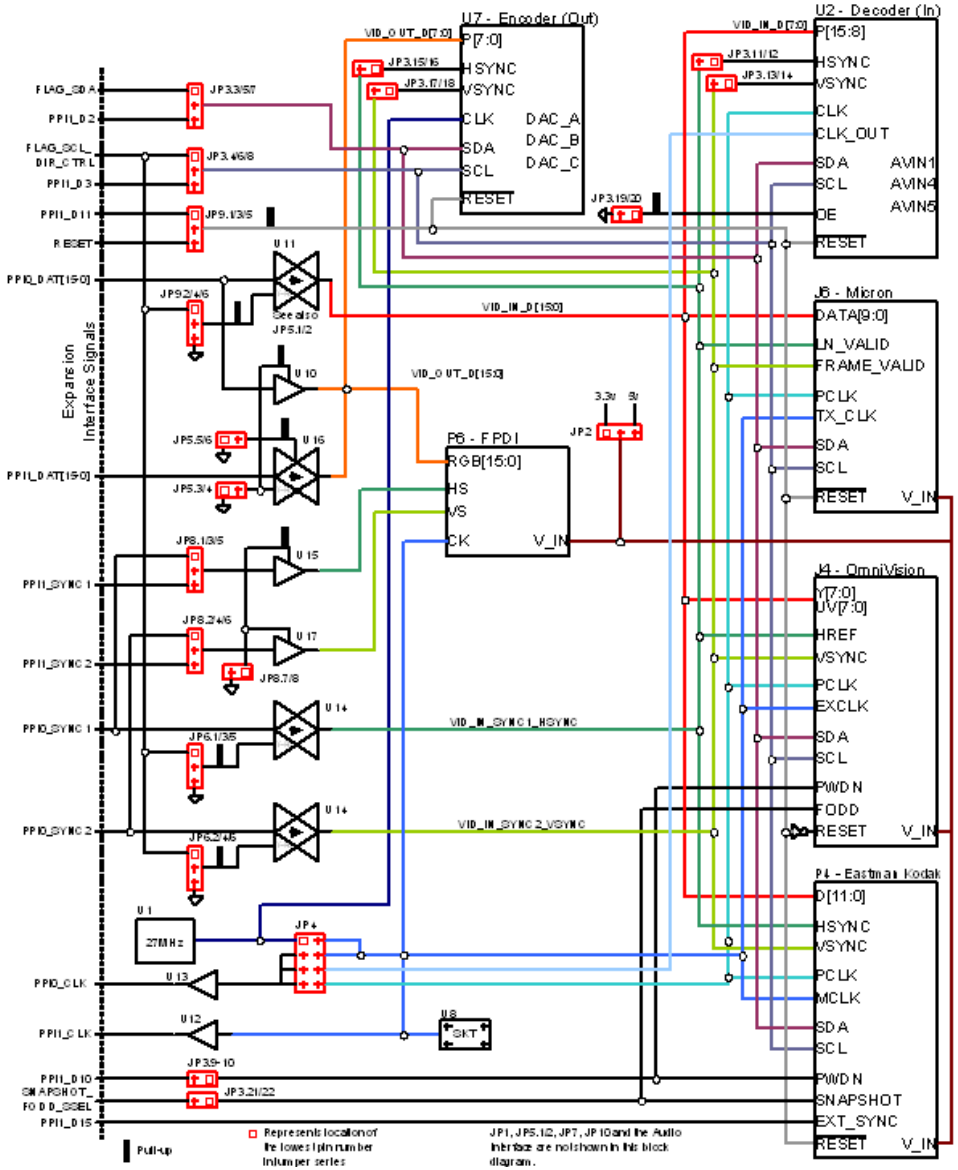

Figure 2-1. A-V EZ-Extender Block Diagram

Table 2-1 summarizes the signals coming and going on the expansion interface connectors.

Table 2-1. Signals of Expansion Interface Connectors

Net/Bus Name (Direction)	Blackfin A-V EZ-Extender Function	Relevant Configuration Jumpers
PPI0_D[0:15] (Bi)	Connects the processor's PPI0 data pins to the VID_IN_D[0:15] or VID_OUT_D[0:15] buses, depending on the jumper settings. This allows PPI0 to interface with all video interfaces on the board. The bus can be bidirectional, where the direction is fixed with a jumper or controlled by a flag pin.	JP5.3/4, JP9.2/4/6
PPI0_CLK (Output)	The clock related to the data on PPI0. This can come from an on-board oscillator, one of the video interfaces, or a socket that allows a user-supplied oscillator.	JP4.1/2, JP4.3/4, JP4.5/6, JP4.7/8
PPI0_SYNC1 (Bi)	The frame sync signal going to the processor's PPI0_SYNC1 pin. The signal behaves as HSYNC or HREF for the video interfaces. The signal also can be used to drive the FPDI's HS signal. The signal can be bidirectional, where the direction is fixed with a jumper or controlled by a flag pin.	JP6.1/3/5, JP8.1/3/5, JP8.7/8
PPI0_SYNC2 (Bi)	The frame sync signal going to the processor's PPI0_SYNC2 pin. The signal behaves as VSYNC or VREF for the video interfaces. In addition, the signal can drive the FPDI's VS signal. The signal can be bidirectional, where the direction is fixed with a jumper or controlled by a flag pin.	JP6.2/4/6, JP8.2/4/6, JP8.7/8
PPI1_D[0:15] (Bi)	Connects the processor's PPI1 data pins to the VID_OUT_D[0:15] bus. The VID_OUT_D[0:15] bus interfaces with the output video interfaces (FPDI and video encoder). The bus can be bidirectional but intended to be an input. Changing the direction is necessary only for test purposes and allows PPI0 to loop-back to PPI1. Note: D2, D3, and D10 of the bus have other functions (follows).	JP5.3/4, JP5.5/6, JP3.9/10, JP3.3/5/7 JP3.4/6/8

Table 2-1. Signals of Expansion Interface Connectors (Cont'd)

Net/Bus Name (Direction)	Blackfin A-V EZ-Extender Function	Relevant Configuration Jumpers
PPI1_D10 (Bi)	The multifunction net that typically functions as the D10 pin of PPI1 but, with a jumper, also can connect to the PDWN input of the OmniVision and Kodak camera interfaces.	JP3.9/10, JP5.3/4, JP5.5/6
PPI1_D2 (Bi)	The multifunction net typically functions as the D2 pin of PPI1 but also can function as the data signal for the processor's 2-wire interface (TWI). Used to program the internal configuration registers of most video interfaces.	JP3.3/5/7, JP5.3/4, JP5.5/6
PPI1_D3 (Bi)	The multifunction net typically functions as the D2 pin of PPI1 but also can function as the data signal for the processor's TWI. Used to program the internal configuration registers of most video interfaces.	JP3.4/6/8, JP5.3/4, JP5.5/6
FLAG_SDA (Bi)	In systems whose processor does not have a TWI, the signal connects to one of the processor's flag pins to emulate the TWI data pin and configure the internal registers of most video interfaces.	JP3.3/5/7
FLAG_SCL_DIR_CTRL (Input)	In systems whose processor does not have a TWI, the signal connects to one of the processor's flag pins to emulate the TWI clock signal and configure the internal registers of most video interfaces.	JP3.4/6/8
PPI1_CLK (Output)	The clock driving the EZ-KIT Lite's PPI1 clock input. The source of this clock can be PPI0_CLK, the on-board 27 MHz oscillator, or a socket accepting oscillators of other frequencies.	JP4.1/2, JP4.3/4, JP4.5/6, JP4.7/8
PPI1_FS1 (Input)	The signal driven to the HS signal of the FPDI. The output going to the FPDI can be disabled by a jumper.	JP8.1/3/5, JP8.7/8
PPI1_FS2 (Input)	The signal driven to the VS signal of the FPDI. The output going to the FPDI can be disabled by a jumper.	JP8.2/4/6, JP8.7/8
SNAPSHOT_FODD_SSEL (Bi)	The audio codec's SPI slave select signal; also can connect to the SNAPSHOT input of the Kodak interface or the FODD output of the OmniVision interface.	JP3.21/22
SCK (Input)	The SPI serial clock used to program the control register of the AD1836A audio codec.	

Table 2-1. Signals of Expansion Interface Connectors (Cont'd)

Net/Bus Name (Direction)	Blackfin A-V EZ-Extender Function	Relevant Configuration Jumpers
MOSI (Output)	The SPI serial output data signal used to program the control register of the AD1836A audio codec.	
MISO (Output)	The SPI serial input data signal used to read the control register of the AD1836A audio codec.	
RSCLK0 (Bi)	The processor's SPORT0 receive clock signal connected to the serial clock on the digital side of the audio codec's analog input. In I^2S mode, the signal can connect to the TSCLK0 net.	JP7.1/2
RFS0 (Bi)	The processor's SPORT0 receive frame sync signal connected to the frame sync on the digital side of the audio codec's analog input. In I^2S mode, the signal can connect to the TFS0 net.	JP7.1/2
DR0PRI (Output)	A connection to the data output of the audio codec; can be disconnected with a jumper if needed for another purpose.	JP7.3/4
DR0SEC (Output)	A secondary connection to the data output of the audio codec. Can be disconnected with a jumper if needed for another purpose.	JP7.5/6
TSCLK0 (Bi)	The processor's SPORT0 transmit clock signal, connects to the serial clock on the digital side of the audio codec's analog output. In I^2S mode, the signal can connect to the RSCLK0 net.	JP7.1/2
TFS0 (Bi)	The processor's SPORT0 transmit frame sync signal. Connects to the frame sync on the digital side of the audio codec's analog output. In I^2S mode, the signal can connect to the RFS0 net.	JP7.1/2
DT0PRI (Input)	A connection to the data input of the audio codec.	
DT0SEC (Input)	A secondary connection to the data input of the audio codec.	

Jumpers

Before using the Blackfin A-V EZ-Extender, follow the procedure in "A-V EZ-Extender Setup" on page 1-2.

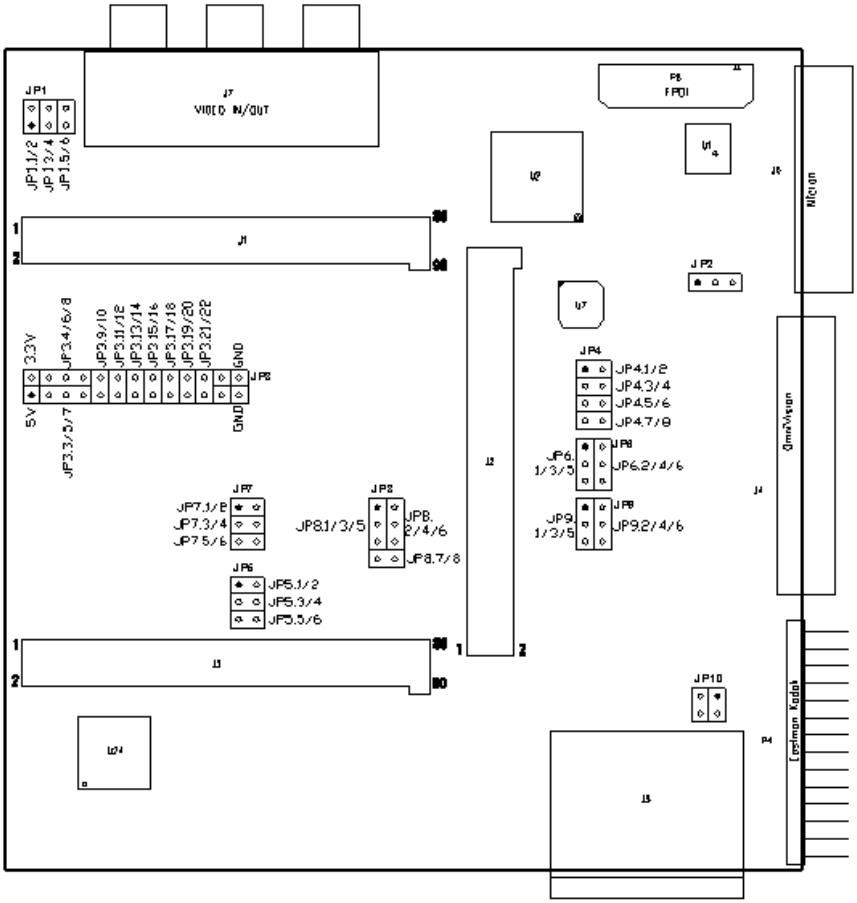

Figure 2-2. Jumper Locations

Figure 2-2 shows the jumper header locations. The jumper headers are divided to show each jumper's placement and rotation. The jumpers are described by the pins of the header on which the jumpers can be placed.

For example, JP3.4/6/8 refers to a single jumper that can be placed across pins 4 and 6 (or pins 6 and 8) of JP3. The dark pin indicates pin 1 of each header.

Video Test Loopback Jumpers (JP1.1/2, JP1.3/4, JP1.5/6)

For test purposes only, the video test jumpers loop-back the video encoder's output signals to the video decoder's input signals. By default, none of the video test loopback jumpers are installed.

Connector Voltage Selection Jumper (JP2)

The camera module and LCD display interfaces can be powered via the extender. The actual voltage of the interfaces, 3.3V or 5V, is determined by the JP2 jumper's placement (see Table 2-2).

Table 2-2. Jumper Locations and Connector Voltages

Jumper Location	Connector Voltage
JP2.1/2	3.3V
JP2.2/3	5V
Not installed	No power

TWI Source Selection Jumpers (JP3.3/5/7, JP3.4/6/8)

Due to the fact that some Blackfin processors feature a built-in 2-wire interface (TWI), while others need to emulate the interface with programmable flags, two jumpers are provided to plug the A-V EZ-Extender to both TWI sources (see Table 2-3).

Table 2-3. Jumper Locations and TWI Interface Sources

Jumper Location	TWI Interface Source
JP3.3/5 and JP3.4/6	Programmable flags
JP3.5/7 and JP3.6/8	2-wire interface of the processor

PDWN Connect Jumper (JP3.9/10)

Depending on the application, the PDWN pin of the OmniVision and Kodak cameras can be left floating or controlled by a flag pin (see Table 2-4).

Table 2-4. PWDN Pin Connections

JP3.9/10 Jumper	PDWN Connection
Uninstalled	PDWN is not used and, by default, the cameras function in standard mode
Installed	The PDWN functionality of the cameras is controlled by a flag pin of the processor.

Decoder HSYNC Disconnect Jumper (JP3.11/12)

To connect the horizontal sync signal of the video decoder to the PPI0 frame sync signal of the processor, install jumper JP3.11/12; otherwise, the decoder's horizontal sync is disconnected.

Decoder VSYNC Connect Jumper (JP3.13/14)

To connect the vertical sync signal of the video decoder to the PPI0 frame sync signal of the processor, install jumper JP3.13/14; otherwise, the decoder's vertical sync is disconnected.

Encoder HREF Connect Jumper (JP3.15/16)

To connect the horizontal sync signal of the video encoder to the PPI0 frame sync signal of the processor, install jumper JP3.15/16; otherwise, the encoder's horizontal reference is disconnected.

Encoder VSYNC Connect Jumper (JP3.17/18)

To connect the vertical sync signal of the video encoder to the PPI0 frame sync signal of the processor, install jumper JP3.17/18; otherwise, the encoder's vertical sync is disconnected.

Decoder Output Enable Jumper (JP3.19/20)

When installed, jumper JP3.19/20 enables the video decoder's data output signals on the VID_IN bus.

SNAPSHOT_FODD Disconnect Jumper (JP3.21/22)

The SNAPSHOT_FODD net of the Blackfin A-V EZ-Extender is a general-purpose flag pin. The flag pin connects to SNAPSHOT (the Kodak camera evaluation board's signal) and FODD (the OmniVision camera evaluation board' control signal). Do not install the jumper unless the processor needs to control these signals. The flag pin also connects to the SPI select pin of the AD1836A audio codec—do not install JP3.21/22 when using the audio interfaces.

PPI Clock Setup Jumpers (JP4.1/2, JP4.3/4, JP4.5/6, JP4.7/8)

The PPI_CLK signals of PPI0 and PPI1 are configured by the clock setup jumpers (see Table 2-5). For more information, refer to Figure 2-1 on page 2-4.

Table 2-5. PPI Clock Setup Jumper Results

Jumper Location	Result
JP4.1/2	Connects EXT_VID_CLK to the on-board 27 MHz oscillator. For more information about the EXT_VID_CLK signal, see the JP4.3/4 description.
JP4.3/4	Connects PPI0_CLK to the EXT_VID_CLK net. The EXT_VID_CLK net is the external clock, which drives the input clock of all three camera module connectors, plus the flat panel display connector. Depending on the JP4 jumper installation, EXT_VID_CLK can be generated by the PIXEL_CLK net, the VDEC_CLKOUT net, a socket (U8), or the on-board 27 MHz oscillator.
JP4.5/6	Connects VDEC_CLKOUT to PPI0_CLK; VDEC_CLKOUT drives the PPI0 clock when the video decoder is used.
JP4.7/8	Connects the PIXEL_CLK net, which is an output from the three camera interfaces, to PPI0_CLK.

PPI0 D8–15 Enable Jumper (JP5.1/2)

The JP5.1/2 jumper, when is not installed, disables the upper eight bits of the PPI0 data bus. This allows the signals connected to the upper eight bits of the PPI data bus of the EZ-KIT Lite to be used elsewhere on the board.

To disable and re-use the upper eight bits of the VID_IN and PPI0 data busses, install JP5.1/2.

VID_OUT Data Bus Control Jumpers (JP5.3/4, JP5.5/6)

The JP5.3/4 and JP5.5/6 jumpers are used together to set up the direction of and enable/disable the VID_OUT data bus drivers. Table 2-6 shows different combinations of JP5.3/4 and JP5.5/6.

Table 2-6. Video Out Data Bus Control Jumper Combinations

JP5.3/4	JP5.5/6	VID_OUT Status
Uninstalled	Uninstalled	VID_OUT, PPI1 are all not driven; PPI0 depends on the state of JP9.2/4/6
Uninstalled	Installed	PPI1 drives VID_OUT
Installed	Uninstalled	PPI0 drives VID_OUT
Installed	Installed	PPI0 drives VID_OUT, and VID_OUT drives PPI1 (loop-back mode)

PPI0_SYNC1 Direction Setup Jumper (JP6.1/3/5)

The direction of the PPI0_SYNC1 signal can be either fixed or programmed, depending on the state of a general-purpose flag. Table 2-7 shows how to set up the PPI0_SYNC1 direction.

Table 2-7. Setting Direction of PPI0_SYNC1 (JP6.1/3/5)

Jumper Location	PPI0_SYNC1 Direction
JP6.1/3	Controlled by a flag pin
JP6.3/5	Input to the processor
Uninstalled	Output from the processor

PPI0_SYNC2 Direction Setup Jumper (JP6.2/4/6)

The direction of the PPI0_SYNC2 signal can be either fixed or programmed, depending on the state of a general-purpose flag. Table 2-8 shows how to set the PPI0_SYNC2 direction.

Table 2-8. Setting Direction of PPI0_SYNC2 (JP6.2/4/6)

Jumper Location	PPI0_SYNC2 Direction
JP6.2/4	Controlled by a flag pin
JP6.4/6	Input to the processor
Uninstalled	Output from the processor

I²S Enable Jumper (JP7.1/2)

When JP7.1/2 is installed, the SPORT signals are routed for I²S SPORT communication protocol mode. To accomplish this, the receive and transmit clocks of the processor are driven by the output clock of the AD1836A audio codec. The same is done for the frame sync signals.

SPORT Data Connect Jumpers (JP7.3/4, JP7.5/6)

The JP7.3/4 and JP7.5/6 jumpers connect data output pins (ASDATA1 and ASDATA2) of the audio codec to the primary and secondary SPORT data input pins of the processor. The audio codec is driving these pins; with the help of the JP7.3/4 and JP7.5/6 jumpers, the processor's pins can be re-used when the codec is disabled.

VID_OUT Bus SYNC Source Select Jumpers (JP8.1/3/5, JP8.2/4/6)

The source of the PPI frame sync signals depends on the PPI port driving the VID_OUT bus. When using PPI0, place the jumpers at JP8.1/3 and JP8.2/4. When using PPI1, place the jumpers at JP8.3/5 and JP8.4/6.

VID_OUT Bus SYNC Enable Jumper (JP8.7/8)

To enable the VID_OUT frame sync signals, install JP8.7/8.

AV_RESET Source Jumper (JP9.1/3/5)

The source of ICs reset on the Blackfin A-V EZ-Extender is controlled by either a flag pin or a system reset; the latter also resets the Blackfin processor (see Table 2-9).

Table 2-9. Jumper Reset Sources

Jumper Location	Reset Source
JP9.1/3	Flag pin multiplexed with PPI1_D11
JP9.3/5	System reset generator
Uninstalled	ICs are not reset

PPI0_D Direction Setup Jumper (JP9.2/4/6)

The direction of the PPI0_D[15:0] signals can be a fixed direction or can be programmed, depending on the state of a general-purpose flag. Table 2-10 shows how to set up the PPI0_D[15:0] direction.

Table 2-10. Setting Direction of PPI0_D[15:0] (JP9.2/4/6)

Jumper Location	PPI0_D[15:0] Direction
JP9.2/4	Controlled by a flag pin
JP9.4/6	Input to the processor
Uninstalled	Output from the processor

Audio Loopback Jumpers (JP10.1/2, JP10.3/4)

The JP10.1/2 and JP10.3/4 jumpers loop-back audio input to output for test purposes and should not be installed.

A A-V EZ-EXTENDER BILL OF MATERIALS

The bill of materials corresponds to "A-V EZ-Extender Schematic" on page B-1.

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
1	1	SN74AHC1G00 SOT23-5	U9	TI	SN74AHC1G00DBVR
2	1	12.288MHZ OSC003	U18	DIGI-KEY	SG-8002CA-PCC-ND (12.288M)
3	5	SN74LVC1G125 SOT23-5	U15,U17,U19,U29-30	TI	74LVC1G125DBVRE4
4	1	27MHZ OSC003	U1	DIGI-KEY	SG-8002CA-PCC-ND (27.00M)
5	1	SN74LVC1G32 SOT23-5	U6	TI	SN74LVC1G32DBVRE4
6	1	74LVTH16244MTD TSSOP48	U10	FAIRCHILD	74LVTH16244MTD
7	3	74LVTH16245MTD TSSOP48	U11,U14,U16	FAIRCHILD	74LVTH16245MTD
8	1	ADP3336ARMZ MSOP8	VR1	ANALOG DEVICES	ADP3336ARMZ-REE
9	1	10MA AD1580BRTZ SOT23D	D1	ANALOG DEVICES	AD1580BRTZ-REEL7
10	3	AD8061ARTZ SOT23-5	U3-5	ANALOG DEVICES	AD8061ARTZ-REEL

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
11	8	AD8606ARZ SOIC8	U20-23,U25-28	ANALOG DEVICES	AD8606ARZ
12	1	AD1836AASZ MQFP52	U24	ANALOG DEVICES	AD1836AASZ
13	1	ADV7179KCPZ LFCSP40	U7	ANALOG DEVICES	ADV7179KCPZ
14	1	ADV7183BKSTZ LQFP80	U2	ANALOG DEVICES	ADV7183BKSTZ
15	1	DIP 8 DIP8SOC	U8	MILL-MAX	614-43-308-31-007000
16	3	0.05 45x2 CON018	P1-3	SAMTEC	TFC-145-32-F-D
17	3	.05 45X2 CON019	J1-3	SAMTEC	SFC-145-T2-F-D-A
18	1	RCA 3X2 CON024	J7	SWITCH-CRAFT	PJRAS3X2S01X
19	5	IDC 3X2 IDC3X2_SMT	JP1,JP5-7,JP9	SAMTEC	TSM-103-01-T-DV
20	1	IDC 16X2 IDC16X2RASOC	J4	SAMTEC	SSW-116-02-F-D-RA
21	1	IDC 13X2 IDC13X2_M_SMT	JP3	SAMTEC	TSM-113-01-T-DV
22	2	IDC 4X2 IDC4X2_M_SMT	JP4,JP8	SAMTEC	TSM-104-01-T-DV
23	1	FPDI 31PIN CON034	P6	FCI	68737-428HLF
24	1	IDC 13x2RA IDC13x2_F_RA	J6	SAMTEC	SSW-113-02-F-D-RA
25	1	IDC 3X1 IDC3X1	JP2	FCI	90726-403HLF
26	1	IDC 2X2 IDC2X2	JP10	SULLINS	PBC02DAAN
27	8	0.22UF 25V 10% 0805	C73,C85,C101, C112,C120-121, C135,C138	AVX	08053C224FAT
28	1	33 1/10W 5% 0805	R49	VISHAY	CRCW080533R0JNEA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
29	1	1.5K 1/10W 5% 0805	R1	VISHAY	CRCW08051K50FKEA
30	6	10UF 16V 10% B	CT1-4,CT12-13	AVX	TAJB106K016R
31	5	600 100MHZ 200MA 0603	FER4-8	DIGI-KEY	490-1014-2-ND
32	4	600 100MHZ 500MA 1206	FER1-3,FER9	STEWARD	HZ1206B601R-10
33	10	10UF 16V 20% CAP002	CT5-11,CT14-16	PANASONIC	EEE1CA100SR
34	2	22 1/10W 5% 0805	R53,R55	VISHAY	CRCW080522R0JNEA
35	6	0.68UH 10% 0805	L1-3,L7-9	MURATA	LQM21NNR68K10D
36	1	.082UF 50V 5% 0805	C5	AVX	08055C823JAT2A
37	3	2.2UH 10% 0805	L4-6	DIGI-KEY	490-1119-2-ND
38	4	22 125MW 5% RNS001	RN1-4	CTS	744C083220JP
39	1	147.0K 1/10W 1% 0805	R36	DIGI-KEY	311-147KCRTR-ND
40	1	76.8K 1/10W 1% 0805	R38	DIGI-KEY	311-76.8KCRTR-ND
41	1	1.2K 1/16W 5% 0402	R42	PANASONIC	ERJ-2GEJ122X
42	57	0.1UF 16V 10% 0603	C1,C4,C7-8,C10-15, C17,C19,C22-23, C26,C30,C32-34, C37-38,C40,C43-44, C46-49,C51-57, C60-69,C75-76,C78, C81,C99,C115, C124,C130-132, C144-145	AVX	0603YC104KAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
43	11	0.01UF 16V 10% 0603	C2-3,C6,C16,C25, C29,C36,C41,C50, C58,C110	AVX	0603YC103KAT2A
44	5	10UF 10V +80/-20% 0805	C42,C45,C59, C79-80	PANASONIC	ECJ-2FF1A106Z
45	2	1UF 16V 10% 0603	C27,C39	PANASONIC	ECJ-1VB1C105K
46	12	330PF 50V 5% 0603	C18,C20-21,C28, C31,C35,C98,C104, C107-108,C133, C137	AVX	06035A331JAT2A
47	3	22 1/10W 5% 0603	R146-148	VISHAY	CRCW060322R0JNEA
48	19	10K 1/10W 5% 0603	R3-4,R10,R32,R37, R44-45,R47,R51, R54,R56-60,R107, R141,R149-150	VISHAY	CRCW060310K0JNEA
49	2	100K 1/10W 5% 0603	R39-40	VISHAY	CRCW0603100KJNEA
50	8	0 1/10W 5% 0603	R2,R15,R20,R25, R111,R115,R130, R135	PHYCOMP	232270296001L
51	1	10 1/10W 5% 0603	R143	VISHAY	CRCW060310R0JNEA
52	6	1K 1/10W 5% 0603	R13-14,R18-19,R23-24	DIGI-KEY	311-1.0KGRTR-ND
53	4	237.0 1/10W 1% 0603	R64,R70,R106,R110	DIGI-KEY	311-237HRTR-ND
54	4	750.0K 1/10W 1% 0603	R65,R69,R127,R129	DIGI-KEY	311-750KHRTR-ND
55	6	11.0K 1/10W 1% 0603	R82,R90,R93-94, R123,R126	DIGI-KEY	311-11.0KHRTR-ND
56	12	5.49K 1/10W 1% 0603	R75,R83,R86-87, R89,R99-101,R116, R119,R131-132	DIGI-KEY	311-5.49KHRTR-ND

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
57	6	3.32K 1/10W 1% 0603	R81,R91-92,R95, R124-125	DIGI-KEY	311-3.32KHRTR-ND
58	6	1.65K 1/10W 1% 0603	R74,R84-85,R88, R117-118	DIGI-KEY	311-1.65KHRTR-ND
59	6	49.9K 1/10W 1% 0603	R96-97,R108-109, R137-138	DIGI-KEY	311-49.9KHRTR-ND
60	6	604.0 1/10W 1% 0603	R98,R102-104,R133, R136	DIGI-KEY	311-604HRTR-ND
61	16	5.76K 1/10W 1% 0603	R61-63,R67,R72-73, R76-77,R105,R120-122,R128,R134, R139-140	DIGI-KEY	311-5.76KHRTR-ND
62	8	120PF 50V 5% 0603	C71,C74,C82-83, C127-128,C141, C143	AVX	06035A121JAT2A
63	12	100PF 50V 5% 0603	C77,C91-92,C97, C105-106,C109, C118,C129,C134, C13	AVX	06035A101JAT2A
64	10	1000PF 50V 5% 0603	C9,C24,C72,C86, C93,C100,C103, C111,C117,C119	PANASONIC	ECJ-1VC1H102J
65	6	220PF 50V 5% 0603	C87,C94-96, C125-126	PANASONIC	ECJ-1VC1H221J
66	6	680PF 50V 5% 0603	C84,C88-90, C122-123	PANASONIC	ECJ-1VC1H681J
67	6	2200PF 50V 5% 0603	C102,C113-114, C116,C140,C142	PANASONIC	ECJ-1VB1H222K
68	7	33.0 1/10W 1% 0603	R5,R8,R33,R68, R142,R144-145	DIGI-KEY	311-33.0HRTR-ND
69	6	2.74K 1/10W 1% 0603	R71,R78-80, R112-113	DIGI-KEY	311-2.74KHRTR-ND

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
70	12	75.0 1/10W 1% 0603	R11-12,R16-17,R21-22,R26-31	DALE	CRCW060375R0FKEA
71	1	680 1/8W 5% 1206	R114	VISHAY	CRCW1206680RFNEA
72	1	150.0 1/8W 1% 1206	R41	VISHAY	CRCW1206150RFKEA
73	1	GREEN LED001	LED1	PANASONIC	LN1361CTR
74	2	3.5MM DUAL_STEREO CON066	J8-J9	SWITCH-CRAFT	35RAPC7JS
75	1	3.5MM STEREO_JACK CON_SJ-3523-SMT	J10	DIGI-KEY	CP-3523SJCT-ND

Blackfin A-V EZ-Extender Schematic

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Title	BLACKFIN A-V EZ-EXTENDER TITLE		
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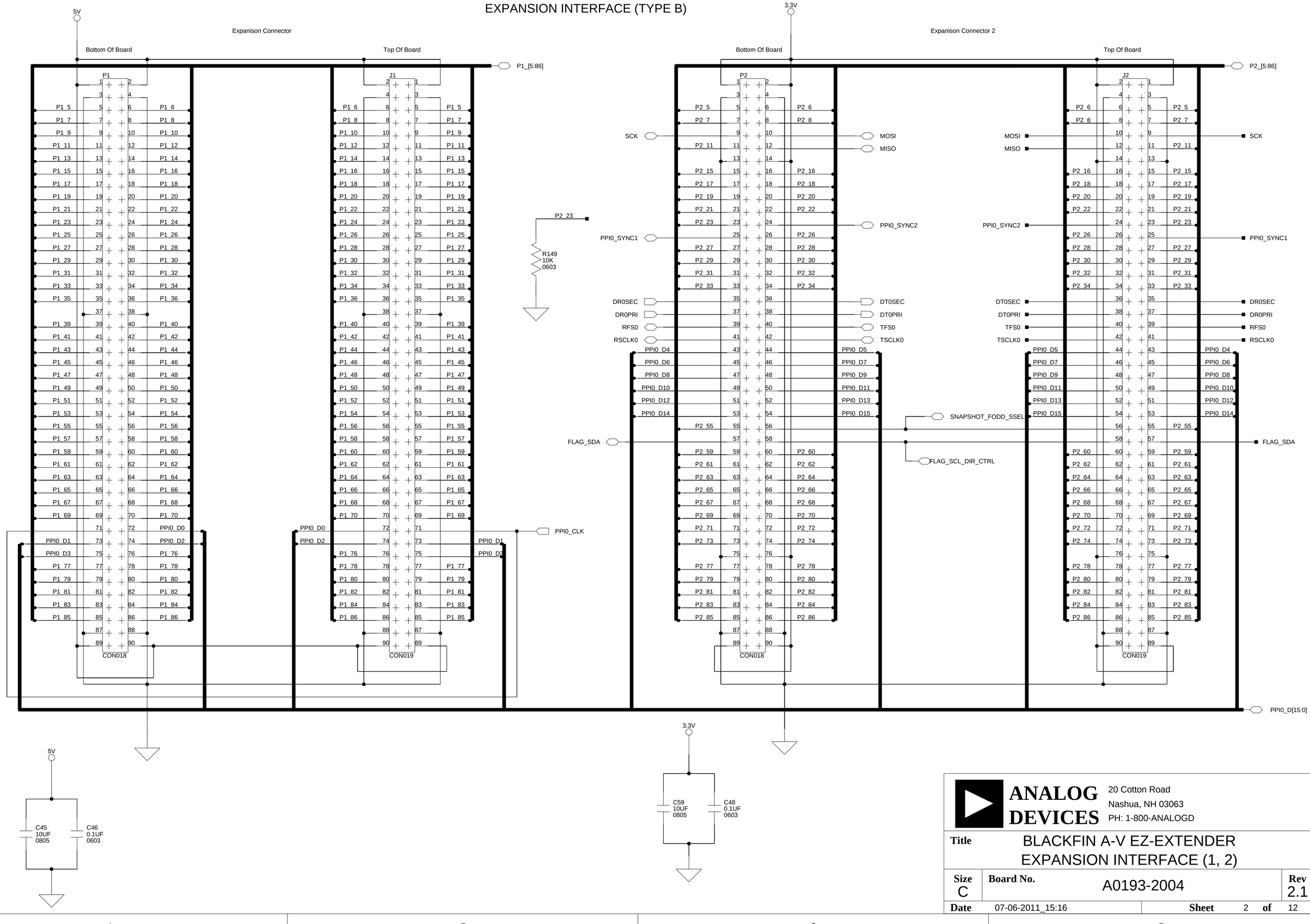
Date 07-06-2011_15:05		**Sheet** 1 **of** 12	

EXPANSION INTERFACE (TYPE B)



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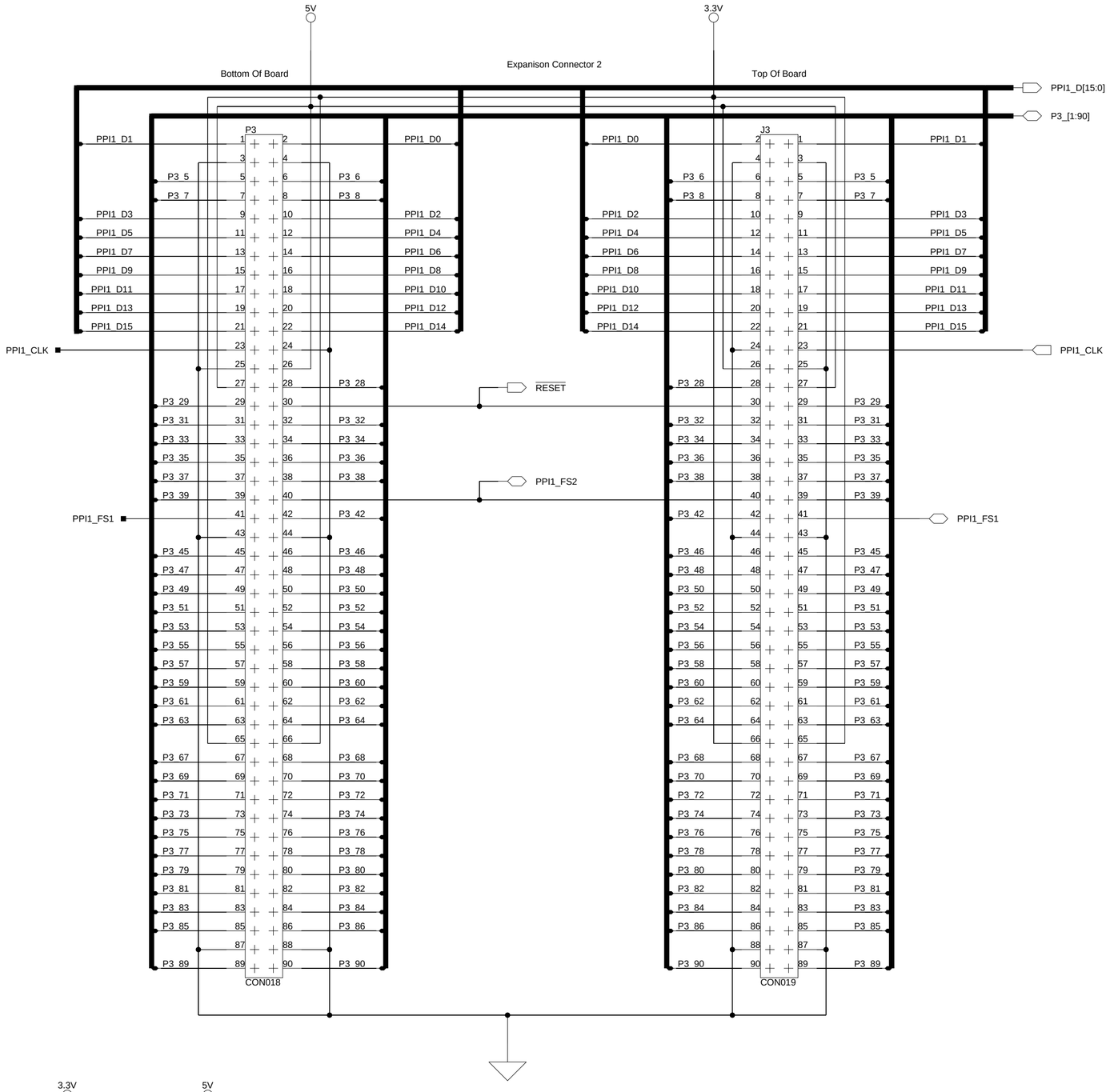
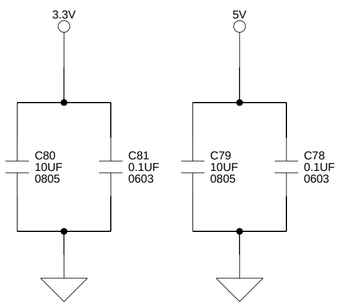
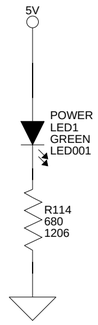
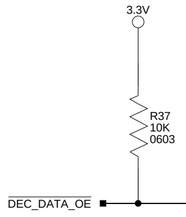
Title	BLACKFIN A-V EZ-EXTENDER EXPANSION INTERFACE (1, 2)		
Size C	**Board No.** A0193-2004		**Rev** 2.1
Date 07-06-2011_15:16		**Sheet** 2 **of** 12	

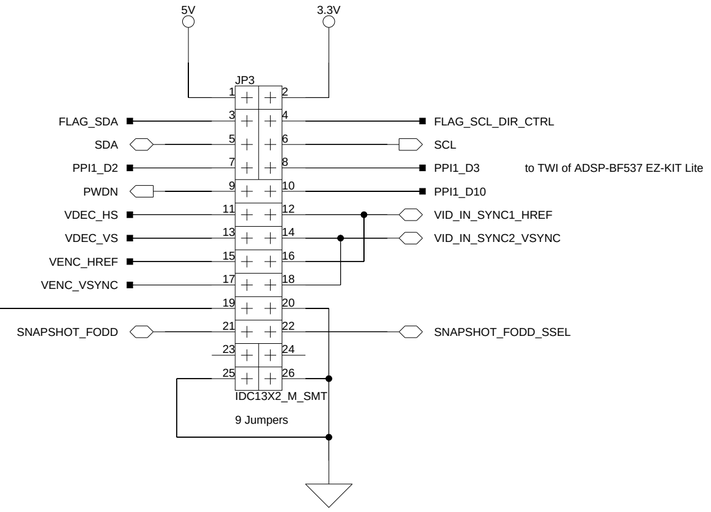
EXPANSION INTERFACE (TYPE B)











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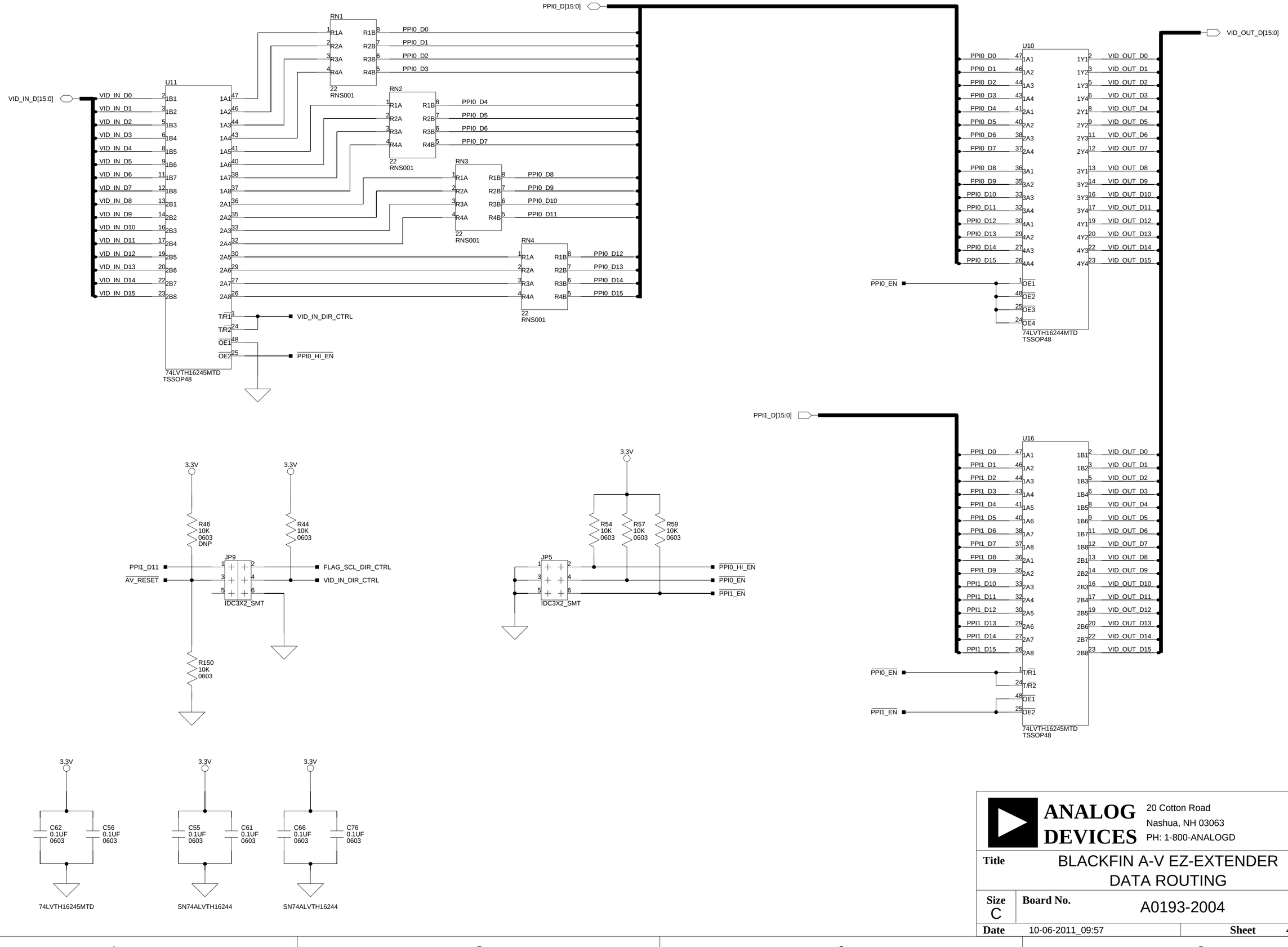
Title	BLACKFIN A-V EZ-EXTENDER EXPANSION INTERFACE (3)		
Size C	**Board No.** A0193-2004		**Rev** 2.1
Date 07-06-2011_15:16		**Sheet** 3 **of** 12	



Title	BLACKFIN A-V EZ-EXTENDER DATA ROUTING
Size	C
Board No.	A0193-2004
Rev	2.1
Date	10-06-2011_09:57
Sheet	4 of 12

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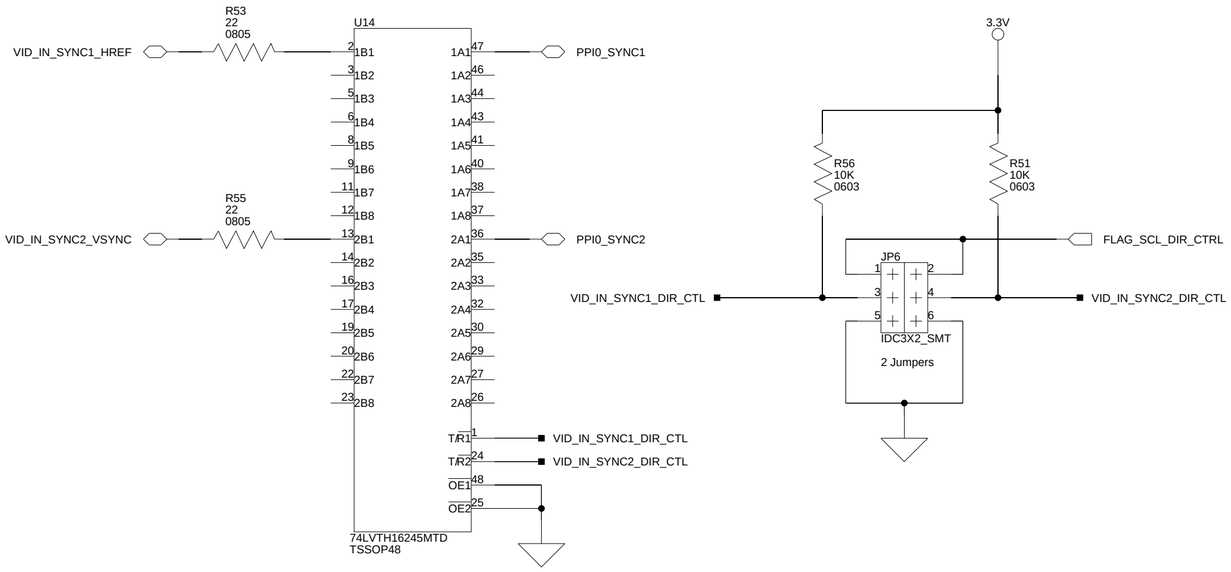
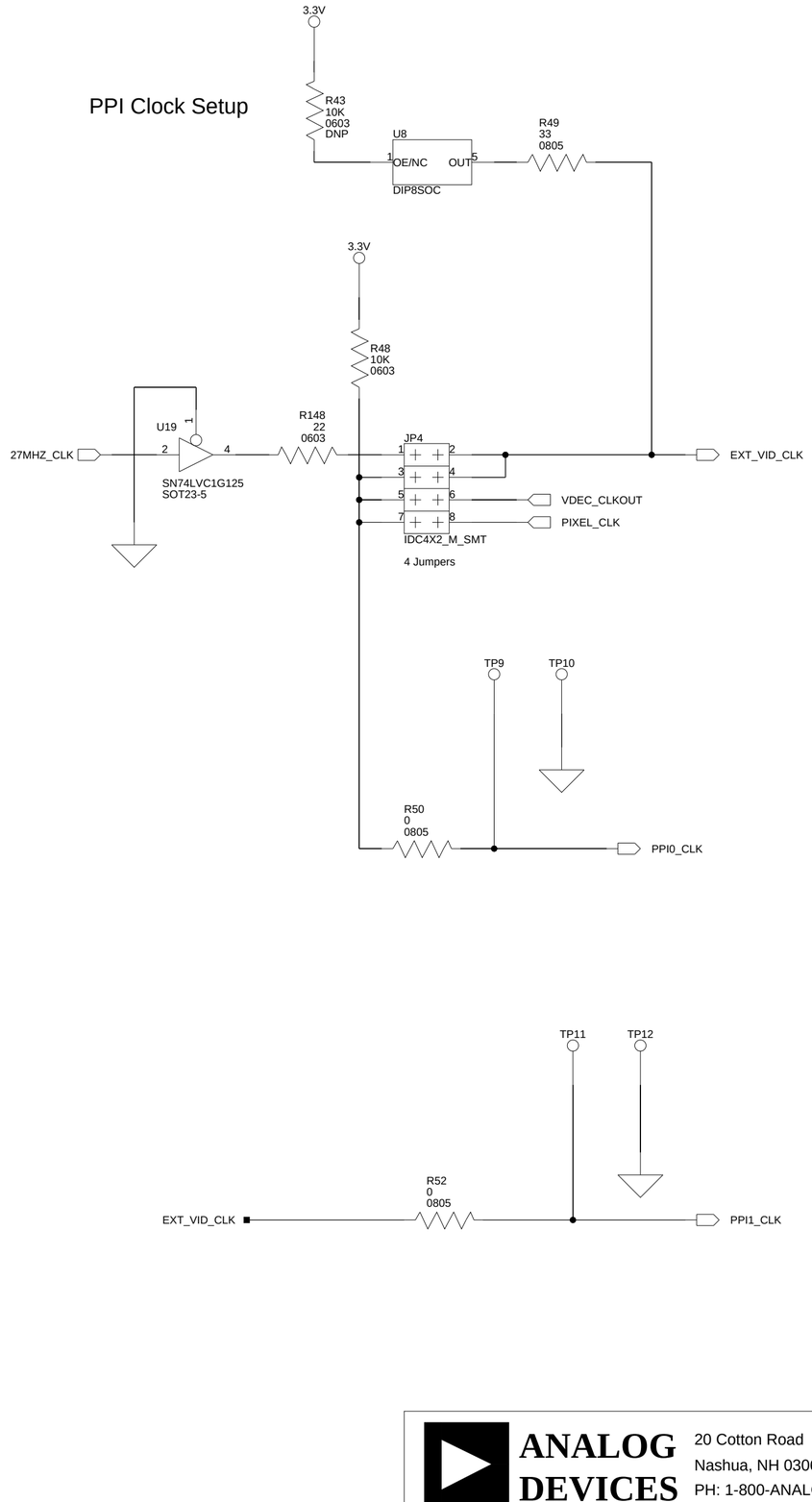
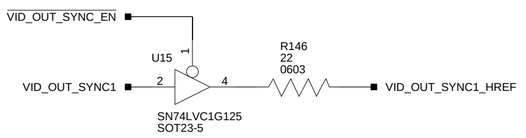
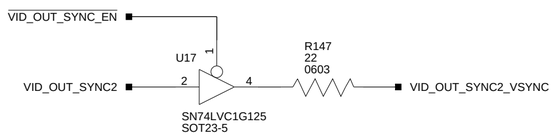
Video In Frame Sync Setup



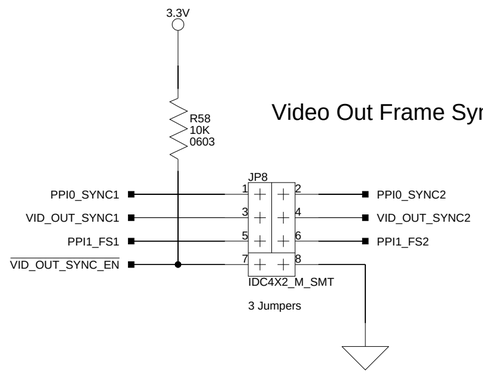
PPI Clock Setup

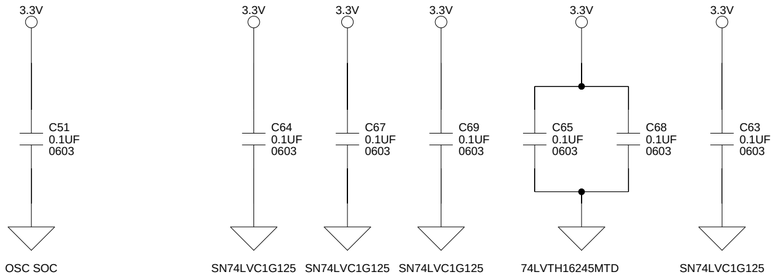






Video Out Frame Sync Setup





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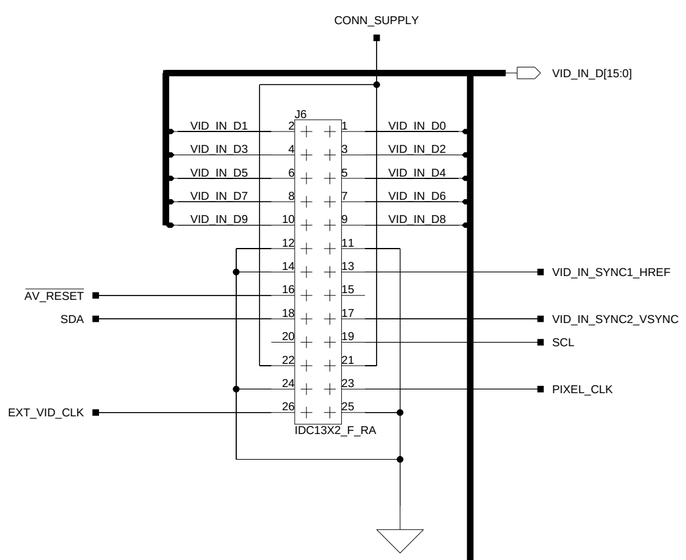
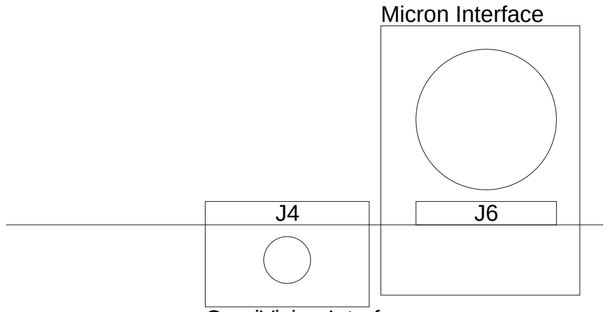
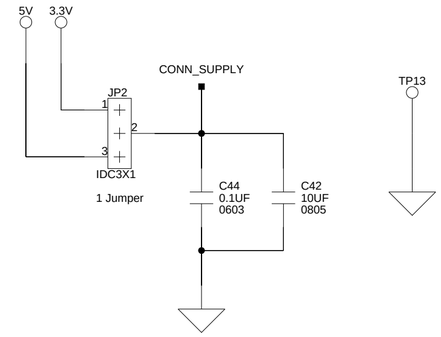
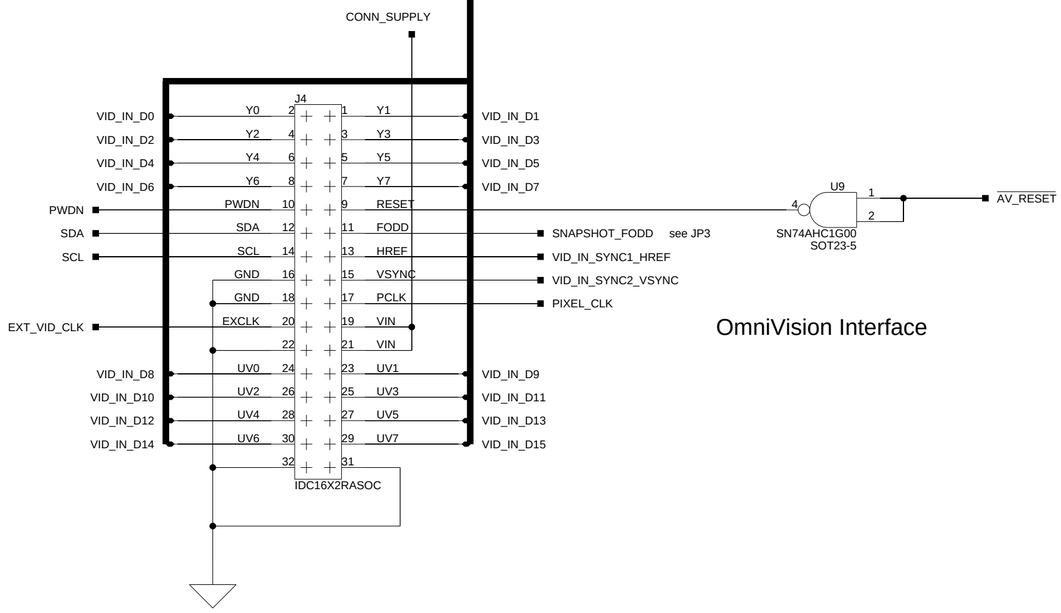
Title	BLACKFIN A-V EZ-EXTENDER FS/CLK CONFIG	
Size C	**Board No.** A0193-2004	**Rev** 2.1
Date 07-06-2011_15:16	**Sheet** 5 **of** 12	



Micron Interface

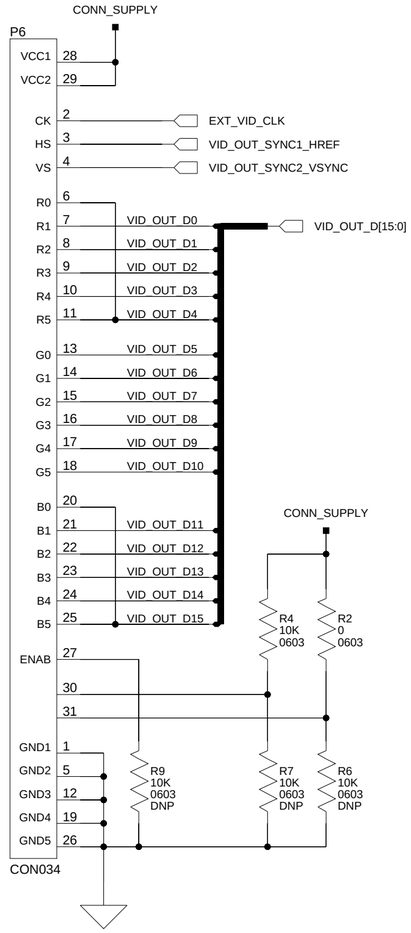


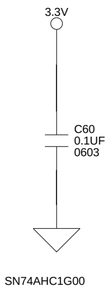




OmniVision Interface

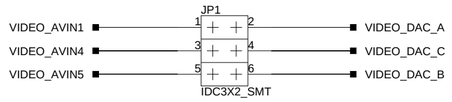
Flat Panal Display Interface

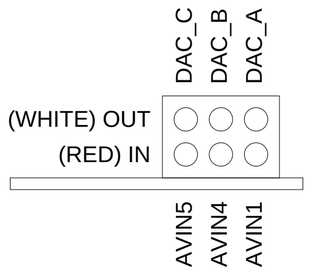




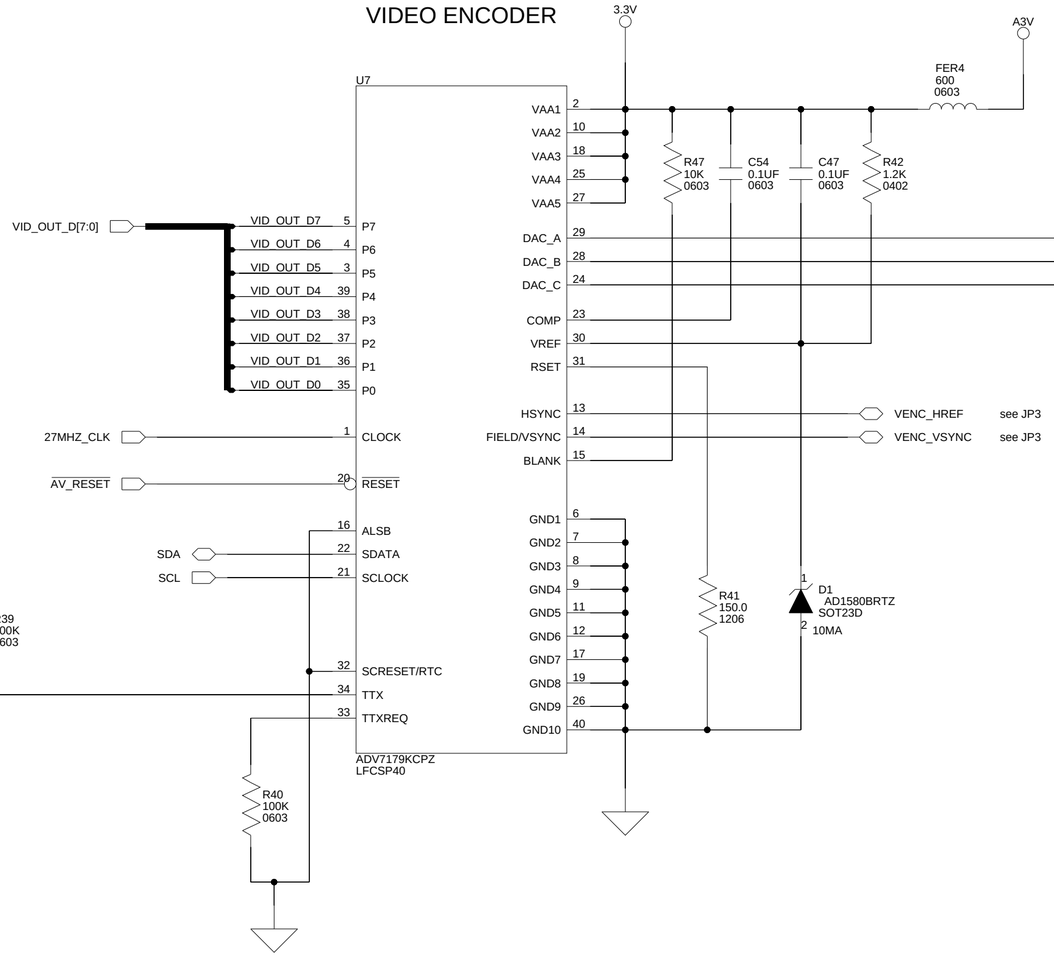
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

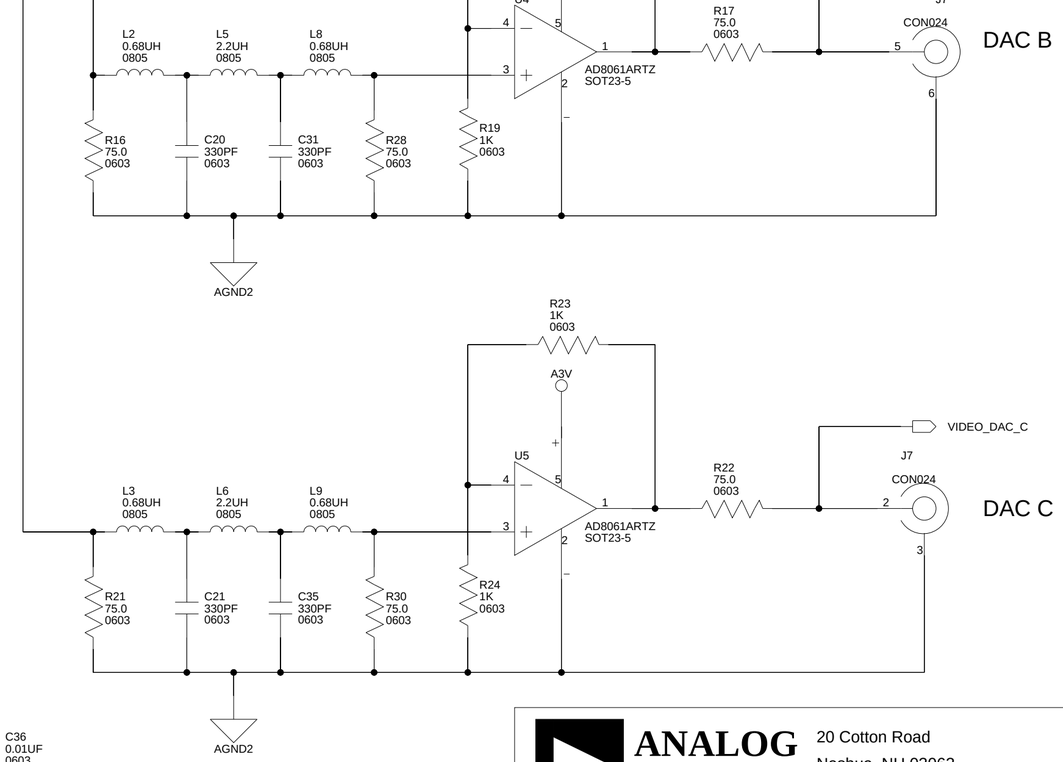
Title	BLACKFIN A-V EZ-EXTENDER PPI0 SETUP	
Size C	**Board No.** A0193-2004	**Rev** 2.1
Date 07-06-2011_15:16	**Sheet** 6 **of** 12	

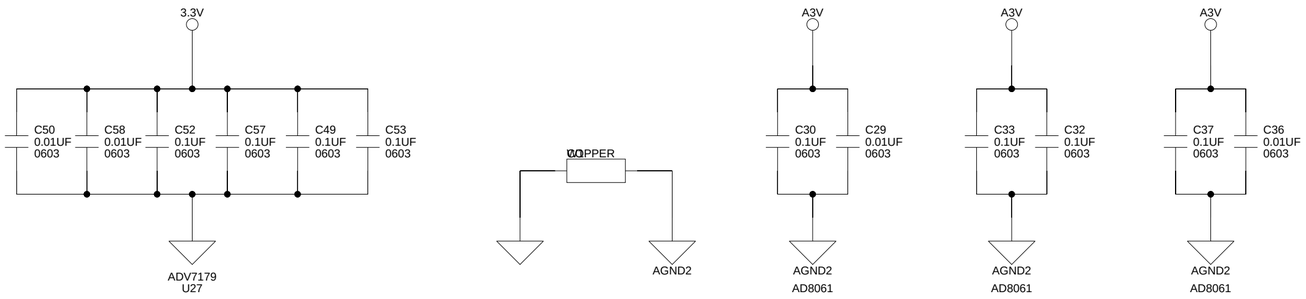




	DAC A	DAC B	DAC C
Composite Video	CVSB	CVSB	C
Component Video	G	B	R
Differential Component Video	Y	U	V
S Video	Y		C







ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	BLACKFIN A-V EZ-EXTENDER VIDEO ENCODER (OUT)	
Size C	**Board No.** A0193-2004	**Rev** 2.1
Date 07-06-2011_15:16	**Sheet** 7 **of** 12	

VIDEO DECODER

	AVIN1	AVIN4	AVIN5
Composite Video	CVBS	CVBS	CVBS
Differential Component Video	Y	V	U
S Video	Y	C	

3.3V
R10 10K 0603
U1
OE
OUT
27MHZ OSC003
R5 33.0 0603
27MHZ_CLK
R34 10K 0603 DNP
R35 10K 0603 DNP
R45 10K 0603
R3 10K 0603
U2
XTAL
XTAL1
ALSB
SDA
SCL
AV_RESET
RESET
PWRDN
NC[ISO]
AIN1
AIN7
AIN2
AIN8
AIN3
AIN9
AIN4
AIN10
AIN5
AIN11
AIN6
AIN12
REFOUT
CML
CAPY1
CAPY2
CAPC1
CAPC2
AVDD
PVDD
AGND1
AGND2
AGND3
AGND4
AGND5
NC[AGND6]
ADV7183BKSTZ LQFP80

J7 CON024
AVIN1
VIDEO_AVIN1
R15 0 0603
C19 0.1UF 0603
TP1
AVIN4
VIDEO_AVIN4
R20 0 0603
C34 0.1UF 0603
TP2
AVIN5
VIDEO_AVIN5
R25 0 0603
C22 0.1UF 0603
TP3
AGND2

R27 75.0 0603
R29 75.0 0603
R31 75.0 0603
CT3 10UF B
C12 0.1UF 0603
CT2 10UF B
C14 0.1UF 0603
CT1 10UF B
C8 0.1UF 0603
C9 1000PF 0603
C1 0.1UF 0603
C11 0.1UF 0603
CT4 10UF B
C23 0.1UF 0603
C24 1000PF 0603
C15 0.1UF 0603
C38 0.1UF 0603
1.8V 3.3V
FER2 600 1206
FER1 600 1206
PVDD_ADV7183
C4 0.1UF 0603
C3 0.01UF 0603
C7 0.1UF 0603
C6 0.01UF 0603

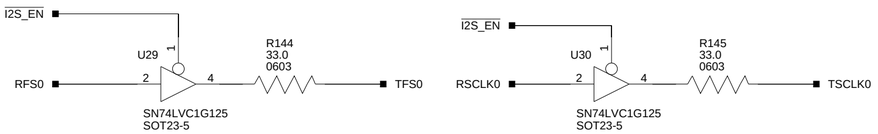
P15 VID_IN_D7
P14 VID_IN_D6
P13 VID_IN_D5
P12 VID_IN_D4
P11 VID_IN_D3
P10 VID_IN_D2
P9 VID_IN_D1
P8 VID_IN_D0
VID_IN_D[7:0]
P7
P6
P5
P4
P3
P2
P1
P0
LLC1
LLC2
NC[LLCREF]
ELPF
HS
VS
FIELD
NC[VREF]
NC[HREF]
NC[CLKIN]
NC[AFF]
SFL[HFF]
NC[AEF]
NC[DV]
NC[RD]
OE
DEC_DATA_OE
NC[GPO3]
NC[GPO2]
NC[GPO1]
NC[GPO0]
DVDD1
DVDD2
DVDD3
DVDDIO1
DVDDIO2
DGND1
DGND2
DGND3
DGND4
DGND5

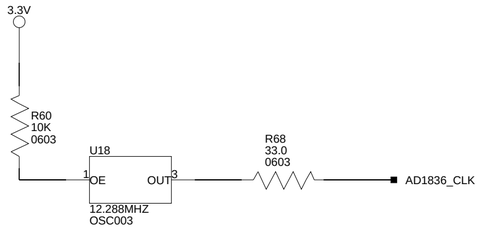
R8 33.0 0603
U6
SN74LVC1G32 SOT23-5
R33 33.0 0603
VDEC_CLKOUT
PVDD_ADV7183
C2 0.01UF 0603
R1 1.5K 0805
C5 .082UF 0805
TP4 TP5 TP6
VDEC_HS see JP3
VDEC_VS see JP3
VDEC_FIELD
VDEC_VREF
VDEC_HREF
DVDD_ADV7183
FER3 600 1206
1.8V 3.3V

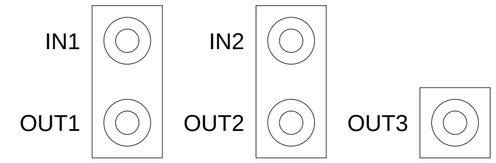
3.3V 3.3V
R32 10K 0603
VR1
IN1
IN2
SD
OUT1
OUT2
OUT3
FB
GND
ADP3336ARMZ MSOP8
R38 76.8K 0805
R36 147.0K 0805
C27 1UF 0603
C39 1UF 0603
1.8V

3.3V
C17 0.1UF 0603
27MHZ OSC
3.3V
C41 0.01UF 0603
SN74LVC1G32
3.3V
DVDD_ADV7183
C40 0.1UF 0603
C13 0.1UF 0603
C16 0.01UF 0603
C25 0.01UF 0603
C26 0.1UF 0603
C43 0.1UF 0603
C10 0.1UF 0603
ADV7183 U28

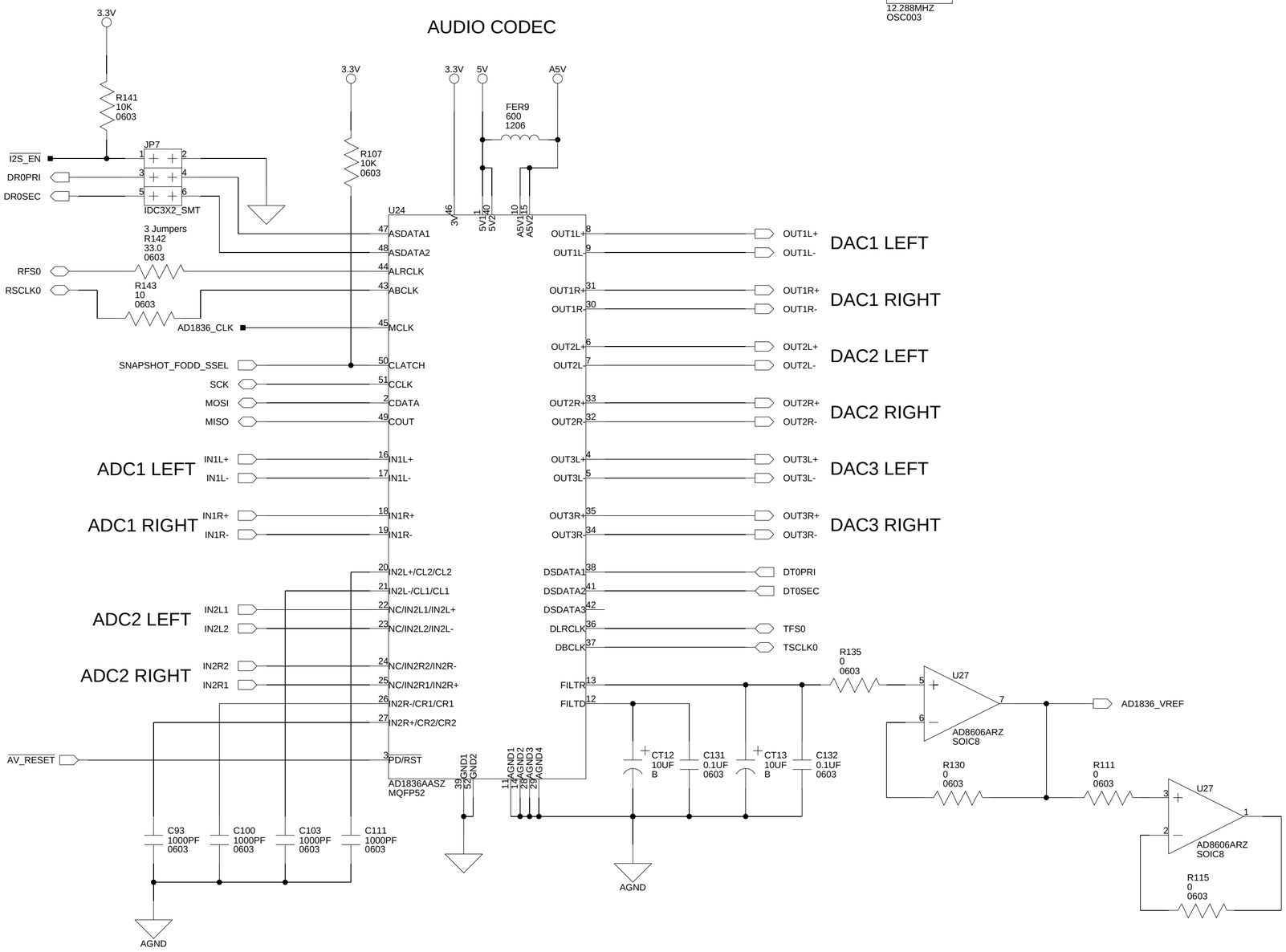
ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	BLACKFIN A-V EZ-EXTENDER VIDEO DECODER (IN)	
Size C	Board No. A0193-2004	Rev 2.1
Date 07-06-2011_15:16	Sheet 8 of 12	

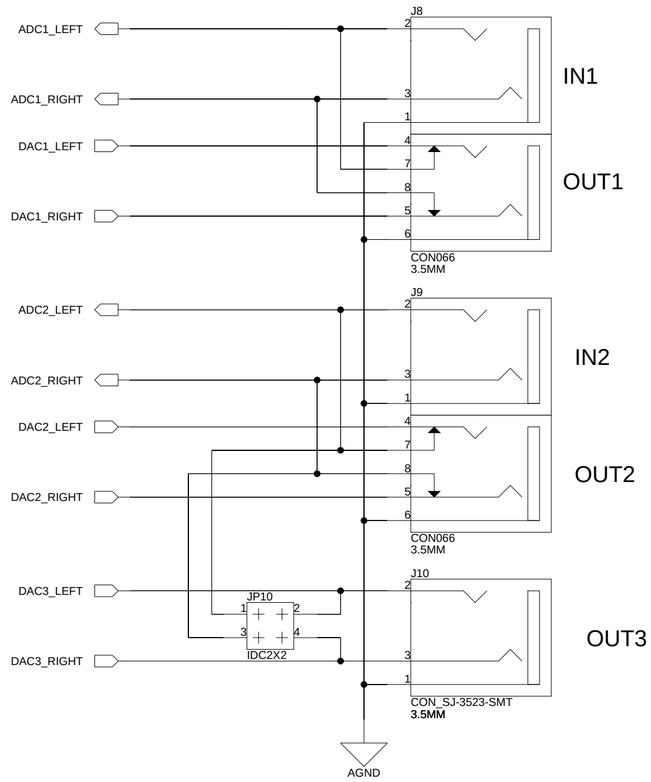


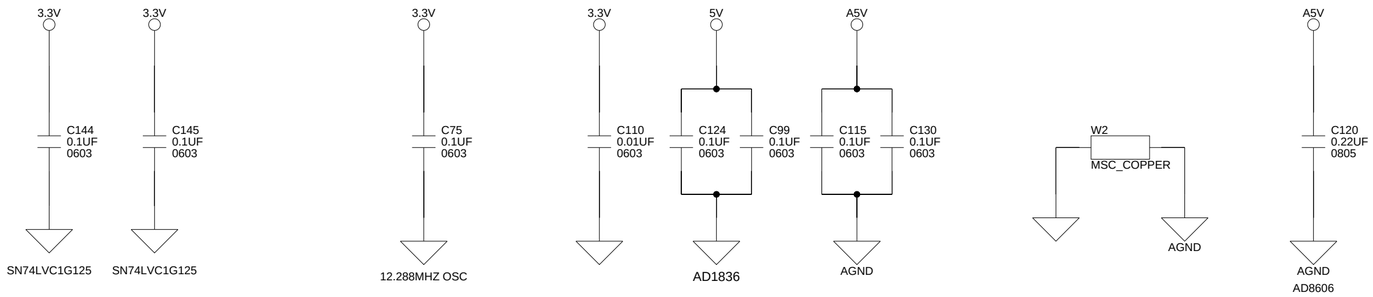




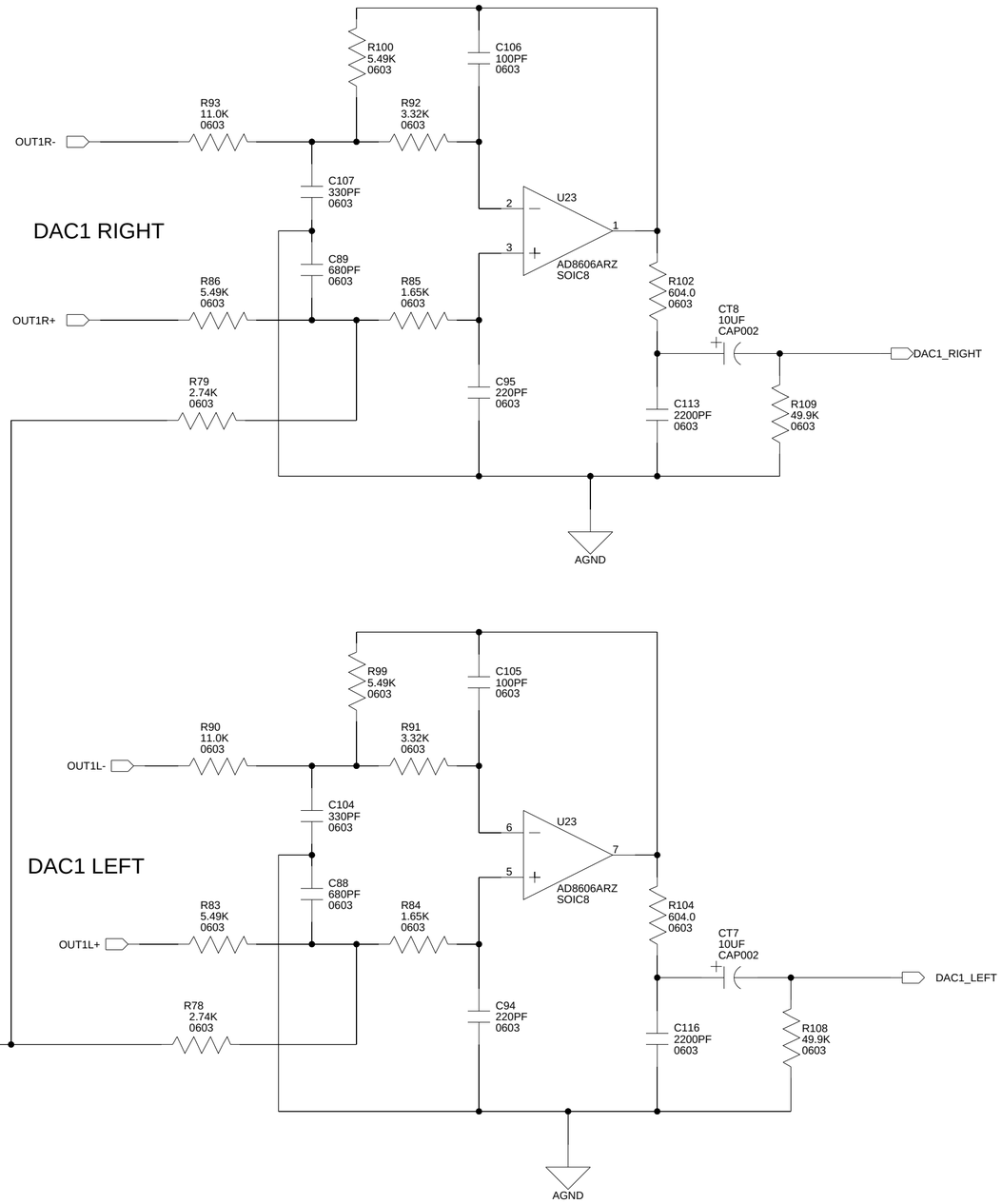
AUDIO CODEC





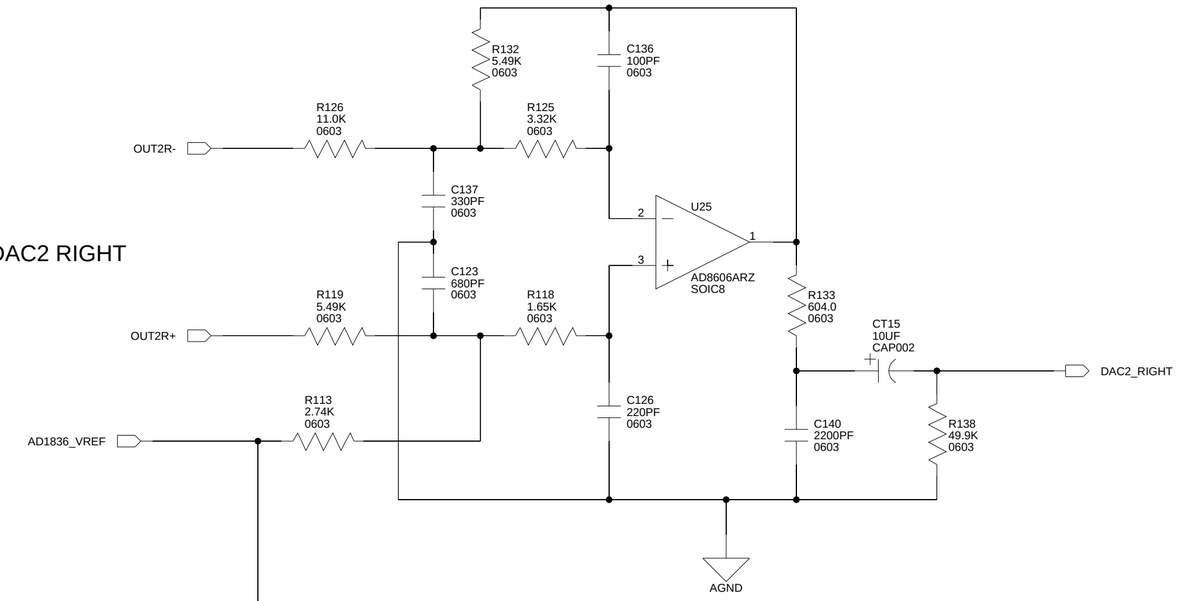


ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
Title	BLACKFIN A-V EZ-EXTENDER AUDIO		
Size C	**Board No.** A0193-2004		**Rev** 2.1
Date 21-06-2011_10:31	**Sheet** 9 **of** 12		

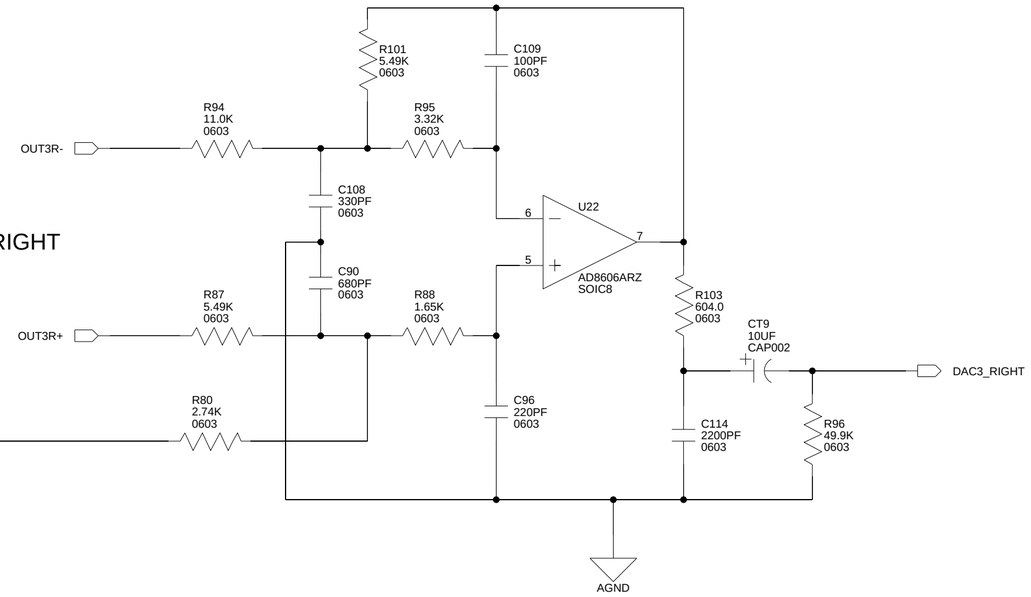


ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	BLACKFIN A-V EZ-EXTENDER AUDIO OUT(CH1)	
Size C	**Board No.** A0193-2004	**Rev** 2.1
Date 07-06-2011_15:16	**Sheet** 10 **of** 12	

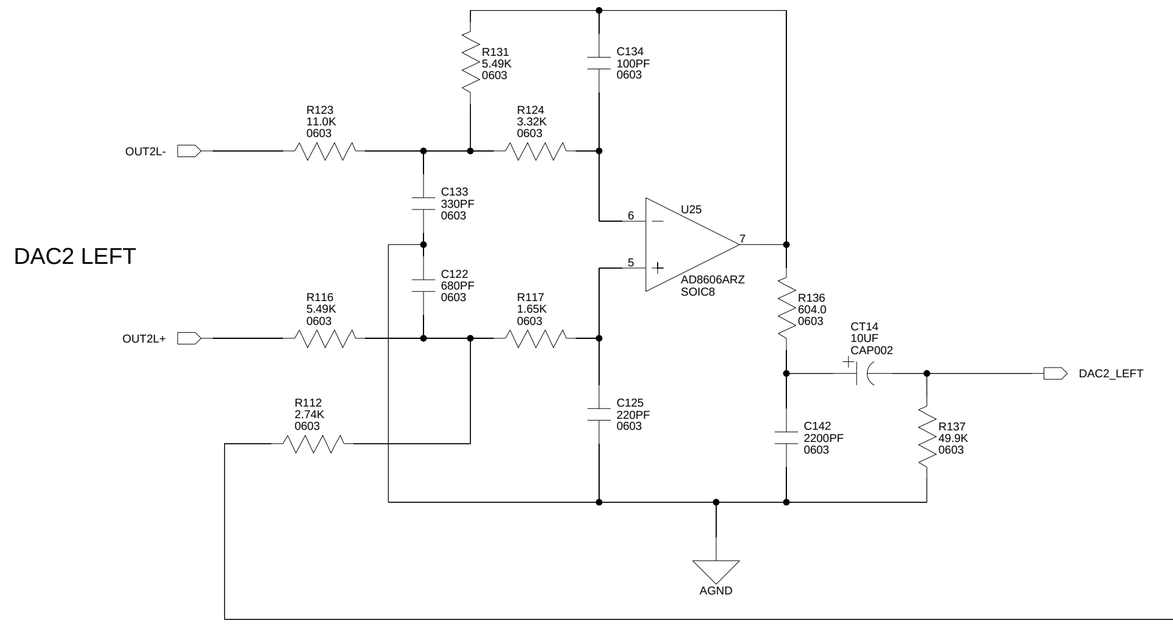
DAC2 RIGHT



DAC3 RIGHT



DAC2 LEFT



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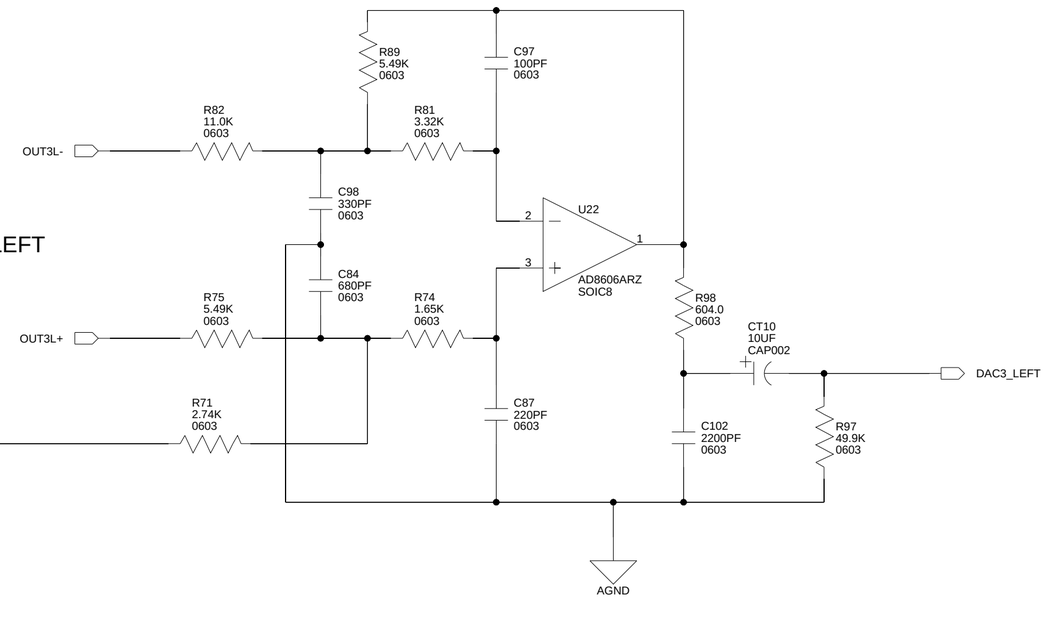
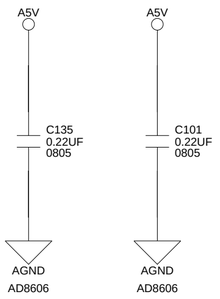
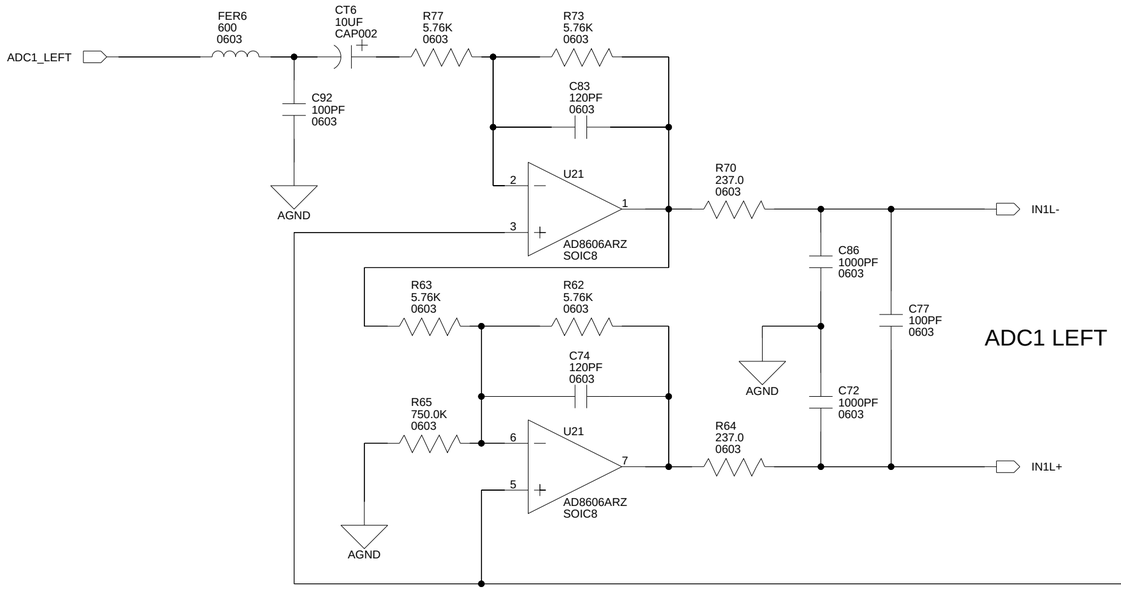




ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	BLACKFIN A-V EZ-EXTENDER AUDIO OUT(CH2, CH3)	
Size C	**Board No.** A0193-2004	**Rev** 2.1
Date 07-06-2011_15:16	**Sheet** 11 **of** 12	



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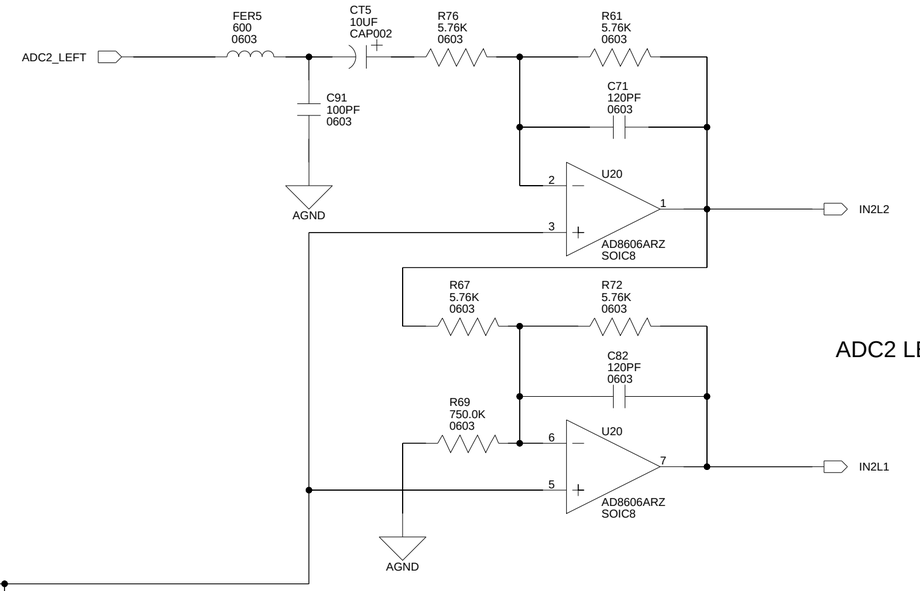
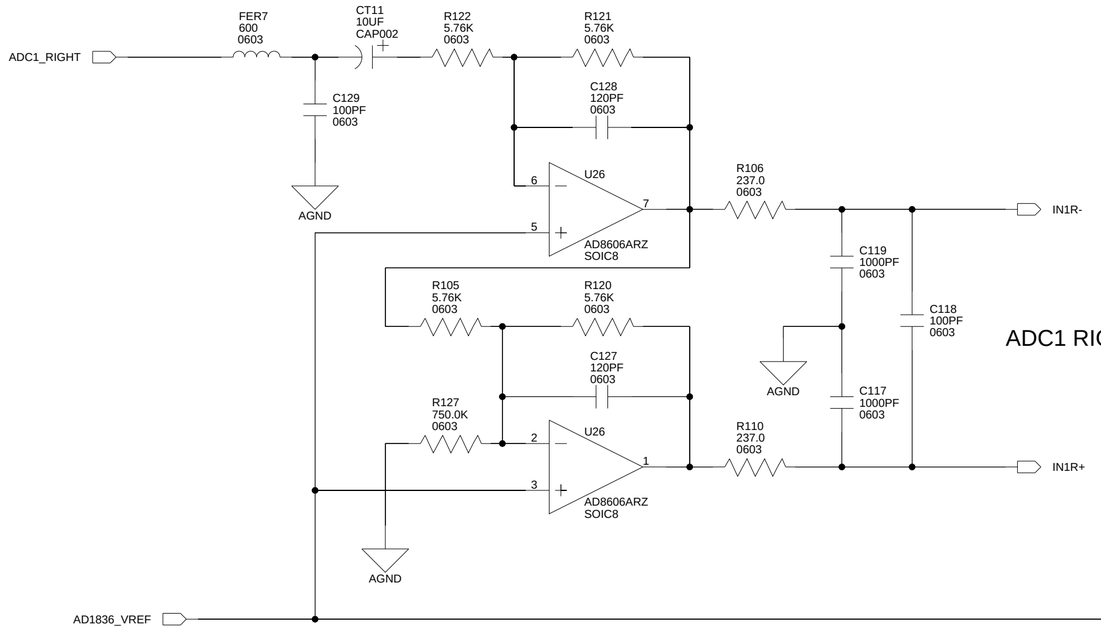
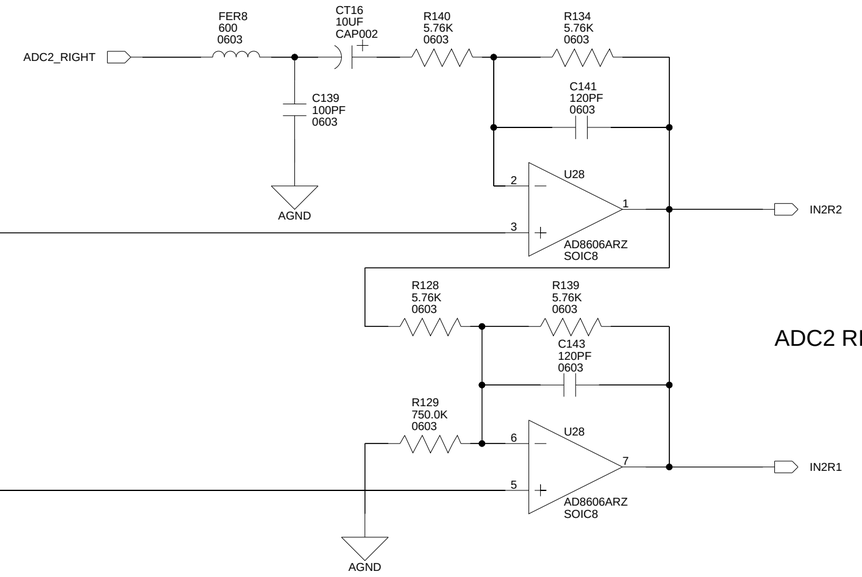


ADC2 LEFT



ADC1 RIGHT



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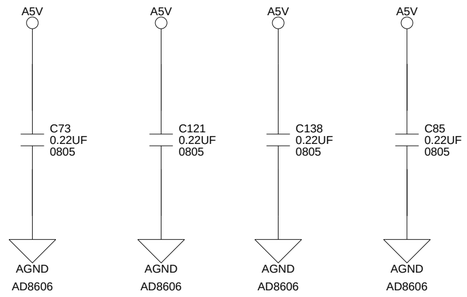

ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
Title	BLACKFIN A-V EZ-EXTENDER AUDIO IN(CH1, CH2)		
Size C	**Board No.** A0193-2004		**Rev** 2.1
Date 10-06-2011_09:57		**Sheet** 12 **of** 12	

I INDEX

D

E

F

G

H

I

J

K

M

O

P

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  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- **Customer Service :**

  Email service@ameya360.com

- **Partnership :**

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com