DLP® 0.7 XGA 2xLVDS Type A DMD

Check for Samples: DLP7000

FEATURES

- 0.7-Inch Diagonal Micromirror Array
  - 1024 x 768 Array of Aluminum, Micrometer-Sized Mirrors
  - 13.68-µm Micromirror Pitch
  - ±12° Micromirror Tilt Angle (Relative to Flat State)
  - Designed for Corner Illumination
- Designed for Use With Broadband Visible Light (400 nm–700 nm):
  - Window Transmission 97% (Single Pass, Through Two Window Surfaces)
  - Micromirror Reflectivity 88%
  - Array Diffraction Efficiency 86%
  - Array Fill Factor 92%
- Two 16-Bit, Low Voltage Differential Signaling (LVDS) Double Data Rate (DDR) input data buses
- Up to 400 MHz Input Data Clock Rate
- 40.6-mm by 31.8-mm by 6.0-mm Package Footprint
- Hermetic Package

APPLICATIONS

- Industrial
  - Direct Imaging Lithography
  - Laser Marking and Repair Systems
  - Computer-to-Plate Printers
  - Rapid Prototyping Machines and 3D Printers
  - 3D Scanners for Machine Vision and Quality Control
- Medical
  - Phototherapy Devices
  - Ophthalmology
  - Vascular Imaging
  - Hyperspectral Imaging
  - 3D Scanners for Limb and Skin measurement
  - Confocal Microscopes
- Display
  - 3D Imaging Microscopes
  - Intelligent and Adaptive Lighting
  - Augmented Reality and Information Overlay

DESCRIPTION

The 0.7 XGA Chipset is part of the DLP Discovery 4100 platform, which enables high resolution and high performance spatial light modulation. The DLP7000 is the digital micromirror device (DMD) at the heart of the 0.7 XGA chipset, and currently supports the fastest pattern rates in the DLP catalog portfolio. The DLP Discovery 4100 platform also provides the highest level of individual micromirror control with the option for random row addressing. Combined with a hermetic package, the unique capability and value offered by DLP7000 makes it well suited to support a wide variety of industrial, medical, and advanced display applications.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

In addition to the DLP7000 DMD, the 0.7 XGA Chipset includes these dedicated components (see Figure 1):

- 1 unit DLPC410 (DLP Discovery 4100 Digital Controller)
- 1 unit DLPR410 / DLPR4101 (DLP Discovery 4100 Configuration PROM)
- 1 unit DLPA200 (DMD Micromirror Driver)

Reliable function and operation of the DLP7000 requires that it be used in conjunction with the other components of the chipset (see Figure 1) . A dedicated chipset provides developers easier access to the DMD as well as high speed, independent micromirror control.

DLP7000 is a digitally controlled MOEMS (micro-opto-electromechanical system) spatial light modulator (SLM). When coupled to an appropriate optical system, the DLP7000 can be used to modulate the amplitude, direction, and/or phase of incoming light.

Electrically, the DLP7000 consists of a two-dimensional array of 1-bit CMOS memory cells, organized in a grid of 1024 memory cell columns by 768 memory cell rows. The CMOS memory array is addressed on row-by-row basis, over two 16-bit Low Voltage Differential Signaling (LVDS) double data rate (DDR) buses. Addressing is handled via a serial control bus. The specific CMOS memory access protocol is handled by the DLPC410 digital controller.

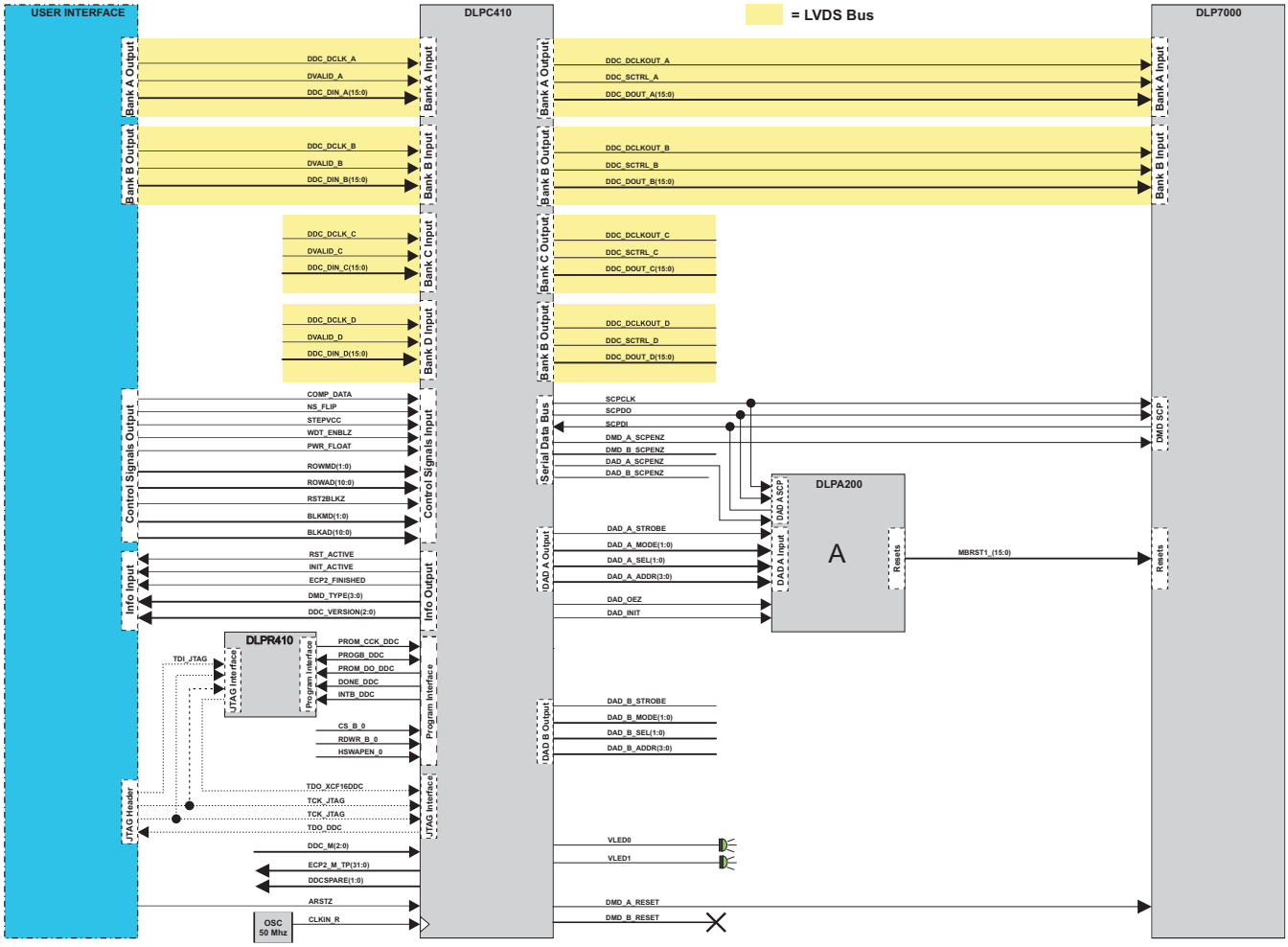


Figure 1. DLP410 and DLP7000 Functional Block Diagram

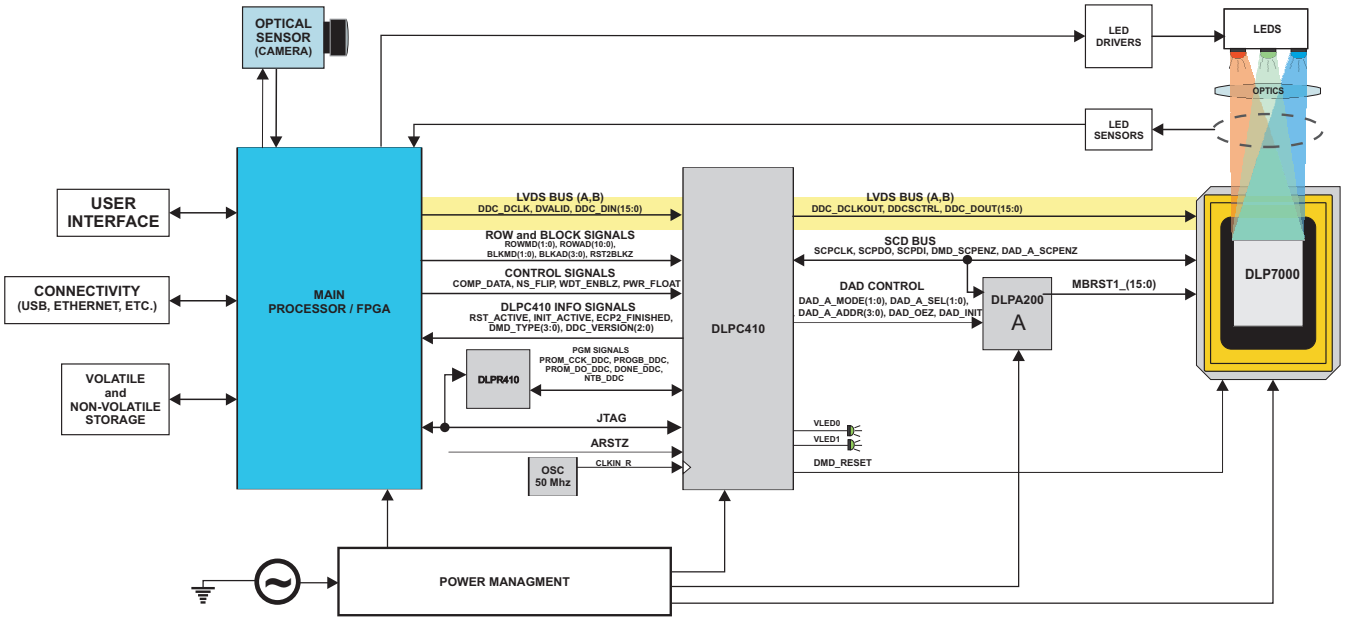


Figure 2. DLP410 and DLP7000 Embedded Example Block Diagram

Optically, the DLP7000 consists of 786,432 highly reflective, digitally switchable, micrometer-sized mirrors (“micromirrors”), organized in a two-dimensional array of 1024 micromirror columns by 768 micromirror rows (Figure 3). Each aluminum micromirror is approximately 13.68 microns in size (see the “Micromirror Pitch” in Figure 3), and is switchable between two discrete angular positions: –12° and +12°. The angular positions are measured relative to a 0° “flat state”, which is parallel to the array plane (see Figure 4). The tilt direction is perpendicular to the hinge-axis which is positioned diagonally relative to the overall array. The “On State” landed position is directed towards “Row 0, Column 0” (upper left) corner of the device package (see the “Micromirror Hinge-Axis Orientation” in Figure 3). In the field of visual displays, the 1024 by 768 “pixel” resolution is referred to as "XGA".

Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the micromirror "clocking pulse" is applied. The angular position (–12° or +12°) of the individual micromirrors changes synchronously with a micromirror “clocking pulse”, rather than being synchronous with the CMOS memory cell data update. Therefore, writing a logic 1 into a memory cell followed by a micromirror "clocking pulse" will result in the corresponding micromirror switching to a +12° position. Writing a logic 0 into a memory cell followed by a micromirror "clocking pulse" will result in the corresponding micromirror switching to a –12° position.

Updating the angular position of the micromirror array consists of two steps. First, updating the contents of the CMOS memory. Second, application of a Micromirror Clocking Pulse to all or a portion of the micromirror array (depending upon the configuration of the system). Micromirror Clocking Pulses are generated externally by a DLPA200, with application of the pulses being coordinated by the DLPC410 controller.

Around the perimeter of the 1024 by 768 array of micromirrors is a uniform band of “border” micromirrors. The border micromirrors are not user-addressable. The border micromirrors land in the –12° position once power has been applied to the device. There are 10 border micromirrors on each side of the 1024 by 768 active array.

Figure 2 shows a typical system application using the DLP Discovery 4100 chipset. The DLPC410 and DLPA200 control and coordinate the data loading and micromirror switching for reliable DLP9500 operation. The DLPR410/DLPR4101 is the programmed PROM required to properly configure the DLPC410 controller. For more information on the chipset components, see DLP Discovery 4100 chipset data sheet.

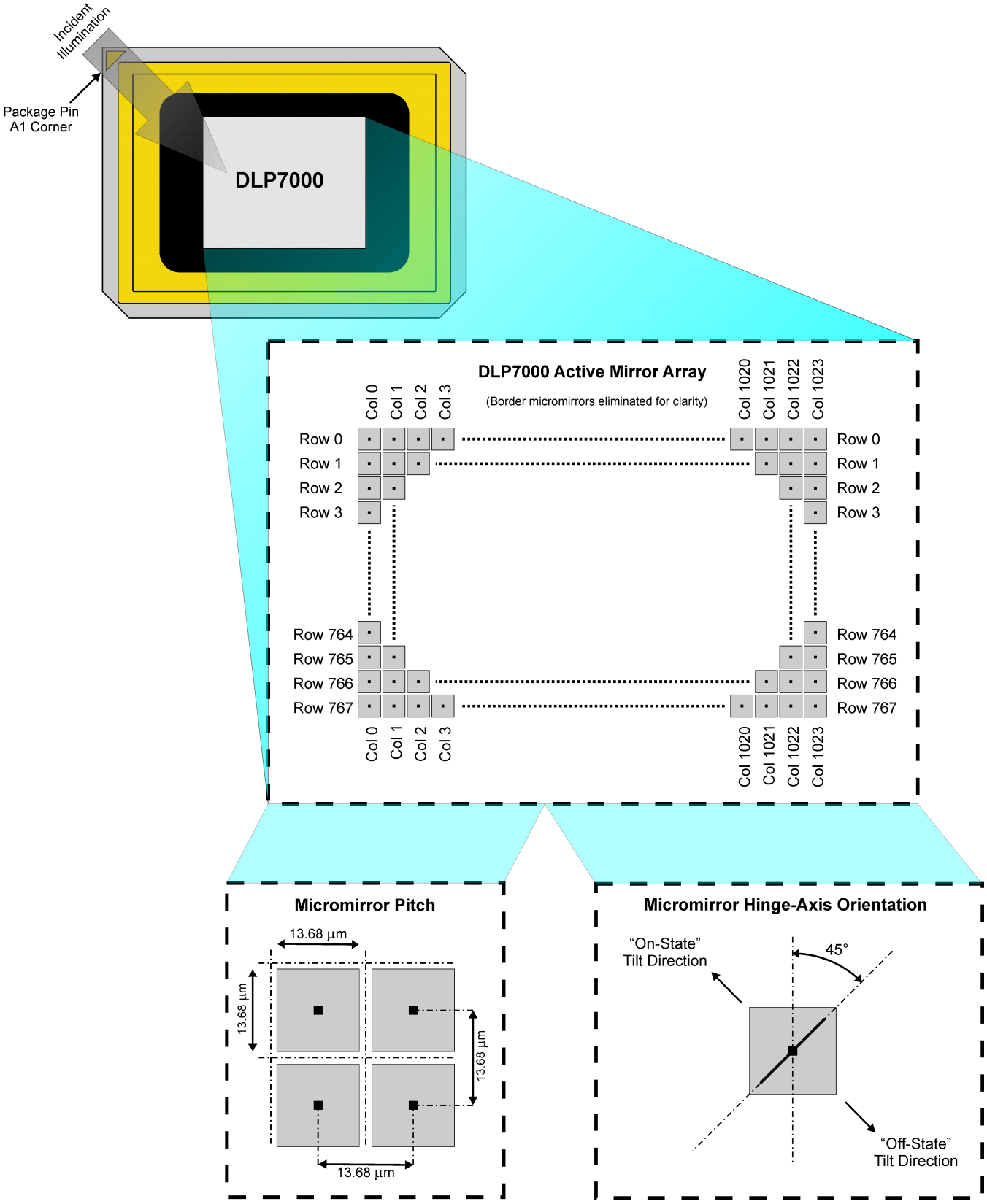


Figure 3. DMD Micromirror Array, Pitch, and Hinge-Axis Orientation

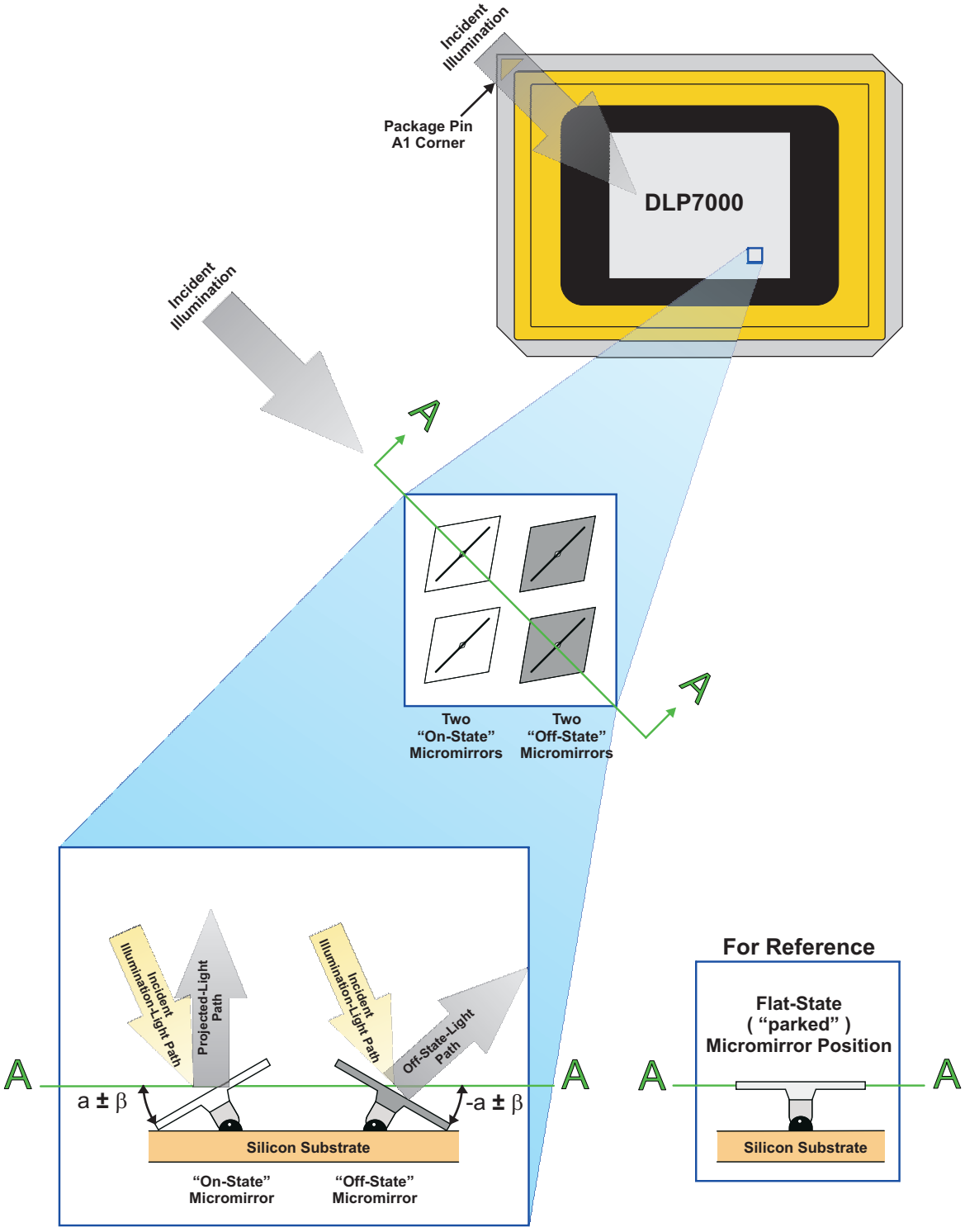


Figure 4. Micromirror Landed Positions and Light Paths

Related Documents

The following documents contain additional information related to the use of the DLP7000 device:

Table 1. Related Documentation

Document	TI Literature Number
DLP® Discovery™ 4100 Chipset Datasheet	DLPU008
DLPC410 Digital Controller data sheet	DLPS024
DLPA200 DMD Micromirror Driver data sheet	DLPS015
DLPR410 / DLPR4101 EEPROM data sheet	DLPS027

Device Part Number Nomenclature

Figure 5 provides a legend of reading the complete device name for any DLP device. DLP7000FLP is functionally equivalent to 1076N7328.

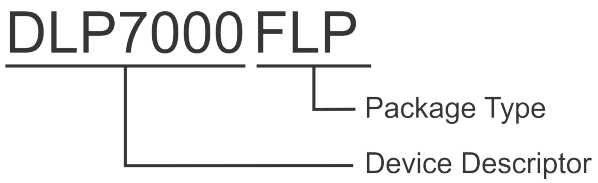


Figure 5. Device Nomenclature

Device Marking

The device marking consists of the fields shown in Figure 6.

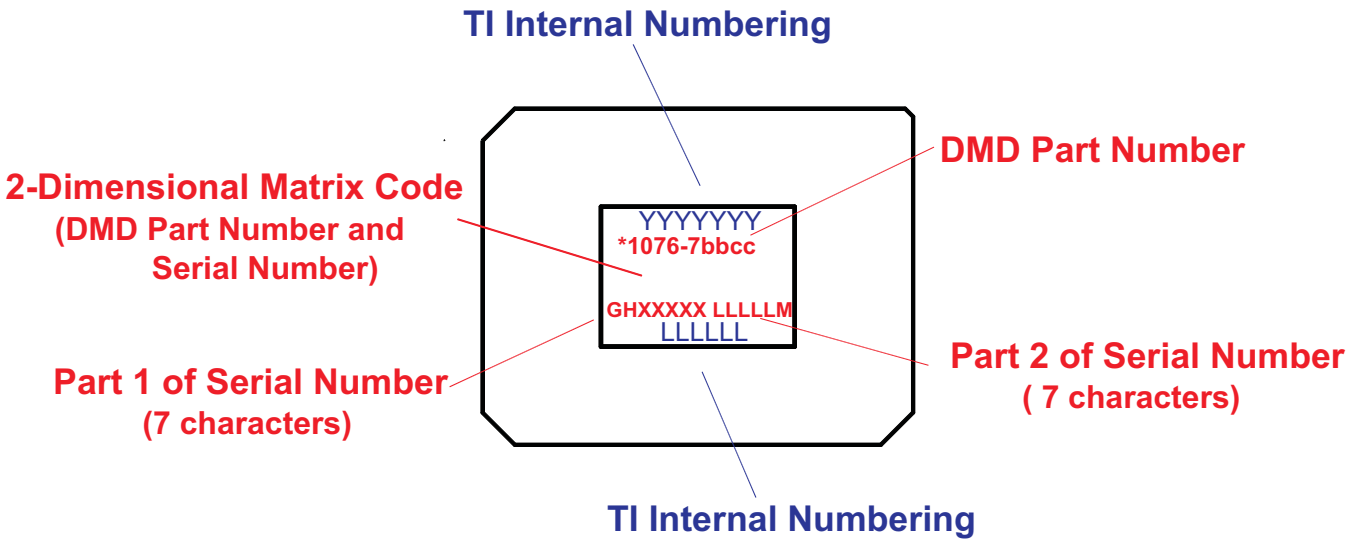


Figure 6. Device Marking

Device Terminals

This section describes the input and output characteristics of signals that interface to the DLP7000, organized by functional groups. Table 2 includes I/O, Type, Internal Termination, Clock Domain, and Data Rate characteristics which are further described in subsequent sections.

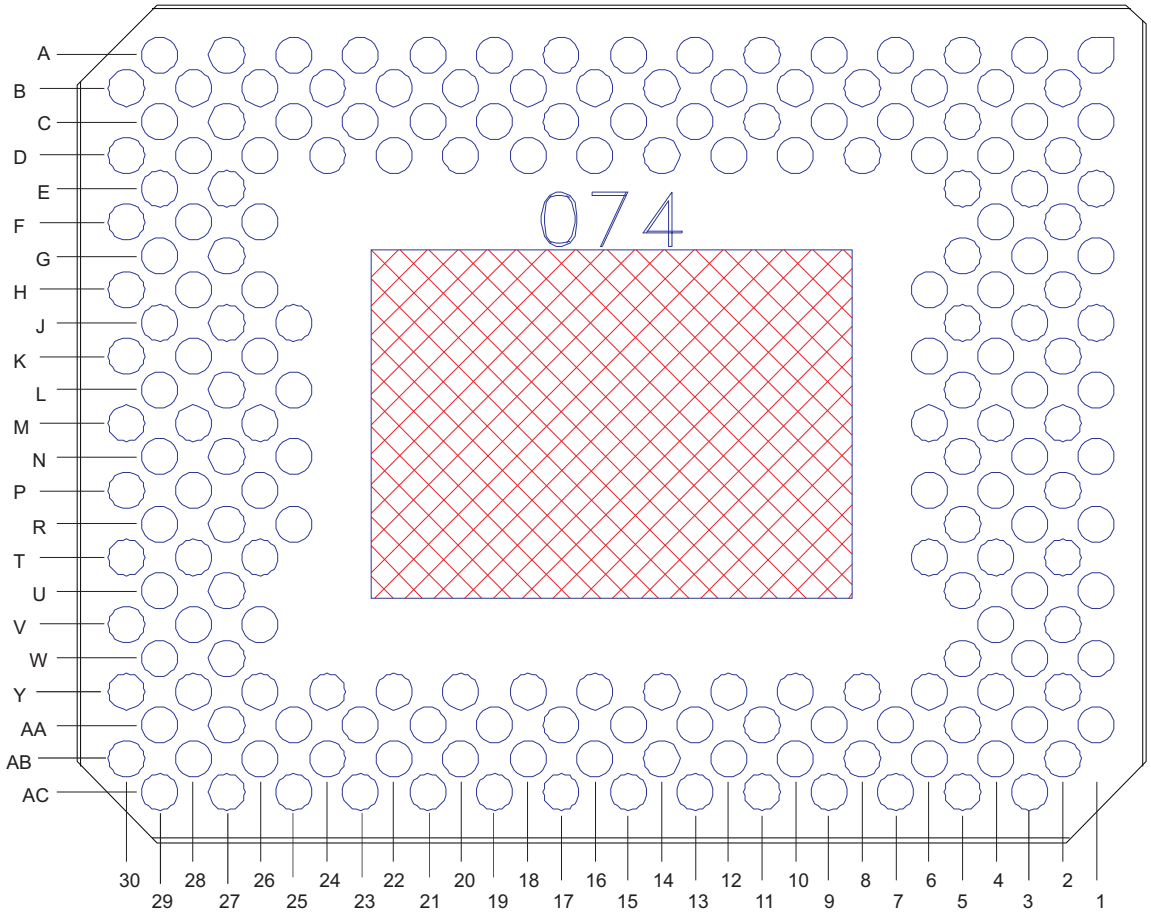


Figure 7. Type A Package Pins (Device Bottom View)

Table 2. Connector Pins

PIN NAME	PIN See Figure 7	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	Internal Trace Length (mils)	DATA RATE	DESCRIPTION
Data Inputs								
D_AN(0)	B10	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	368.72	DDR	Input data bus A (LVDS)
D_AN(1)	A13	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	424.61	DDR	
D_AN(2)	D16	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	433.87	DDR	
D_AN(3)	C17	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	391.39	DDR	
D_AN(4)	B18	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	438.57	DDR	
D_AN(5)	A17	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	391.13	DDR	
D_AN(6)	A25	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	563.26	DDR	
D_AN(7)	D22	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	411.62	DDR	
D_AN(8)	C29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	595.11	DDR	
D_AN(9)	D28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	543.07	DDR	
D_AN(10)	E27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	455.98	DDR	
D_AN(11)	F26	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	359.5	DDR	
D_AN(12)	G29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	542.67	DDR	
D_AN(13)	H28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	551.51	DDR	
D_AN(14)	J27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	528.04	DDR	
D_AN(15)	K26	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	484.38	DDR	
D_AP(0)	B12	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	366.99	DDR	Input data bus B (LVDS)
D_AP(1)	A11	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	417.47	DDR	
D_AP(2)	D14	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	434.89	DDR	
D_AP(3)	C15	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	394.67	DDR	
D_AP(4)	B16	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	437.3	DDR	
D_AP(5)	A19	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	389.01	DDR	
D_AP(6)	A23	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	562.92	DDR	
D_AP(7)	D20	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	410.34	DDR	
D_AP(8)	A29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	594.61	DDR	
D_AP(9)	B28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	539.88	DDR	
D_AP(10)	C27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	456.78	DDR	

Table 2. Connector Pins (continued)

PIN NAME	PIN See Figure 7	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	Internal Trace Length (mils)	DATA RATE	DESCRIPTION
D_AP(11)	D26	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	360.68	DDR	
D_AP(12)	F30	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	543.97	DDR	
D_AP(13)	H30	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	570.85	DDR	
D_AP(14)	J29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	527.18	DDR	
D_AP(15)	K28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	481.02	DDR	
D_BN(0)	AB10	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	368.72	DDR	
D_BN(1)	AC13	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	424.61	DDR	
D_BN(2)	Y16	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	433.87	DDR	
D_BN(3)	AA17	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	391.39	DDR	
D_BN(4)	AB18	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	438.57	DDR	
D_BN(5)	AC17	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	391.13	DDR	
D_BN(6)	AC25	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	563.26	DDR	
D_BN(7)	Y22	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	411.62	DDR	Input data bus B (LVDS)
D_BN(8)	AA29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	595.11	DDR	
D_BN(9)	Y28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	543.07	DDR	
D_BN(10)	W27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	455.98	DDR	
D_BN(11)	V26	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	360.94	DDR	
D_BN(12)	T30	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	575.85	DDR	
D_BN(13)	R29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	519.37	DDR	
D_BN(14)	R27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	532.59	DDR	
D_BN(15)	N27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	441.14	DDR	
D_BP(0)	AB12	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	366.99	DDR	
D_BP(1)	AC11	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	417.47	DDR	
D_BP(2)	Y14	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	434.89	DDR	
D_BP(3)	AA15	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	394.67	DDR	

Table 2. Connector Pins (continued)

PIN NAME	PIN See Figure 7	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	Internal Trace Length (mils)	DATA RATE	DESCRIPTION
D_BP(4)	AB16	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	437.3	DDR	Input data bus B (LVDS)
D_BP(5)	AC19	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	389.01	DDR	
D_BP(6)	AC23	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	562.92	DDR	
D_BP(7)	Y20	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	410.34	DDR	
D_BP(8)	AC29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	594.61	DDR	
D_BP(9)	AB28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	539.88	DDR	
D_BP(10)	AA27	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	456.78	DDR	
D_BP(11)	Y26	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	360.68	DDR	
D_BP(12)	U29	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	578.46	DDR	
D_BP(13)	T28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	509.74	DDR	
D_BP(14)	P28	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	534.59	DDR	
D_BP(15)	P26	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	440	DDR	
DCLK_AN	B22	Input	LVCMOS	Differential Terminated - 100 Ω	–	477.1	–	Input data bus A Clock (LVDS)
DCLK_AP	B24	Input	LVCMOS	Differential Terminated - 100 Ω	–	477.11	–	
DCLK_BN	AB22	Input	LVCMOS	Differential Terminated - 100 Ω	–	477.1	–	Input data bus B Clock (LVDS)
DCLK_BP	AB24	Input	LVCMOS	Differential Terminated - 100 Ω	–	477.11	–	
Data Control Inputs								
SCTRL_AN	C21	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	477.07	DDR	Serial control for data bus A (LVDS)
SCTRL_AP	C23	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_A	477.14	DDR	
SCTRL_BN	AA21	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	477.07	DDR	Serial control for data bus B (LVDS)
SCTRL_BP	AA23	Input	LVCMOS	Differential Terminated - 100 Ω	DCLK_B	477.14	DDR	
Serial Communication and Configuration								
SCPCLK	E3	Input	LVCMOS	pull-down	–	379.29	–	Serial port clock
SCPDO	B2	Output	LVCMOS	–	SCPCLK	480.91	–	Serial port output
SCPDI	F4	Input	LVCMOS	pull-down	SCPCLK	323.56	–	Serial port input
SCPENZ	D4	Input	LVCMOS	pull-down	SCPCLK	326.99	–	Serial port enable
PWRDNZ	C3	Input	LVCMOS	pull-down	–	406.28	–	Device Reset
MODE_A	D8	Input	LVCMOS	pull-down	–	396.05	–	Data bandwidth mode select
MODE_B	C11	Input	LVCMOS	pull-down	–	208.86	–	

Table 2. Connector Pins (continued)

PIN NAME	PIN See Figure 7	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	Internal Trace Length (mils)	DATA RATE	DESCRIPTION
Micromirror Bias Reset								
MBRST(0)	P2	Input	Analog	–	–	1225.87	–	Micromirror Bias Reset "MBRST" signals "clock" micromirrors into state of LVCMOS memory cell associated with each mirror.
MBRST(1)	AB4	Input	Analog	–	–	1277.24	–	
MBRST(2)	AA7	Input	Analog	–	–	1306.01	–	
MBRST(3)	N3	Input	Analog	–	–	926.71	–	
MBRST(4)	M4	Input	Analog	–	–	1092.91	–	
MBRST(5)	AB6	Input	Analog	–	–	1238.86	–	
MBRST(6)	AA5	Input	Analog	–	–	1186.57	–	
MBRST(7)	L3	Input	Analog	–	–	941.2	–	
MBRST(8)	Y6	Input	Analog	–	–	458.84	–	
MBRST(9)	K4	Input	Analog	–	–	813.88	–	
MBRST(10)	L5	Input	Analog	–	–	742.95	–	
MBRST(11)	AC5	Input	Analog	–	–	824.02	–	
MBRST(12)	Y8	Input	Analog	–	–	377.26	–	
MBRST(13)	J5	Input	Analog	–	–	876.96	–	
MBRST(14)	K6	Input	Analog	–	–	753.35	–	
MBRST(15)	AC7	Input	Analog	–	–	749.82	–	
Power								
VCC	A7,A15,C1,E1,U1,W1,AB2,AC9,AC15	Power	Analog	–	–	–	–	Power for LVCMOS Logic
VCC1	A21,A27,D30,M30,Y30,AC21,AC27	Power	Analog	–	–	–	–	Power supply for LVDS Interface
VCC2	G1,J1,L1,N1,R1	Power	Analog	–	–	–	–	Power for High Voltage CMOS Logic
VSS	A1,A3,A5,A9,B4,B8,B14,B20,B26,B30,C7,C13,C19,C25,D6,D12,D18,D24,E29,F2,F28,G3,G27,H2,H4,H26,J3,J25,K2,K30,L25,L27,L29,M2,M6,M26,M28,N5,N25,N29,P4,P30,R3,R5,R25,T2,T26,U27,V28,V30,W5,W29,Y4,Y12,Y18,Y24,AA3,AA9,AA13,AA19,AA25,AB8,AB14,AB20,AB26,AB30	Power	Analog	–	–	–	–	Common return for all power inputs
Reserved Signals (Not for use in system)								
RESERVED_AA1	AA1	input	LVCMOS	pull-down	–	–	–	Pins should be connected to VSS
RESERVED_B6	B6	input	LVCMOS	pull-down	–	–	–	
RESERVED_T4	T4	input	LVCMOS	pull-down	–	–	–	
RESERVED_U5	U5	input	LVCMOS	pull-down	–	–	–	
NO_CONNECT	AA11,AC3,C5,C9,D10,D2,E5,G5,H6,P6,T6,U3,V2,V4,W3,Y10,Y2	–	–	–	–	–	–	DO NOT CONNECT

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. The Absolute Maximum Ratings are stress ratings only, and functional performance of the device at these or any other conditions beyond those indicated under " Recommended Operating Conditions" is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Electrical						
V_{CC}	Voltage applied to V_{CC} (1) (2)		–0.5		4	V
V_{CCI}	Voltage applied to V_{CCI} (1) (2)		–0.5		4	V
	Delta supply voltage $\lvert V_{CC} - V_{CCI} \rvert$ (3)				0.3	V
$\lvert V_{ID} \rvert$	Maximum differential voltage, Damage can occur to internal termination resistor if exceeded, See Figure 11				700	mV
V_{CC2}	Voltage applied to V_{VCC2} (1) (2) (3)		–0.5		9	V
V_{MBRST}	Micromirror Clocking Pulse Waveform Voltage applied to MBRST[15:0] Input Pins (supplied by DLPA200)		-28		28	V
	Voltage applied to all other input terminals (1)		–0.5		V_{CC} + 0.3	V
	Current required from a high-level output	V_{OH} = 2.4 V			–20	mA
	Current required from a low-level output	V_{OL} = 0.4 V			15	mA
Environmental						
	Storage temperature range		-40		80	°C
	Storage humidity	Non-Condensing	0		95	% RH
	Electrostatic discharge immunity for LVCMOS pins (4)				2000	V
	Electrostatic discharge immunity for MBRST[15:0] pins				250	

(1) All voltages referenced to V_{SS} (ground).
(2) Voltages V_{CC}, V_{CCI}, and V_{CC2} are required for proper DMD operation.
(3) Exceeding the recommended allowable absolute voltage difference between V_{CC} and V_{CCI} may result in excess current draw. The difference between V_{CC} and V_{CCI}, $\lvert V_{CC} - V_{CCI} \rvert$, should be less than 0.3 V.
(4) Tested in accordance with JESD22-A114-B Electrostatic Discharge (ESD) sensitivity testing Human Body Model (HBM).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

PARAMETER			CONDITIONS	MIN	NOM	MAX	UNIT
Electrical							
V_{CC}	LVCMOS interface supply voltage(1)(2)			3.0	3.3	3.6	V
V_{CCI}	LVCMOS logic supply voltage(1)(2)			3.0	3.3	3.6	V
V_{CC2}	Mirror electrode and HVCMOS supply voltage (1)(2)			7.25	7.5	7.75	V
V_{MBRST}	Clocking Pulse Waveform Voltage applied to MBRST[29:0] Input Pins (supplied by DLPA200s)			-27		26.5	V
Mechanical							
	Static load applied to electrical interface area, See (3) Figure 8					423	N
	Static load applied to the thermal interface area, See(4) Figure 8					111	N
	Static load applied to Datum "A" interface area Figure 8					400	N
Environmental							
	Illumination power density(5)(6)		< 400 nm(7)			2	mW/cm^2
			400 to 700 nm(8)		see table notes	25	W/cm^2
			> 700 nm			10	mW/cm^2
T_C	Operating Case Temperature	Thermal Test Points 1 and 2(9)	Operating Case Temperature(9)(10)	10	25-45	65 (9)	°C
		Thermal Test Point 3 and Array(9)				65 (9)	
	Operating Device Temperature Gradient		Gradient between any two points on the package(9)			10	°C
	Operating Humidity(5)		Non-Condensing			95	%RH
	Operating Landed Duty Cycle(11)				25		%

(1) All voltages referenced to V_{SS} (ground).
(2) Voltages V_{CC}, V_{CCI}, and V_{CC2}, are required for proper DMD operation.
(3) Load should be uniformly distributed across the entire Electrical Interface area number 1 and number 2.
(4) Load should be uniformly distributed across Thermal Interface Area. Refer to the for size and location of the datum-A surfaces.
(5) Optimal, long-term performance of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty cycle, ambient temperature (both storage and operating), case temperature, and power on/off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle. Contact your local Texas Instruments representative for additional information related to optimizing the DMD performance.
(6) Total integrated illumination power density, above or below the indicated wavelength threshold.
(7) The maximum operating conditions for operating temperature and illumination power density for wavelengths < 400 nm shall not be implemented simultaneously.
(8) Also Limited by the resulting micromirror array temperature. See the Thermal Characteristics for information related to calculating the micromirror array temperature.
(9) See the for Thermal Test Point Locations, Package Thermal Resistance, and Device Temperature Calculation.
(10) In some applications, the total DMD heat load can be dominated by the amount of incident light energy absorbed. See the Thermal Characteristics for further details.
(11) "Landed Duty-Cycle" refers to the percentage of time an individual micromirror spends landed in one state (+12° or -12°) versus the other state (-12° or +12°).

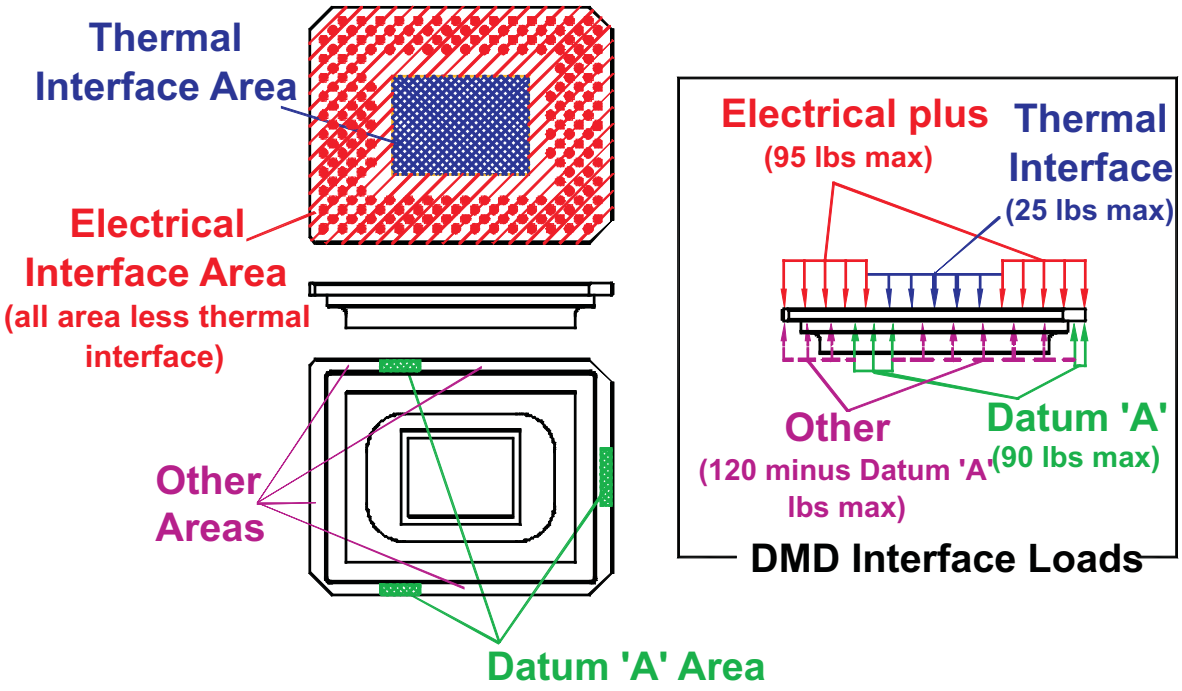


Figure 8. System Interface Loads

ELECTRICAL CHARACTERISTICS

Over the range of recommended supply voltage and recommended case operating temperature (unless otherwise noted)

PARAMETERS (Under RECOMMENDED OPERATING CONDITIONS)		TEST CONDITIONS		MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage(1), See Figure 9	V_{CC} = 3.0 V,	I_{OH} = –20 mA	2.4			V
V_{OL}	Low-level output voltage(1), See Figure 9	V_{CC} = 3.6 V,	I_{OH} = 15 mA			0.4	V
V_{MBRST}	Clocking Pulse Waveform applied to MBRST[29:0] Input Pins (supplied by DLPA200s)			-27		26.5	V
I_{OZ}	High impedance output current(1)	V_{CC} = 3.6 V				10	µA
I_{OH}	High-level output current (1)	V_{OH} = 2.4 V, V_{CC} ≥ 3 V				–20	mA
		V_{OH} = 1.7 V, V_{CC} ≥ 2.25 V				–15	
I_{OL}	Low-level output current (1)	V_{OL} = 0.4 V, V_{CC} ≥ 3 V				15	mA
		V_{OL} = 0.4 V, V_{CC} ≥ 2.25 V				14	
V_{IH}	High-level input voltage(1)			1.7		VCC + .3	V
V_{IL}	Low-level input voltage(1)			-0.3		0.7	V
I_{IL}	Low-level input current(1)	V_{CC} = 3.6 V,	V_I = 0 V			–60	µA
I_{IH}	High-level input current(1)	V_{CC} = 3.6 V,	V_I = V_{CC}			200	µA
I_{CC}	Current into V_{CC} pin	V_{CC} = 3.6 V,				1475	mA
I_{CCI}	Current into V_{CCI} pin (2)	V_{CCI} = 3.6 V				450	mA
I_{CC2}	Current into V_{CC2} pin	V_{CC2} = 8.75V				25	mA
Z_{IN}	Internal Differential Impedance			95		105	Ohms
Z_{LINE}	Line Differential Impedance (PWB, Trace)			90	100	110	Ohms
C_I	Input capacitance (1)	f = 1 MHz				10	pF
C_O	Output capacitance (1)	f = 1 MHz				10	pF
C_{IM}	Input capacitance for MBRST[29:0] pins	f = 1 MHz		220		270	pF

(1) Applies to LVCMOS pins only.
(2) Exceeding the maximum allowable absolute voltage difference between V_{CC} and V_{CCI} may result in excess current draw. (See the Absolute Maximum Ratings for details)

Measurement Conditions

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Figure 9 shows an equivalent test load circuit for the output under test. The load capacitance value stated is only for characterization and measurement of ac timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving. All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL} MAX and V_{OH} MIN for output clocks.

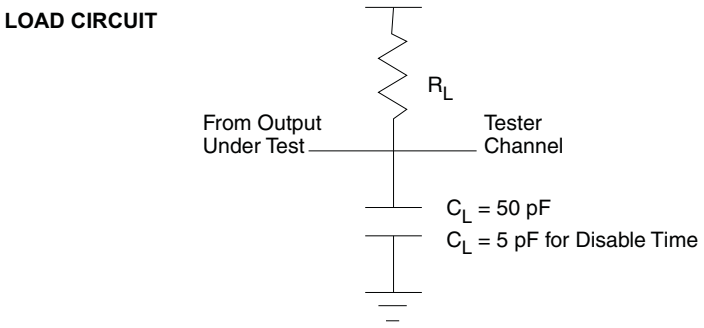


Figure 9. Test Load Circuit for AC Timing Measurements

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

LVDS TIMING PARAMETERS See		MIN	NOM	MAX	UNIT
f_{DCLK_*}	DCLK_* clock frequency {where * = [A, or B]}	200		400	MHz
t_c	Clock Cycle - DLCK_*	2.5			ns
t_w	Pulse Width - DLCK_*		1.25		ns
t_s	Setup Time - D_*[15:0] and SCTRL_* before DCLK_*	.35			ns
t_h	Hold Time, D_*[15:0] and SCTRL_* after DCLK_*	.35			ns
t_{skew}	Skew between bus A and B	-1.25		1.25	ns

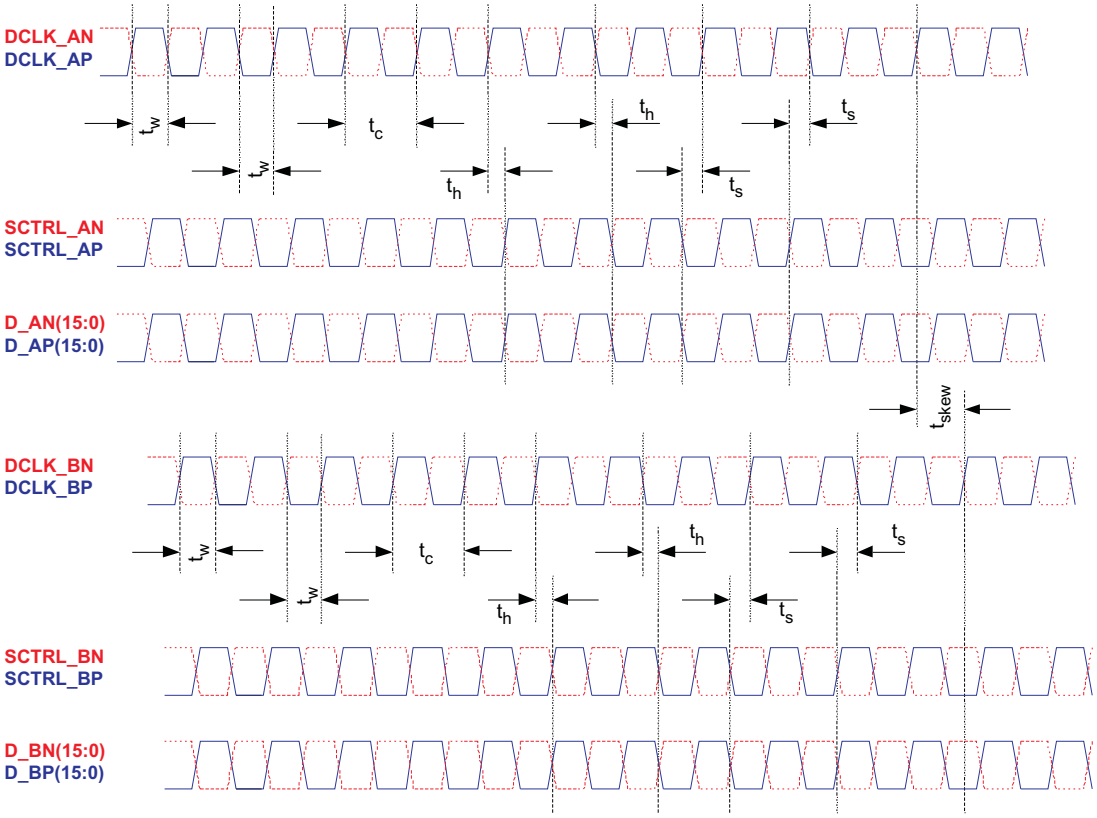


Figure 10. LVDS Timing Waveforms

SWITCHING CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

LVDS Waveform Requirements See		MIN	NOM	MAX	UNIT
$\|V_{ID}\|$	Input Differential Voltage (absolute difference)	100	400	600	mV
V_{CM}	Common Mode Voltage		1200		mV
V_{LVDS}	LVDS Voltage	0		2000	mV
t_r	Rise Time (20% to 80%)	100		400	ps
t_r	Fall Time (80% to 20%)	100		400	ps

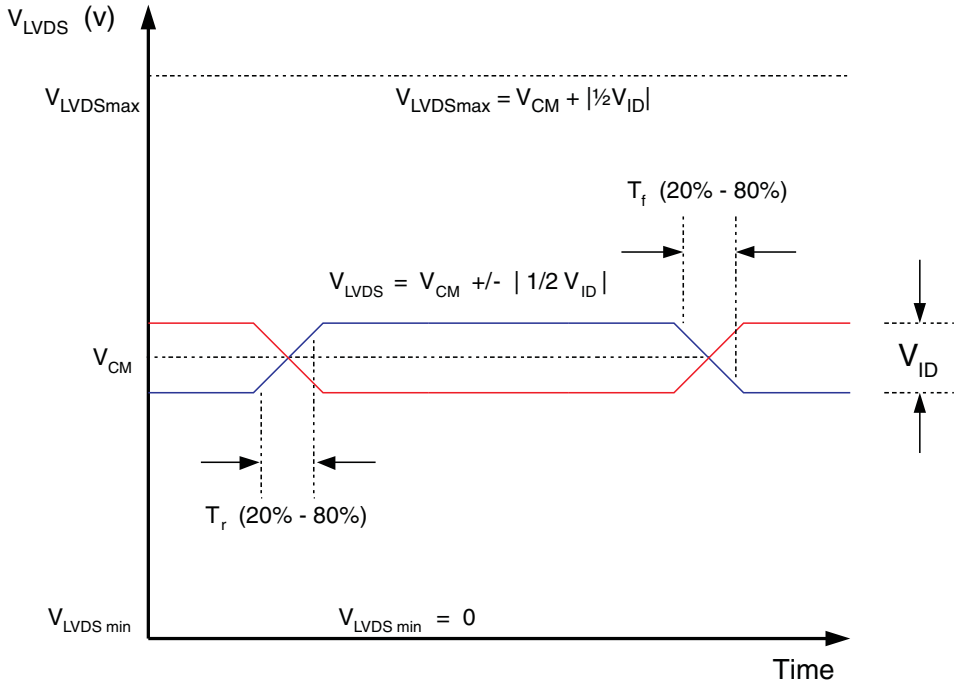


Figure 11. LVDS Waveform Requirements

SWITCHING CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

Serial Control Bus Timing Parameters See and		MIN	NOM	MAX	UNIT
f_{SCP_CLK}	SCP Clock Frequency	50		500	KHz
t_{SCP_SKEW}	Time between valid SCP_DI and rising edge of SCP_CLK	-300		300	ns
t_{SCP_DELAY}	Time between valid SCP_DO and rising edge of SCP_CLK			960	ns
t_{SCP_ENZ}	Time between falling edge of SCP_ENZ and the first rising edge of SCP_CLK	30			ns
$t_{\_SCP}$	Rise time for SCP signals			200	ns
t_{f_SCP}	Fall time for SCP signals			200	ns

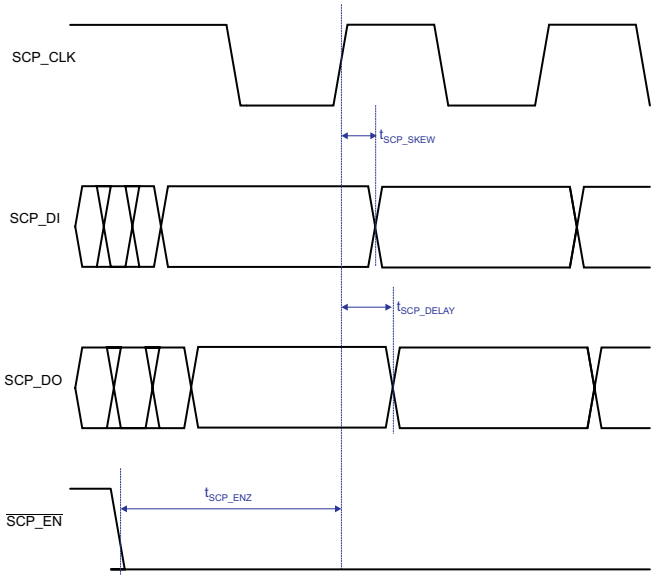


Figure 12. Serial Communications Bus Timing Parameters

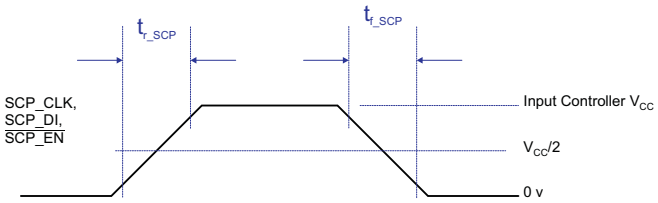


Figure 13. Serial Communications Bus Waveform Requirements

DMD Power-Up and Power-Down Procedures

Repeated failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. The DLP7000 power-up and power-down procedures are defined by the DLPC410 data sheet (TI Literature number DLPS024) and the DLP Discovery Chipset Data sheet (TI Literature number DLPU008). These procedures must be followed to ensure reliable operation of the device.

Micromirror Array Physical Characteristics

Physical characteristics of the micromirror array are provided in . Additional details are provided in the **Package Mechanical Characteristics** section at the end of this document.

Table 3. Micromirror Array Physical Characteristics

PARAMETER	VALUE	UNITS
Number of active micromirror columns (1)	1024	micromirrors
Number of active micromirror rows (1)	768	micromirrors
Micromirror pitch (1)	13.68	microns
Micromirror active array height (1)	768	micromirrors
	11.664	millimeters
Micromirror active array width (1)	1024	micromirrors
	20.736	millimeters
Micromirror array border (2)	10	mirrors/side

(1) See
(2) The mirrors that form the array border are hard-wired to tilt in the –12° (“Off”) direction once power is applied to the DMD (see and).

Micromirror Array Optical Characteristics

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-off’s between numerous component and system design parameters. See the related application reports (listed in Related Documents) for guidelines.

Table 4. Micromirror Array Optical Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
α	Micromirror tilt angle	DMD “parked” state (1)(2)(3), See Figure 4		0		degrees
		DMD “landed” state (1)(4)(5) See Figure 4		12		
β	Micromirror tilt angle variation (1)(4)(6)(7)(8)	See Figure 4	–1		1	degrees
	Micromirror Cross Over Time (9)			16	22	us
	Micromirror Switching Time (10)			140		us
	Non Operating micromirrors (11)	Non-adjacent micromirrors			10	micromirrors
		adjacent micromirrors			0	
	Orientation of the micromirror axis-of-rotation (12)	See Figure 3	44	45	46	degrees
	Micromirror array optical efficiency (13)(14)	400 nm to 700 nm, with all micromirrors in the ON state		68%		
	Window material			Corning 7056		
	Window refractive index	at 545 nm		1.487		
	Window flatness (15)	Per 25 mm			4	fringes
	Window Artifact Size	Within the Window Aperture (16)			400	um
	Window aperture			See (16)		

(1) Measured relative to the plane formed by the overall micromirror array
(2) “Parking” the micromirror array returns all of the micromirrors to an essentially flat (0˚) state (as measured relative to the plane formed by the overall micromirror array).
(3) When the micromirror array is “parked”, the tilt angle of each individual micromirror is uncontrolled.
(4) Additional variation exists between the micromirror array and the package datums, as shown in the **Package Mechanical Characteristics** section at the end of this document.
(5) When the micromirror array is “landed”, the tilt angle of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of “1” will result in a micromirror “landing” in an nominal angular position of “+12 degrees”. A binary value of 0 results in a micromirror “landing” in an nominal angular position of “-12 degrees”.
(6) Represents the “landed” tilt angle variation relative to the Nominal “landed” tilt angle.
(7) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.

(8) For some applications, it is critical to account for the micromirror tilt angle variation in the overall System Optical Design. With some System Optical Designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some System Optical Designs, the micromirror tilt angle variation between devices may result in colorimetry variations and/or system contrast variations.

(9) Micromirror Cross Over time is primarily a function of the natural response time of the micromirrors.

(10) Micromirror switching is controlled and coordinated by the DLPC410 (TI Literature number DLPS024) AND DLPA200 (TI Literature number DLPS015). Nominal Switching time depends on the system implementation and represents the time for the entire micromirror array to be refreshed.

(11) Non-operating micromirror is defined as a micromirror that is unable to transition nominally from the -12 degree position to +12 degree or vice versa.

(12) Measured relative to the package datums “B” and “C”, shown in the **Package Mechanical Characteristics** section at the end of this document.

(13) The minimum or maximum DMD optical efficiency observed in a specific application depends on numerous application-specific design variables, such as:

- Illumination wavelength, bandwidth/line-width, degree of coherence
- Illumination angle, plus angle tolerance
- Illumination and projection aperture size, and location in the system optical path
- Illumination overfill of the DMD micromirror array
- Aberrations present in the illumination source and/or path
- Aberrations present in the projection path
- Etc.

The specified nominal DMD optical efficiency is based on the following use conditions:

- Visible illumination (400 nm – 700 nm)
- Input illumination optical axis oriented at 24° relative to the window normal
- Projection optical axis oriented at 0° relative to the window normal
- f/3.0 illumination aperture
- f/2.4 projection aperture

Based on these use conditions, the nominal DMD optical efficiency results from the following four components:

- Micromirror array fill factor: nominally 92%
- Micromirror array diffraction efficiency: nominally 86%
- Micromirror surface reflectivity: nominally 88%
- Window transmission: nominally 97% (single pass, through two surface transitions)

(14) Does not account for the effect of micromirror switching duty cycle, which is application dependant. Micromirror switching duty cycle represents the percentage of time that the micromirror is actually reflecting light from the optical illumination path to the optical projection path. This duty cycle depends on the illumination aperture size, the projection aperture size, and the micromirror array update rate.

(15) At a wavelength of 632.8nm.

(16) See the **Package Mechanical Characteristics** section at the end of this document for details regarding the size and location of the window aperture.

Thermal Characteristics

Achieving optimal DMD performance requires proper management of the maximum DMD case temperature, the maximum temperature of any individual micromirror in the active array, the maximum temperature of the window aperture, and the temperature gradient between case temperature and the predicted micromirror array temperature. (see Figure 14).

See the RECOMMEND OPERATING CONDITIONS for applicable temperature limits.

Package Thermal Resistance

The DMD is designed to conduct absorbed and dissipated heat to the back of the Type A package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the specified operational temperatures, refer to Figure 14. The total heat load on the DMD is typically driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.

Package Thermal Resistance

	Min	Nom	Max	Units
Active Micromirror Array resistance to TC2			0.9	ºC/W

Case Temperature

The temperature of the DMD case can be measured directly. For consistency, a Thermal Test Point locations TC1 and TC2 are defined, as shown in Figure 14.

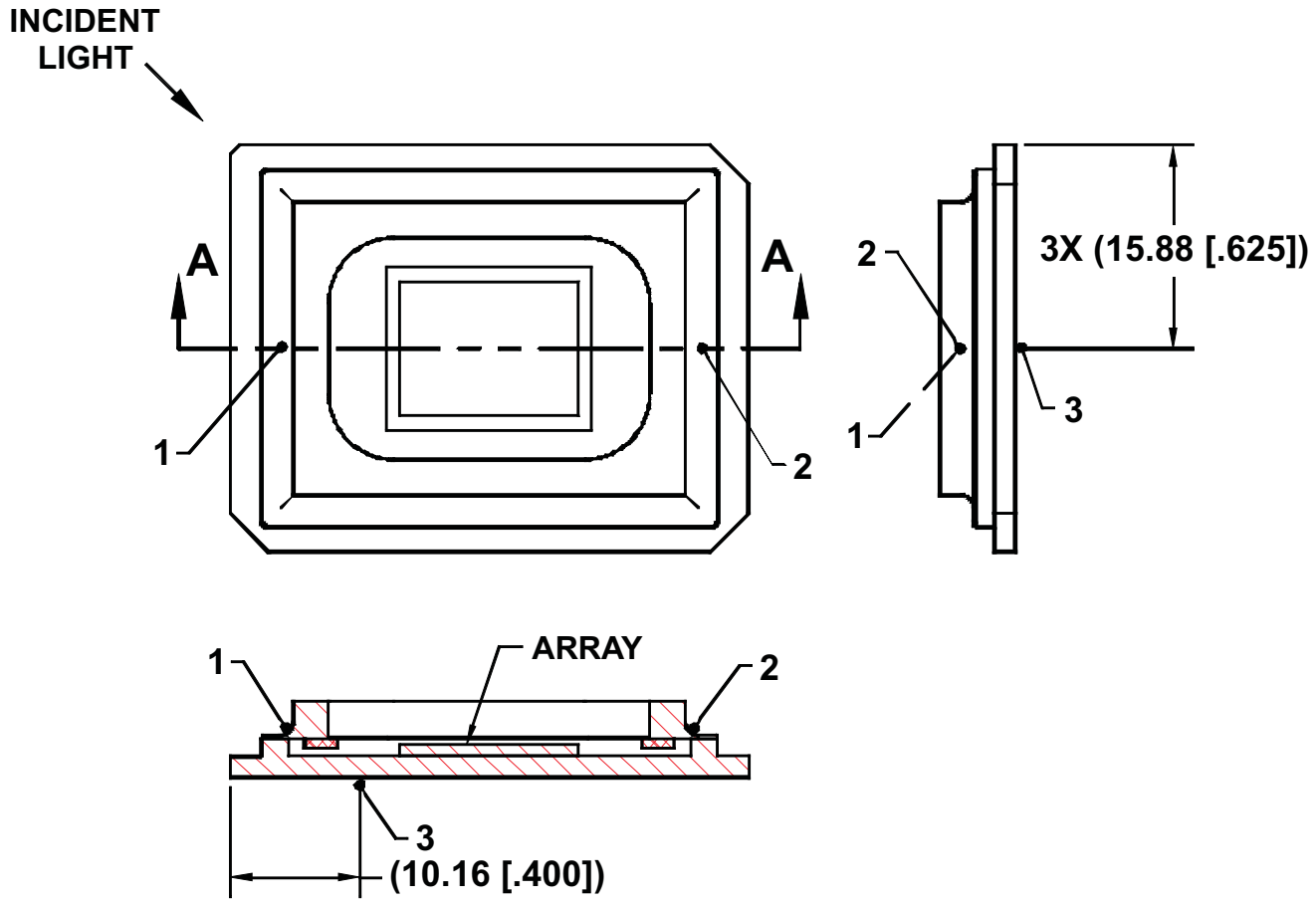


Figure 14. Thermal Test Point Location

Micromirror Array Temperature Calculation

Micromirror array temperature cannot be measured directly; therefore, it must be computed analytically from measurement points (Figure 14), the package thermal resistance, the electrical power, and the illumination heat load. The relationship between micromirror array temperature and the case temperature are provided by Equation 1 and Equation 2:

$$T_{Array} = T_{Ceramic} + (Q_{Array} \times R_{Array\text{-}To\text{-}Ceramic}) \quad (1)$$

$$Q_{Array} = Q_{ELE} + Q_{ILL} \quad (2)$$

Where the following elements are defined as:

T_{Array} = computed micromirror array temperature (°C)

$T_{Ceramic}$ = Ceramic temperature (°C) (TC2 Location Figure 14)

Q_{Array} = Total DMD array power (electrical + absorbed) (measured in Watts)

$R_{Array\text{-}To\text{-}Ceramic}$ = thermal resistance of DMD package from array to TC2 (°C/Watt) (see Package Thermal Resistance)

Q_{ELE} = Nominal electrical power (Watts)

Q_{ILL} = Absorbed illumination energy (Watts)

An example calculation is provided below based on a traditional DLP Video projection system. The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. The nominal electrical power dissipation to be used in the calculation is 2 Watts. Thus, Q_{ELE} = 2 Watts. The absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source. Based on modeling and measured data from DLP projection system $Q_{ILL} = C_{L2W} \times SL$.

Where:

C_{L2W} is a Lumens to Watts constant, and can be estimated at 0.00274 Watt/Lumen

SL = Screen Lumens nominally measured to be 2000 lumens

Qarray = 2.0 + (0.00274 x 2000) = 7.48 watts, Estimated total power on micromirror Array

$T_{Ceramic}$ = 55°C, assumed system measurement

Finally, T_{Array} (micromirror active array temperature) is

T_{Array}= 55°C + (7.48 watts x 0.9°C/watt) = **61.7°C**

REVISION HISTORY

Changes from Original (August 2012) to Revision A **Page**

- Changed the device From: Product Preview To: Production 1

Changes from Revision A (September 2012) to Revision B **Page**

- Added / DLPR4101 Enhanced PROM to DLPR410 in Chipset List 2
- Added / DLPR4101 Enhanced PROM to DLPR410 in Related Documentation 6
- Changed pin number of DCLK_AN From: D19 To: B22 10
- Changed pin number of DCLK_AP From: E19 To: B24 10
- Changed pin number of DCLK_BN From: M19 To: AB22 10
- Changed pin number of DCLK_BP From: N19 To: AB24 10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DLP7000FLP	ACTIVE	LCCC	FLP	203	3	Green (RoHS & no Sb/Br)	W NIAU	N / A for Pkg Type			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

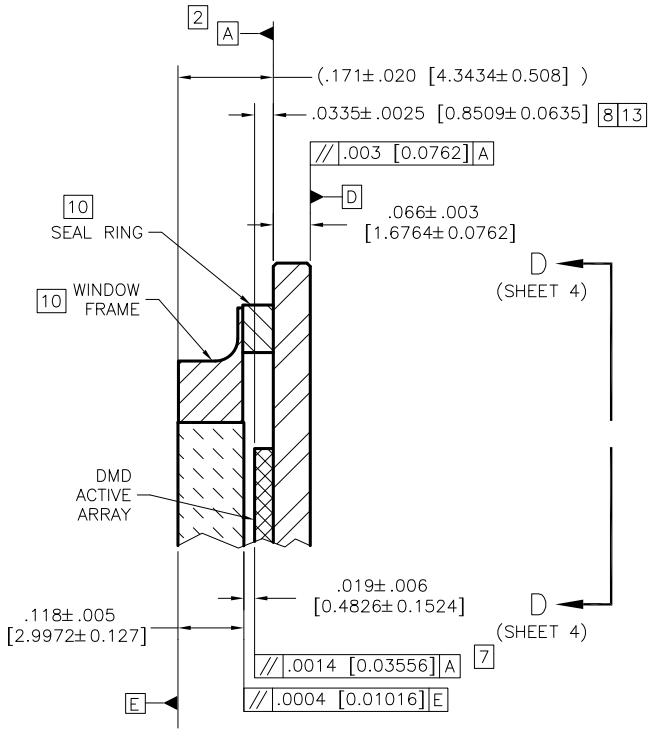
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

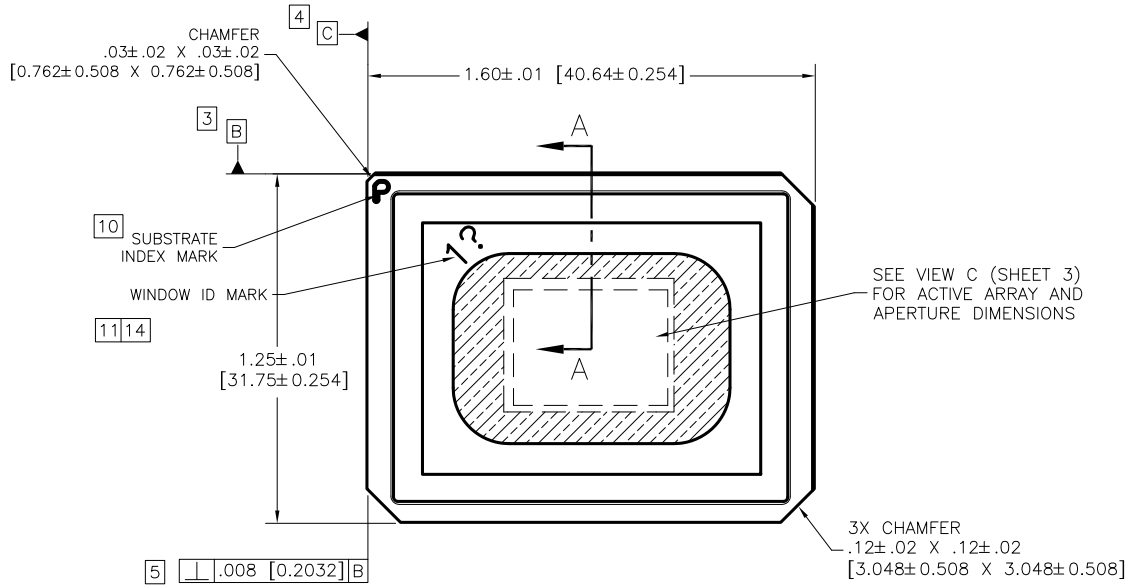
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2071155, INITIAL RELEASE	07/24/06	MRW
B	ECO 2077187, CHG DESG FROM 29	02/19/07	MRW

NOTES: UNLESS OTHERWISE SPECIFIED:

1. INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M–1994.
2. DATUM A (SYSTEM INTERFACE PLANE) ESTABLISHED BY THREE DATUM AREAS SHOWN IN VIEW B (SHEET 2).
3. DATUM B ESTABLISHED BY TWO DATUM AREAS SHOWN IN VIEW B (SHEET 2).
4. DATUM C ESTABLISHED BY DATUM AREA SHOWN IN VIEW B (SHEET 2).
5. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
6. LOCALIZED BACKSIDE SURFACE FLATNESS APPLIES TO ENTIRE CERAMIC SURFACE.
7. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
8. DIE HEIGHT TOLERANCE APPLIES TO CENTER OF DMD ACTIVE ARRAY ONLY.
9. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND IS THE MAXIMUM VALUE ALLOWED.
10. SUBSTRATE INDEX MARK, SYMBOLIZATION PAD, SEAL RING, AND WINDOW FRAME TO BE ELECTRICALLY CONNECTED TO VSS PLANE IN SUBSTRATE.
11. WINDOW SHALL BE ORIENTED SUCH THAT WINDOW ID MARK ALIGNS WITH SUBSTRATE INDEX MARK AS SHOWN.
12. THE OUTER DIMENSIONS OF THE SYMBOLIZATION PAD REPRESENT THE APPROXIMATE SIZE AND LOCATION OF THE RECOMMENDED THERMAL INTERFACE AREA.
13. DMD ACTIVE ARRAY DIMENSIONS ARE RELATED TO DATUM A (PRIMARY), DATUM B (SECONDARY), AND DATUM C (TERTIARY).
14. ? IS A WILD CARD CHARACTER AND CAN BE ANY LETTER.



SECTION A–A
SCALE 6/1



–1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES [MILLIMETERS]
- TOLERANCES: ANGLES ± 1°
  3 PLACE DECIMALS ±.005 [0.127]
  2 PLACE DECIMALS ±.01 [0.254]
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- ~~CONCENTRICITY MACHINED DIAMETERS .010 FIM~~
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125 +.004 −.001	.126 THRU .250 +.005 −.001	.251 THRU .500 +.006 −.001
.501 THRU .750 +.008 −.001	.751 THRU 1.000 +.010 −.001	1.001 THRU 2.000 +.012 −.001

THIRD ANGLE PROJECTION

NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

DWN M.WILLIAMS 07/12/06
ENGR A. ARAYATA 07/12/06
QA
APVD

TEXAS INSTRUMENTS
Dallas, Texas

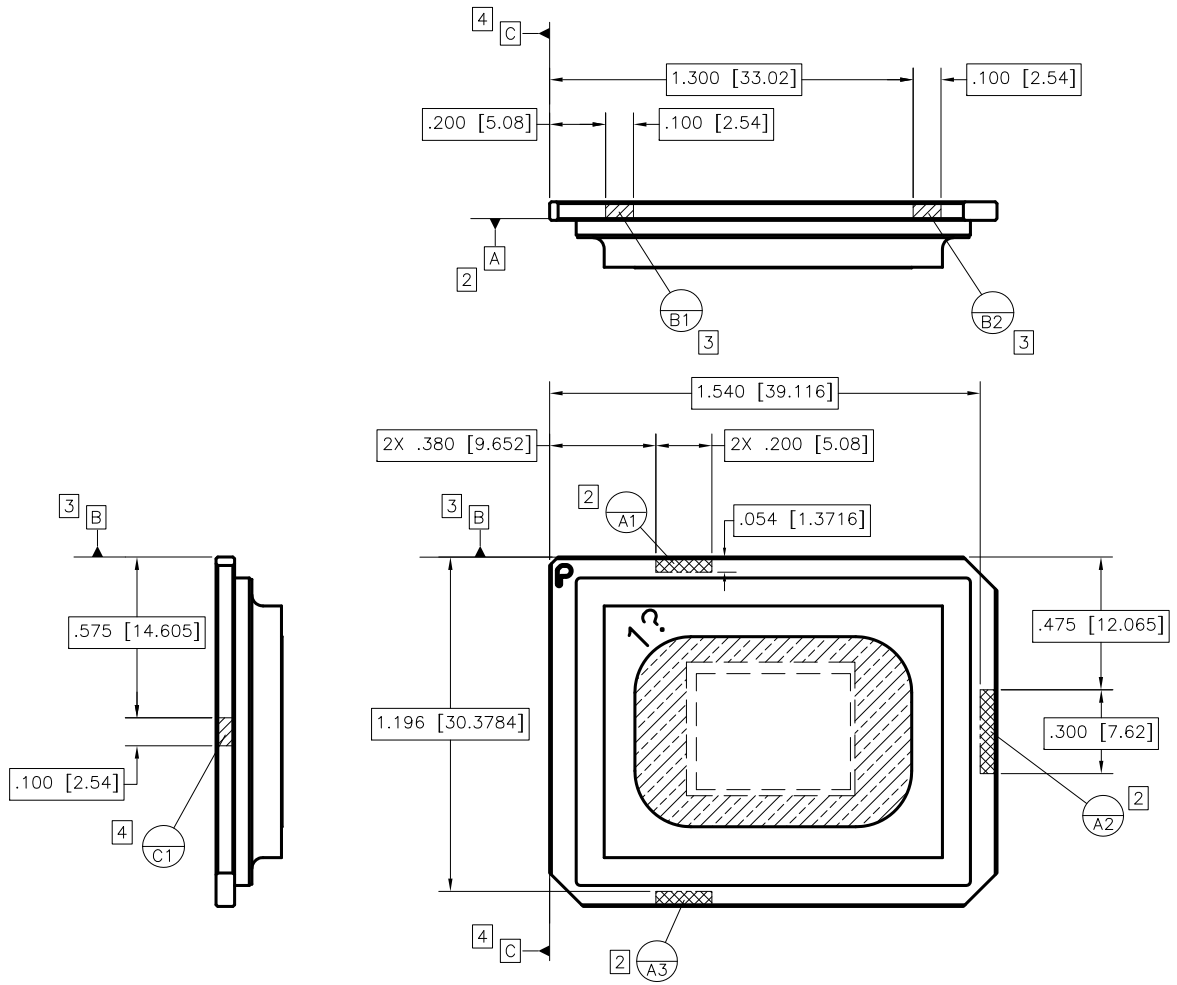
ICD, MECHANICAL, DMD
.7XGA 2X LVDS TYPE A

SIZE	DRAWING NO	REV
C	2507867	B

SCALE 3/1 SHEET 1 OF 4

DWG NO 2507867 SH 1

ACEC1g

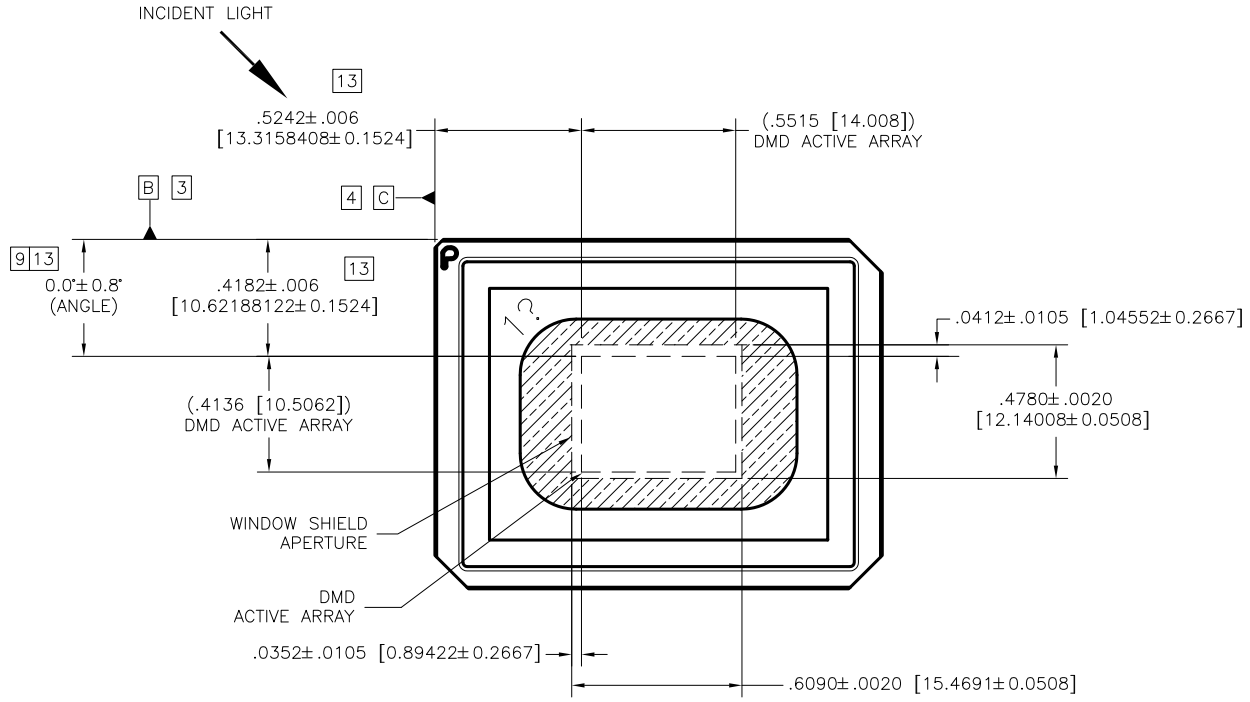


VIEW B (SHEET 1 NOTES)
DATUMS A, B, AND C

Texas Instruments, Dallas, Texas	DWN DATE	SIZE C		DRAWING NO 2507867	REV B
	ISSUE DATE	SCALE 3/1		SHEET 2	

DWG NO 2507867 SH 2

ACEC2c

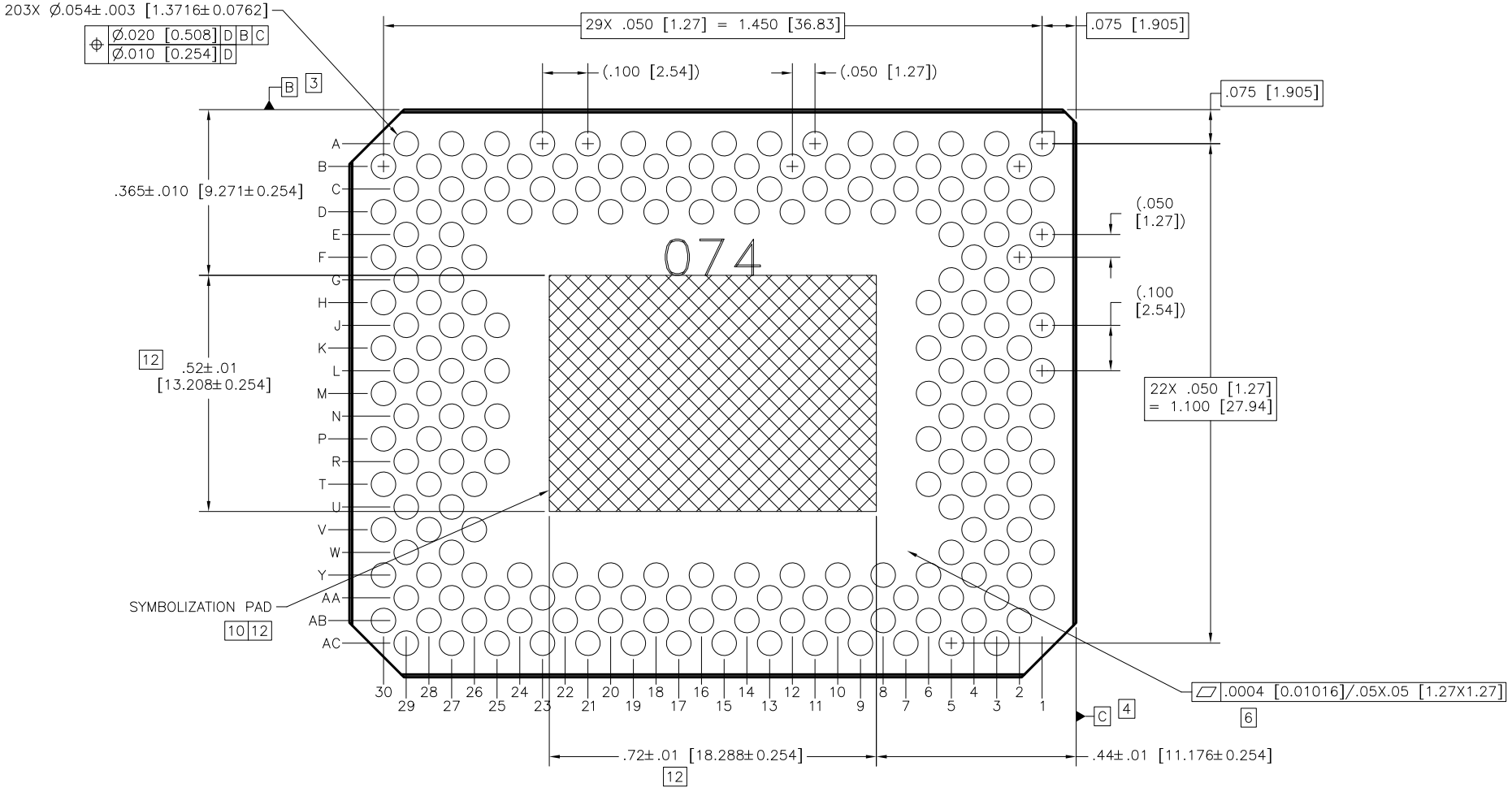


VIEW C (SHEET 1)
DMD ACTIVE ARRAY AND
WINDOW SHIELD APERTURE

Texas Instruments Dallas, Texas	DWN DATE	SIZE C		DRAWING NO 2507867	REV B
	ISSUE DATE	SCALE 3/1		SHEET 3	

DWG NO 2507867 SH 3

ACEC2c



VIEW D–D (SHEET 1)
SCALE 6/1

SH 4
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