Dual 3A/Single 6A Step-Down DC/DC Power Module

ISL8203M

The ISL8203M is an integrated step-down power module rated for dual 3A output current or 6A current sharing operation. Optimized for generating low output voltages down to 0.8V, the ISL8203M is ideal for any low power low-voltage applications. The supply voltage range is from 2.85V to 6V. The two channels are 180° out-of-phase for input RMS current and EMI reduction. Each channel is capable of 3A output current. They can be combined to form a single 6A output in current sharing mode. While in current sharing mode, the interleaving of the two channels reduces input and output voltage ripple.

The ISL8203M offers an independent power-good (PG) signal for each channel. When shut down, the ISL8203M discharges the output capacitor. Other features include internal digital soft-start, enable for power sequence, overcurrent protection and over-temperature protection.

The ISL8203M integrates a PWM controller, synchronous switching MOSFETs, inductors and passive components to maximize efficiency and minimize external component count. The ISL8203M is available in a thermally-enhanced, compact QFN package.

Features

- Dual 3A and single 6A switching power supply
- High efficiency, up to 95%
- Input voltage range: 2.85V to 6V
- Output voltage range: 0.8V to 5V
- Internal digital soft-start: 1.5ms
- External synchronization up to 4MHz
- Compact size: 9.0mmx6.5mmx1.83mm
- Peak current limiting and hiccup mode short-circuit protection
- Overcurrent protection

Applications

- µC/µP, FPGA and DSP power
- Plug-in DC/DC modules for routers and switchers
- Test and measurement systems
- Barcode reader

Related Literature

- AN1941, “ISL8203MEVAL2Z Dual 3A/single 6A Evaluation Board Set-Up Procedure”

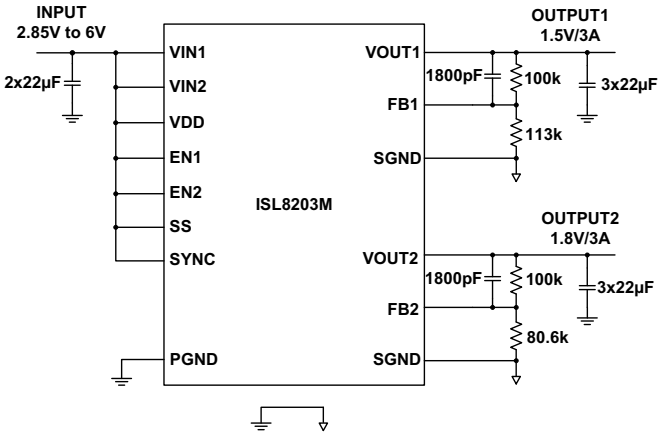


FIGURE 1. TYPICAL APPLICATION CIRCUIT - DUAL 3A

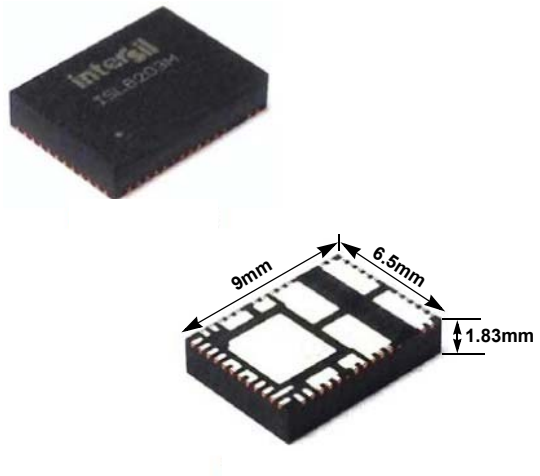


FIGURE 2. SMALL FOOTPRINT PACKAGE WITH LOW PROFILE

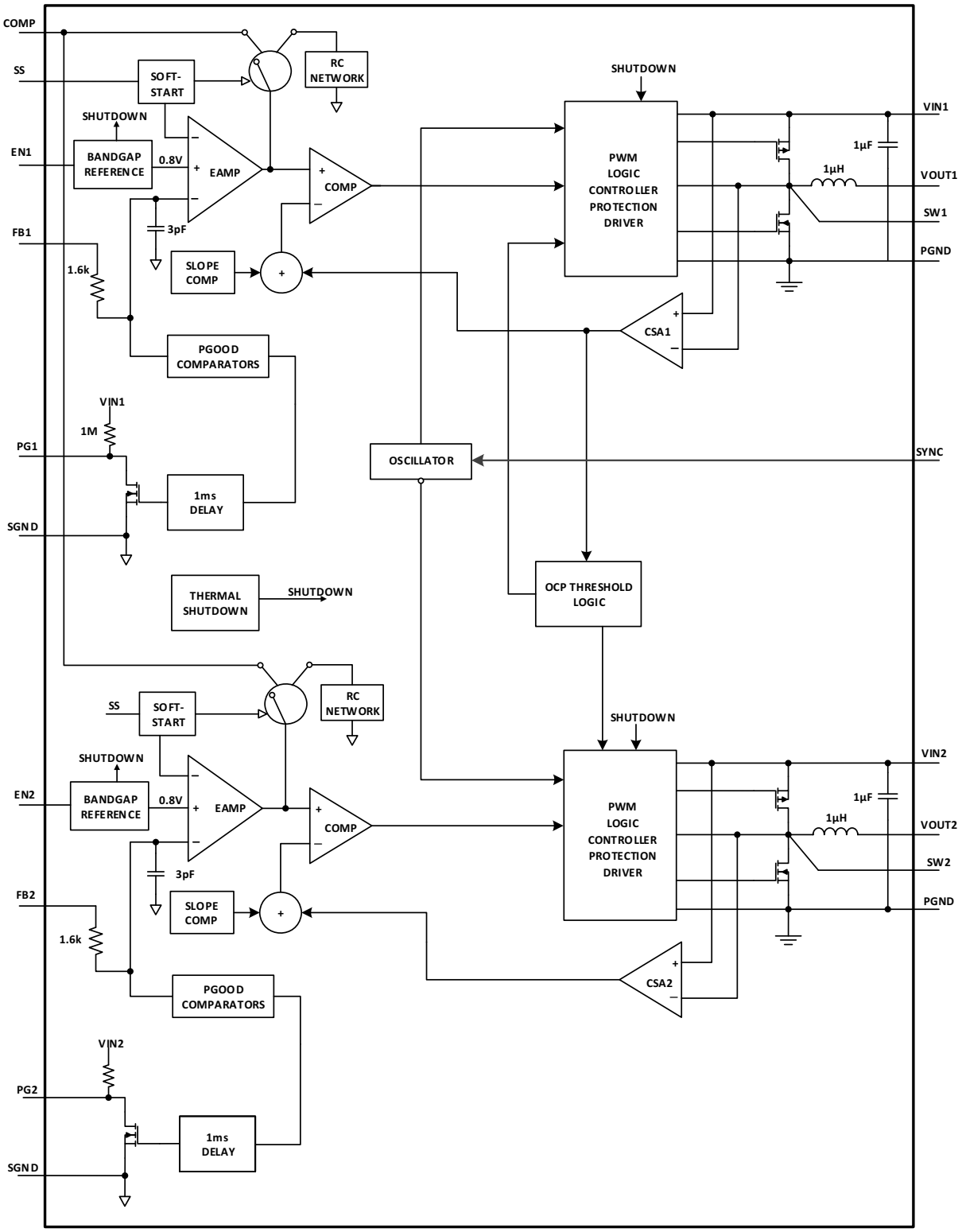
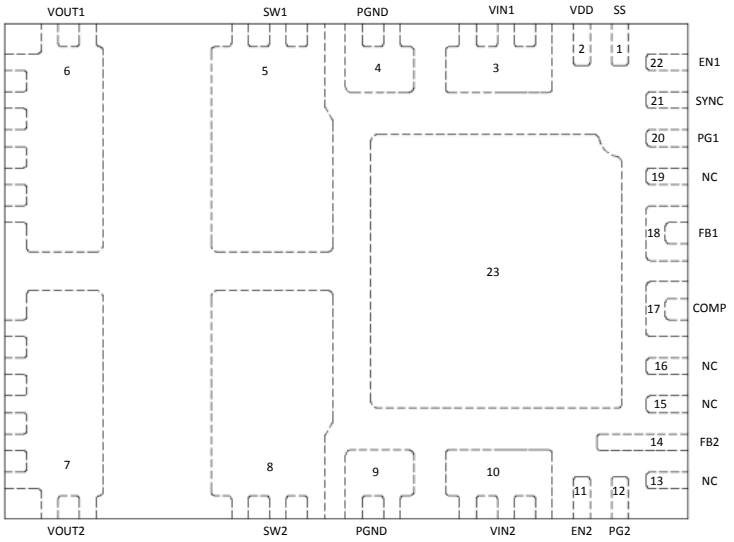


FIGURE 3. INTERNAL BLOCK DIAGRAM

Pin Configuration

ISL8203M
(23 LD QFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	SS	**Soft-start pin.** SS is used to adjust the soft-start time. For dual-output mode, tie SS pin to VIN directly and the soft-start time is fixed at 1.5ms. SS pin is tied to CSS only in parallel mode operation, with external compensation. In parallel mode, connect a capacitor C_{SS} from SS to SGND to adjust the soft-start time. C_{SS} should not be larger than 33nF. This capacitor, along with an internal 5µA current source sets the soft-start time, (refer to Equation 2).
2	VDD	**Input voltage for internal control circuit.** Tie VDD directly to VIN1. VDD should be at the same potential as the input voltage.
3, 10	VIN1, VIN2	**Power Inputs.** Input voltage range: 2.85V to 6V. Tie directly to the input rail. Input ceramic capacitors are needed between these two pins and PGND.
4, 9	PGND	**Power ground.** Power ground pins for both input and output returns.
5, 8	SW1, SW2	**Switching node.** Use for monitoring switching frequency. Switching nodes should be floating or used for snubber connections.
6, 7	VOUT1, VOUT2	**Power Output.** Apply output load between these pins and PGND pins. Output voltage range: 0.8V to 5V.
22, 11	EN1, EN2	**Power enable pins.** The output is enabled when the respective ENABLE pin is driven to high. The output is shut down and output capacitors discharged when the respective ENABLE pin is driven to low. Typically, tie to VIN pin directly. Do not leave this pin floating.
20, 12	PG1, PG2	**Power-good pins.** At power-up or EN HI, this output is a 1ms delayed Power-Good signal for the output voltage.
13, 15, 16, 19	NC	**No Connection pins.** These pins have no connections inside. Leave these pins floating.
14	FB2	**Voltage setting pin.** The output voltage V_{OUT2} is set by an external resistor divider connected to FB2. Refer to "Programming the Output Voltage" on page 12.
17	COMP	**Compensation pin.** Typically floating for dual output mode. For dual output operation, internal compensation networks are implemented for stable operation in the full range of I/O conditions. For parallel mode operation, external compensation is required. Refer to "Output Current Sharing" on page 11.
18	FB1	**Voltage setting pin.** The output voltage VOUT1 is set by an external resistor divider connected to FB1. Refer to "Programming the Output Voltage" on page 12.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
21	SYNC	**Synchronization pin.** Connect to logic high or input voltage VIN for non-use. Connect to an external function generator for external Synchronization. Negative edge trigger. Do not leave this pin floating. **Do not tie this pin low (or to PGND).**
23	SGND	**Control signal ground.** Connect to PGND under the module on the top layer. Make sure to have only two connect locations between SGND and PGND to avoid noise coupling. See "PCB Layout Recommendation" on page 14.

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL8203MIRZ (Note 1)	ISL8203M	-40 to +85	23 Ld QFN	L23.6.5x9
ISL8203MEVAL2Z	Evaluation Board			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL8203M. For more information on MSL, please see Technical Brief TB363.

Absolute Maximum Ratings (Reference to SGND)

VIN1, VIN2, VDD . . . . . -0.3V to 6.5V (DC) or 7V (20ms)
SW1, SW2 . . . . . -3V/(10ns)/-1.5V (100ns)/-0.3V (DC) to 6.5V (DC) or
. . . . . 7V (20ms)/8.5V(10ns)
EN1, EN2, PG1, PG2, SYNC, SS. . . . . -0.3V to +6.5V
FB1, FB2, COMP . . . . . -0.3V to 2.7V
ESD Ratings
Human Body Model (Tested per JESD22-A114) 1.5kV
Charged Device Model (Tested per JESD22-C101E). 1kV
Latch-up (Tested per JESD-78A; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
23 Ld QFN (Notes 4, 5)	15	2

Junction Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range. . . . . -55°C to +150°C
Ambient Temperature Range . . . . . -40°C to +85°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

V_{IN} Supply Voltage Range . . . . . 2.85V to 6V
Output Voltage Range . . . . . 0.8V to 5V
Load Current Range per Channel . . . . . 0A to 3A
Ambient Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on the ISL8203MEVAL2Z evaluation board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, the typical specifications are measured at the following conditions: T_A = +25°C, V_{OUT} = 1.2V. **Boldface limits apply across internal junction temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
INPUT SUPPLY						
VIN Undervoltage Lock-out Threshold (Note 7)	V_{UVLO}	Rising		2.5	**2.85**	V
		Hysteresis	**35**	130		mV
Input Supply Current (Note 7)	I_{VIN}	V_{IN} = 6V, EN1 = EN2 = 0, no load			**42**	µA
OUTPUT REGULATION						
Output Continuous Current Range	$I_{OUT(DC)}$	V_{IN} = 5V, V_{OUT1} = 1.2V	**0**		**3**	A
		V_{IN} = 5V, V_{OUT2} = 1.2V	**0**		**3**	A
		V_{IN} = 5V, V_{OUT1} = 1.2V, in parallel mode	**0**		**6**	A
Line Regulation	$\Delta V_{OUT1}/V_{OUT1}$ $\Delta V_{OUT2}/V_{OUT2}$	V_{IN} = 2.85V to 6V, V_{OUT1} = 1.2V, no load		0.25		%
		V_{IN} = 2.85V to 6V, V_{OUT2} = 1.2V, no load		0.25		%
		V_{IN} = 2.85V to 6V, V_{OUT1} = 1.2V, I_{OUT1} = 3A		0.25		%
		V_{IN} = 2.85V to 6V, V_{OUT2} = 1.2V, I_{OUT2} = 3A		0.25		%
Load Regulation	$\Delta V_{OUT1}/V_{OUT1}$ $\Delta V_{OUT2}/V_{OUT2}$	V_{IN} = 5V, 2x22µF ceramic output capacitor				
		I_{OUT1} = 0A to 3A, V_{OUT1} = 1.2V			**1**	%
		I_{OUT2} = 0A to 3A, V_{OUT2} = 1.2V			**1**	%
Output Voltage Accuracy		Over line/load/temperature range	**-1.5**		**1.5**	%
		Over line/load/temperature/life range	**-2.0**		**2.0**	%
Output Ripple Voltage	ΔV_{OUT}	V_{IN} = 5V, 3x22µF ceramic output capacitor				
		I_{OUT1} = 0A, V_{OUT1} = 1.2V		10		mV_{P-P}
		I_{OUT2} = 0A, V_{OUT2} = 1.2V		10		mV_{P-P}
		I_{OUT1} = 3A, V_{OUT1} = 1.2V		12		mV_{P-P}
		I_{OUT2} = 3A, V_{OUT2} = 1.2V		12		mV_{P-P}
FB1, FB2 Regulation Voltage (Note 7)	V_{FB}			0.8		V
FB1, FB2 Bias Current (Note 7)	I_{FB}	VFB = 0.75V		0.1		µA
Soft-start Ramp Time Cycle (Note 7)		SS = VDD		1.5		ms
Soft-start Charging Current (Note 7)	I_{SS}		**4**	5	**6**	µA

Electrical Specifications Unless otherwise noted, the typical specifications are measured at the following conditions: T_A = +25°C, V_{OUT} = 1.2V. **Boldface limits apply across internal junction temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
DYNAMIC CHARACTERISTICS						
Voltage Change for Positive Load Step	ΔV_{OUT-DP}	Current slew rate = 1A/µs, V_{IN} = 5V, V_{OUT} = 1.2V, 3x22µF ceramic output capacitor				
		I_{OUT1} = 0A to 1.5A		35		mV_{P-P}
		I_{OUT2} = 0A to 1.5A		35		mV_{P-P}
Voltage Change for Negative Load Step	ΔV_{OUT-DP}	Current slew rate = 1A/µs, V_{IN} = 5V, V_{OUT} = 1.2V, 3x22µF ceramic output capacitor				
		I_{OUT1} = 1.5A to 0A		45		mV_{P-P}
		I_{OUT2} = 1.5A to 0A		45		mV_{P-P}
OVERCURRENT PROTECTION						
Dynamic Current Limit ON-time	t_{OCON}			17		Clock pulses
Dynamic Current Limit OFF-time	t_{OCOFF}			8		SS cycle
Output Overcurrent Limit	I_{OUT1}	V_{IN} = 5V, V_{OUT1} = 1.2V		4.8		A
	I_{OUT2}	V_{IN} = 5V, V_{OUT2} = 1.2V		4.8		A
SW1, SW2 (Note 7)						
SW_ Maximum Duty Cycle				100		%
PWM Switching Frequency	f_{SW}		**0.85**	1.1	**1.32**	MHz
Synchronization Frequency Range (Note 8)	f_{SYNC}		**2.64**		**4**	MHz
Channel 1 to Channel 2 Phase Shift		Rising edge to rising edge timing		180		°
SW Minimum On Time		SYNC = High (PWM mode)			**140**	ns
Soft Discharge Resistance	R_{DIS}	EN = LOW	**80**	100	**124**	Ω
PG1, PG2 (Note 7)						
Output Low Voltage		Sinking 1mA, VFB = 0.7V			**0.32**	V
PG Pin Leakage Current		PG = V_{IN} = 6V		0.01	**0.1**	µA
Internal PGOOD Threshold		Percentage of nominal regulation voltage		90		%
Delay Time (Rising Edge)		Time from V_{OUT} reached regulation		1		ms
Internal PGOOD Delay Time (Falling Edge)				7	**15**	µs
EN1, EN2, SYNC (Note 7)						
Logic Input Low					**0.4**	V
Logic Input High			**1.5**			V
SYNC Logic Input Leakage Current	I_{SYNC}	Pulled up to 6V		0.1	**1**	µA
Enable Logic Input Leakage Current	I_{EN}	Pulled up to 6V		0.1	**1**	µA
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				25		°C

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. Parameters with MIN and/or MAX limits are 100% tested for internal IC prior to module assembly, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. The operational frequency per switching channel is half of the SYNC frequency.

Typical Performance Characteristics

Efficiency T_A = +25°C.

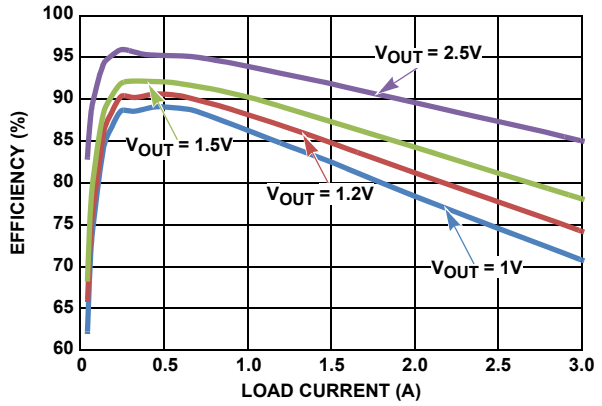


FIGURE 4. SINGLE CHANNEL, EN1 = HIGH, EN2 = LOW, V_{IN} = 3.3V

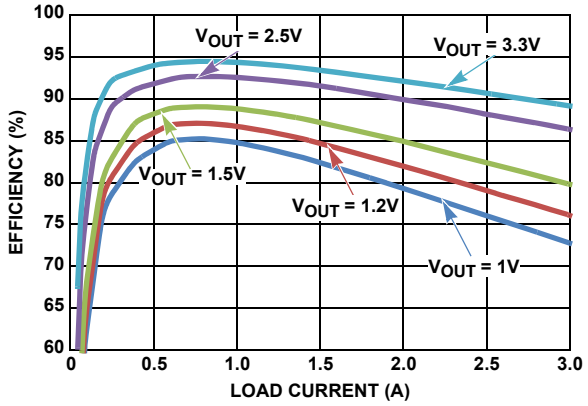


FIGURE 5. SINGLE CHANNEL, EN1 = HIGH, EN2 = LOW, V_{IN} = 5V

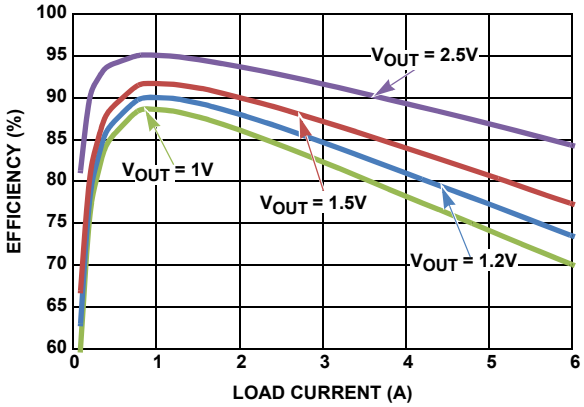


FIGURE 6. PARALLEL SINGLE OUTPUT, V_{IN} = 3.3V

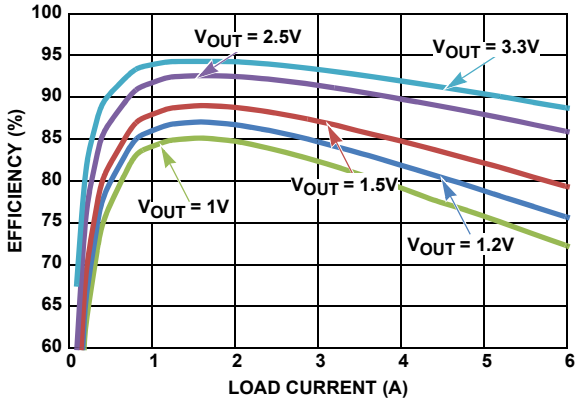


FIGURE 7. SINGLE CHANNEL, V_{IN} = 5V

Output Voltage Ripple T_A = +25°C.

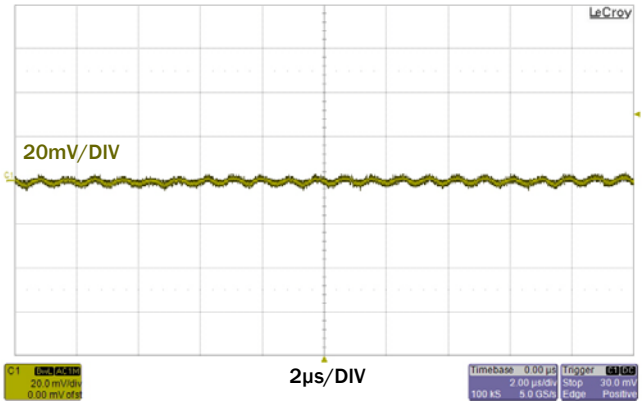


FIGURE 8. SINGLE CHANNEL, EN1 = HIGH, EN2 = LOW, V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 3A, C_{OUT} = 3x22µF CERAMIC CAPACITORS

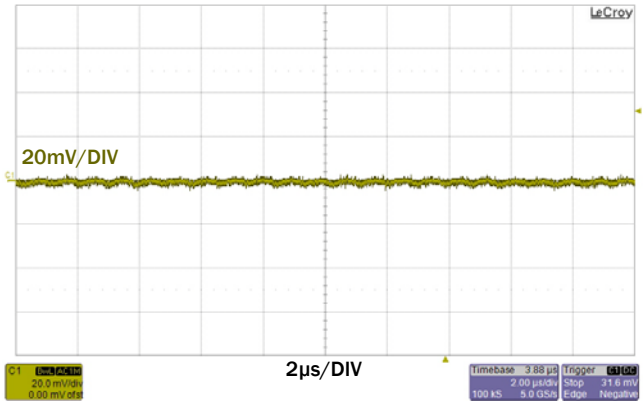


FIGURE 9. PARALLEL SINGLE OUTPUT, V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 6A, C_{OUT} = 6x22µF CERAMIC CAPACITORS

Typical Performance Characteristics (Continued)

Load Transient Response

T_A = +25°C. Load current step slew rate: 1A/µs

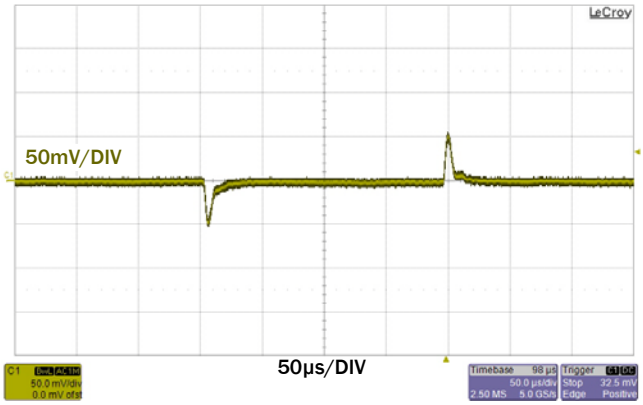


FIGURE 10. SINGLE CHANNEL, EN1 = HIGH, EN2 = LOW, V_{IN} = 3.3V, V_{OUT} = 1V, I_{OUT} = 0A to 1.5A STEP, C_{OUT} = 3x22µF CERAMIC CAPACITORS

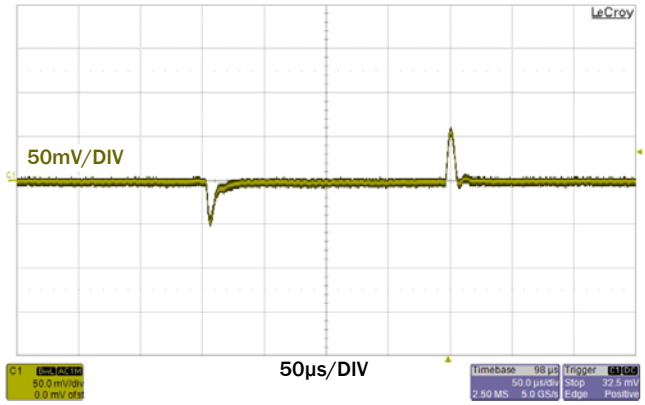


FIGURE 11. SINGLE CHANNEL, EN1 = HIGH, EN2 = LOW, V_{IN} = 5V, V_{OUT} = 1V, I_{OUT} = 0A TO 1.5A STEP, C_{OUT} = 3x22µF CERAMIC CAPACITORS

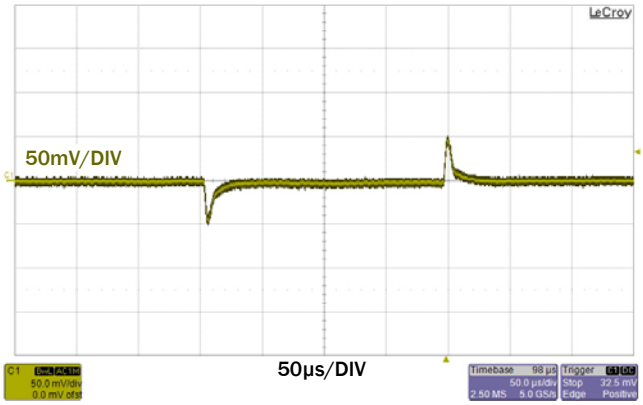


FIGURE 12. SINGLE CHANNEL, EN1 = HIGH, EN2 = LOW, V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 0A to 1.5A STEP, C_{OUT} = 3x22µF CERAMIC CAPACITORS

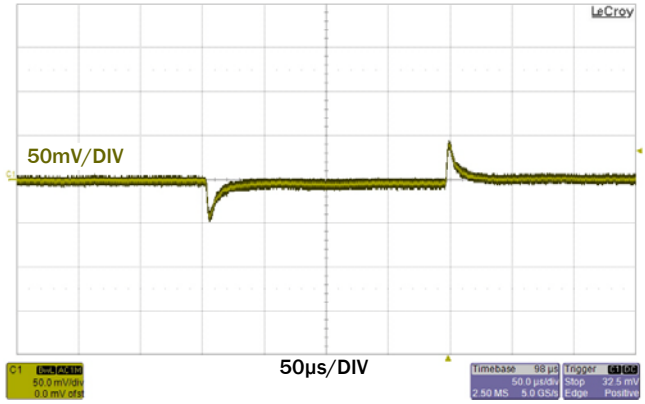


FIGURE 13. SINGLE CHANNEL, EN1 = HIGH, EN2 = LOW, V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 0A TO 1.5A STEP, C_{OUT} = 3x22µF CERAMIC CAPACITORS

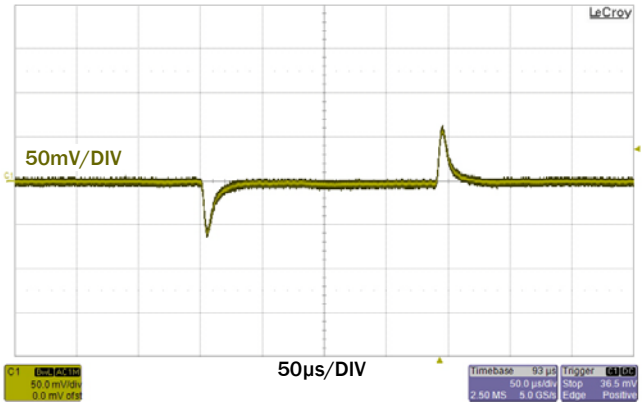


FIGURE 14. PARALLEL SINGLE OUTPUT, V_{IN} = 3.3V, V_{OUT} = 1V, I_{OUT} = 0A TO 1.5A STEP, C_{OUT} = 6x22µF CERAMIC CAPACITORS

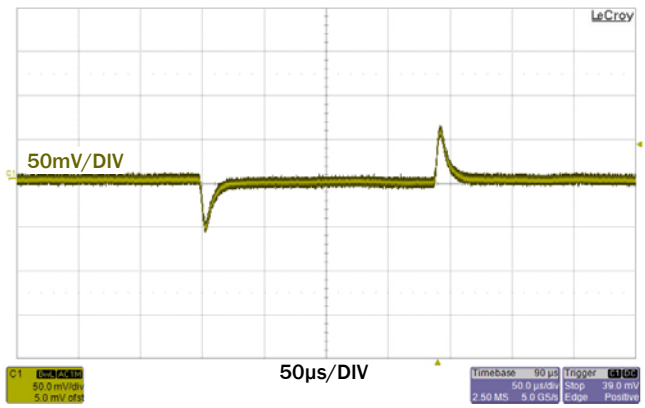


FIGURE 15. PARALLEL SINGLE OUTPUT, V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A TO 1.5A STEP, C_{OUT} = 6x22µF CERAMIC CAPACITORS

Typical Performance Characteristics (Continued)

Start-Up T_A = +25°C

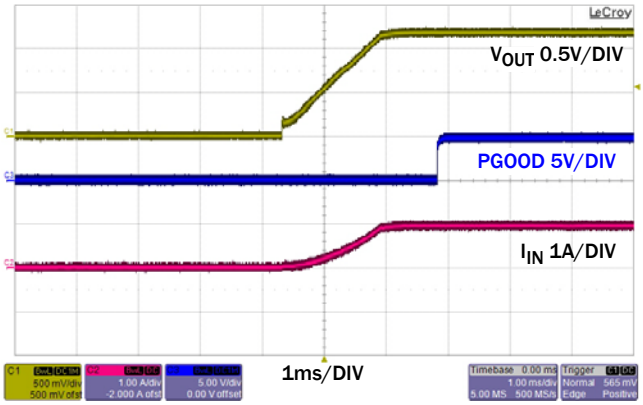


FIGURE 16. SINGLE CHANNEL, EN1 = HIGH, EN2 = LOW, SOFT-START WITH 3A LOAD, V_{IN} = 5V, V_{OUT1} = 1.2V, I_{OUT1} = 3A, C_{OUT} = 3x22µF CERAMIC CAPACITORS, C_{IN} = 100µF + 22µF CERAMIC CAPACITORS

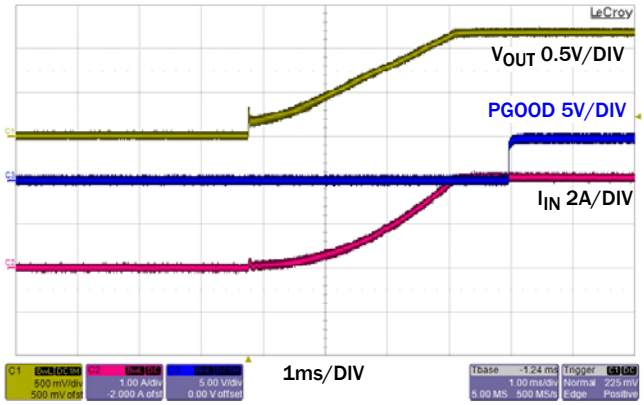


FIGURE 17. PARALLEL SINGLE OUTPUT, SOFT-START WITH 6A LOAD, V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 6A, CSS = 0.022µF, C_{OUT} = 6x22µF CERAMIC CAPACITORS, C_{IN} = 100µF + 22µF CERAMIC CAPACITORS

Short-Circuit Protection

T_A = +25°C, parallel single output mode, V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 6A, C_{IN} = 100µF+22µF ceramic capacitors, C_{OUT} = 6x22µF ceramic capacitors.

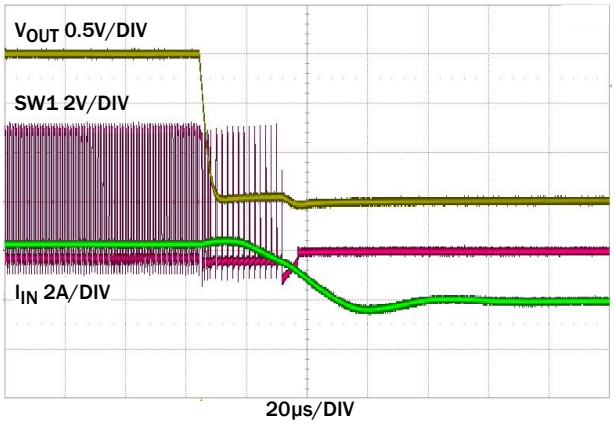


FIGURE 18. OUTPUT SHORT-CIRCUIT PROTECTION

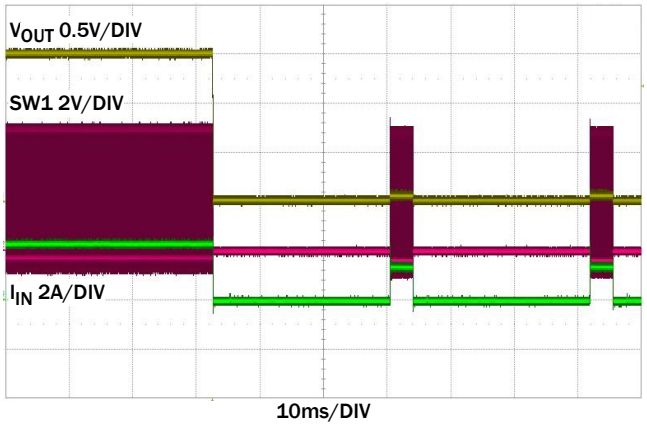


FIGURE 19. OUTPUT SHORT-CIRCUIT PROTECTION, HICCUP MODE

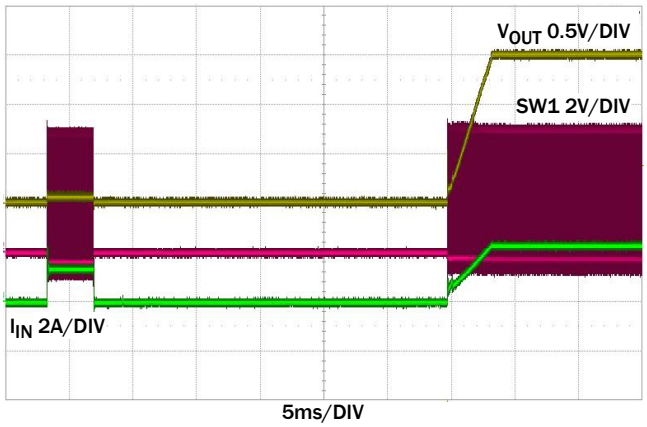


FIGURE 20. OUTPUT SHORT-CIRCUIT RECOVERY FROM HICCUP

Typical Application Circuits

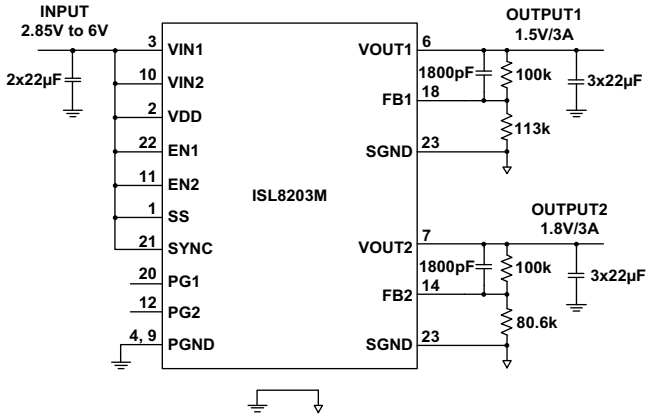


FIGURE 21. DUAL OUTPUT FOR 1.5V/3A AND 1.8V/3A

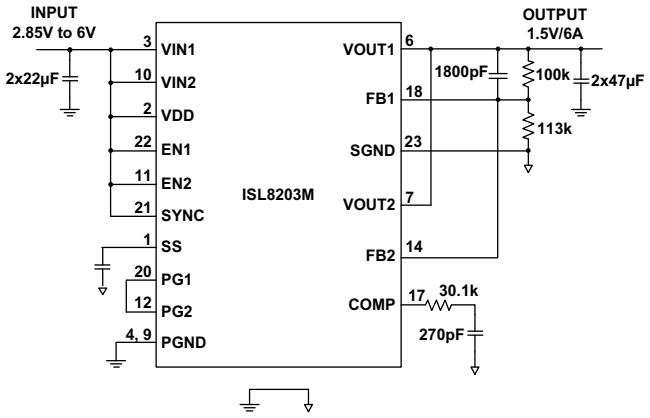


FIGURE 22. PARALLEL SINGLE OUTPUT FOR 1.5V/6A

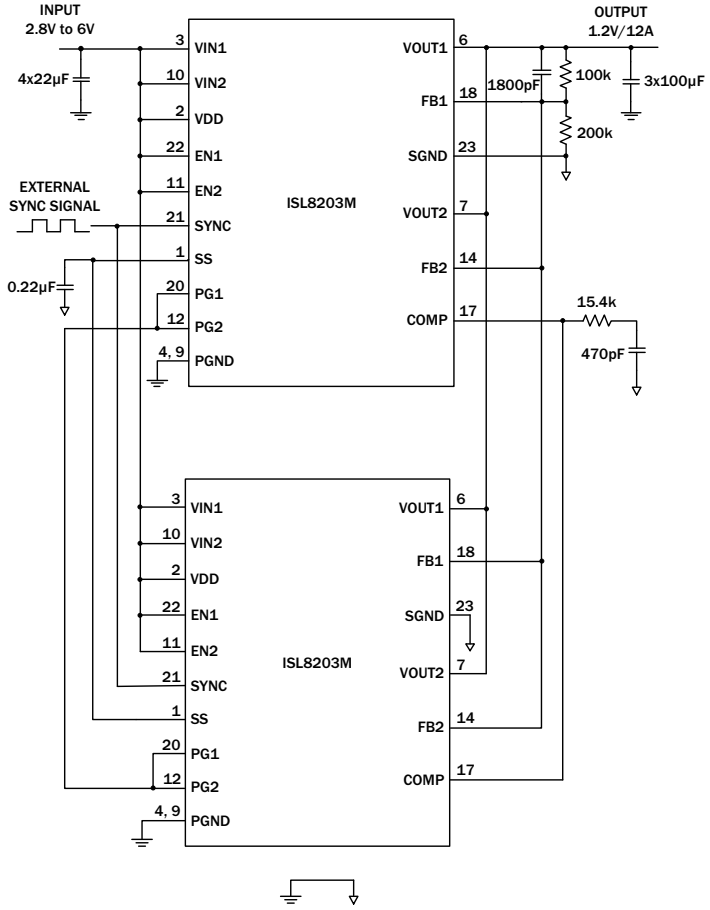


FIGURE 23. 4-PHASE PARALLEL SINGLE OUTPUT FOR 1.2V/12A

NOTES:

9. Refer to "PCB Layout Recommendation" on page 14 for shorting SGND to PGND.
10. Refer to "Output Current Sharing" on page 11 for external compensation components.

Functional Description

PWM Control Scheme

Each channel of the ISL8203M employs the current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting, as shown in the "INTERNAL BLOCK DIAGRAM" on page 2 and with waveforms in Figure 24. The current loop consists of the oscillator, the PWM comparator COMP, current sensing circuit, and the slope compensation for the current loop stability. The current sensing circuit consists of the resistance of the P-MOSFET when it is turned on and the current sense amplifier CSA1 (or CSA2 of Channel 2). The gain for the current sensing circuit is typically 0.2V/A. The control reference for the current loops comes from the error amplifier EAMP of the voltage loop.

The PWM operation is initialized by the clock from the oscillator. The P-channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA1 (or CSA2 of channel 2) and the compensation slope (0.46V/µs) reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-MOSFET and to turn on the N-channel MOSFET. The N-MOSFET stays on until the end of the PWM cycle. Figure 24 shows the typical operating waveforms during the PWM operation, where the dotted lines illustrate the sum of the compensation ramp and the current-sense amplifier output V_{CSA1}, V_{EAMP} represents the output of the error amplifier, and I_L represents the inductor current.

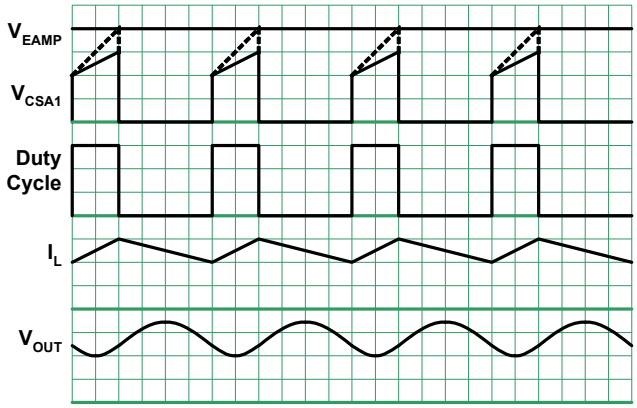


FIGURE 24. PWM OPERATION WAVEFORMS

The output voltage is regulated by controlling the reference voltage to the current loop. The bandgap circuit outputs a 0.8V reference voltage to the voltage control loop. The feedback signal comes from the FB pin. The soft-start circuitry only affects the operation during start-up and will be discussed separately; please refer to "Soft-Start" on page 12. The voltage loop is internally compensated for the dual output mode. For parallel current sharing mode, external compensation is required.

Synchronization Control

The frequency of operation can be synchronized up to 4MHz by an external signal applied to the SYNC pin. The 1st falling edge on the SYNC triggers the rising edge of the PWM ON pulse of Channel 1. The 2nd falling edge of the SYNC triggers the rising edge of the PWM ON pulse of Channel 2. This process alternates indefinitely allowing 180° out-of-phase operation between the two channels. The switching frequency per channel is half of the external signal's frequency applied to the SYNC pin. The maximum external signal frequency is limited by the SW minimum on time (140ns MAX) requirement. The maximum external signal frequency can be calculated as shown in Equation 1.

$$\frac{1}{2} \cdot f_{SYNC-MAX} = f_{SW-MAX} \leq \frac{V_{OUT}}{V_{IN}} \cdot \frac{1}{140ns} \quad \text{(EQ. 1)}$$

where:

- $f_{SYNC-MAX}$ is the maximum external signal frequency
- f_{SW-MAX} is the maximum switching frequency per channel
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Output Current Sharing

The ISL8203M's two channels can be paralleled for dual-phase operation in order to support a 6A output. In the parallel mode, the two channels are 180° out-of-phase, which reduces input and output voltage ripple and EMI. Connect V_{OUT1} to V_{OUT2}, FB1 to FB2, EN1 to EN2, PG1 to PG2 and connect a soft-start capacitor C_{SS} from SS to SGND; refer to Figure 22. In parallel mode, external compensation network of a resistor and a capacitor is required with the typical values of 30.1kΩ and 270pF; refer to Figure 22.

Similar to the dual-phase operation, multiple modules can be paralleled for higher current capability. Connect all the modules' FB pins, COMP pins, SS pins, EN pins and PG pins; refer to Figure 23.

Overcurrent Protection

Current sense amplifiers CSA1 and CSA2 are used to monitor the two channels' internal inductor current respectively. The overcurrent protection is realized by monitoring the CSA output with the OCP threshold logic, as shown in Figure 2 on page 1. The current sensing circuit has a gain of 0.2V/A, from the P-MOSFET current to the CSA_ output. When the CSA1 output reaches the threshold, the OCP comparator is tripped to turn off the P-MOSFET immediately. The overcurrent function protects the module from a shorted output by monitoring the current flowing through the upper MOSFETs.

Upon detection of an overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the overcurrent fault counter is set to 1 and the overcurrent condition flag is set from LOW to HIGH. If, on the subsequent cycle, another overcurrent condition is detected, the OC fault counter will be incremented. If there are 17 sequential OC fault detections, the module will shut down under an overcurrent fault condition. An overcurrent fault condition will result in the module attempting to restart in a hiccup mode with the delay between restarts being 8 soft-start periods. At the end of the eighth soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away prior to the OC fault counter reaching a count of four, the overcurrent condition flag will set back to LOW.

If the negative current of the internal inductor reaches -2.5A, the module enters negative overcurrent protection. At this point, all switching stops and the module enters tri-state mode while the pull-down MOSFET discharges the output until it reaches normal regulation voltage, then the module restarts.

Power-Good

There are two independent power-good signals for each of the two outputs via the FB pins. PG1 monitors the output Channel 1 and PG2 monitors the output Channel 2. When powering up, the open-collector power-on reset output holds low for about 1ms after V_{OUT} reaches within ±8% of the preset voltage. The PG pins do not require a pull-up resistor.

UVLO (Undervoltage Lock-Out)

When the input voltage is below the undervoltage lockout (UVLO) threshold, the module is disabled. The maximum UVLO threshold is 2.85V.

Enable

The enable (EN) input allows the user to control the turning on or off of the module for purposes such as power-up sequencing. Each channel of the ISL8203M can be turned on or off independently through the EN pins. Once the module is enabled, there is typically a 600µs delay for waking up the bandgap reference, then the soft start-up begins.

Soft-Start

The ISL8203M employs an internal digital soft-start circuitry which minimizes input inrush current during the start-up. The soft-start circuitry outputs a ramp reference to both the voltage loop and the current loop. The two ramps limit the inductor current rising speed as well as the output voltage rising speed so that the output voltage rises in a controlled fashion. At the beginning of the soft-start internal, when the voltage on the FB pin is less than 0.5V, the PWM oscillator frequency is forced to half of the normal frequency. During the soft-start, the module cannot sink current, behaving as in diode emulated mode for the soft-start time.

If SS pin is tied to VIN, the soft-start time is an internally fixed 1.5ms. For parallel current sharing mode operation, connect a capacitor C_{SS} from SS to SGND. C_{SS} should not be larger than 33nF. This capacitor along with the internal current source of 5µA sets the soft-start time t_{SS}, which can be calculated as shown in Equation 2.

$$t_{SS}[ms] = 0.16 \cdot C_{SS}[nF] \quad \text{(EQ. 2)}$$

Discharge Mode

When a transition to shutdown mode occurs, or the output undervoltage fault latch is set, the module's output discharges to PGND through an internal 100Ω switch.

Power MOSFETs

The internal power MOSFETs are optimize for best efficiency. The ON-resistance for the P-MOSFET is typically 50mΩ and the ON-resistance for the N-MOSFET is typically 50mΩ.

100% Duty Cycle Operation

The ISL8203M offers 100% duty cycle operation. When the input voltage drops to a level that the ISL8203M can no longer maintain the regulation at the output, the module completely turns on the P-MOSFET. The maximum dropout voltage under the 100% duty-cycle operation is the product of the load current and the ON-resistance of the P-MOSFET.

Thermal Shutdown

The ISL8203M offers built-in over-temperature protection. When the junction temperature reaches +150°C, the module is completely shut down. As the temperature drops to +125°C, the ISL8203M resumes operation by stepping through a soft-start.

Applications Information

Programming the Output Voltage

The output voltage of the module is programmed by an external resistor divider between VOUT, FB, and SGND pins, as shown in Figure 21. The output voltage can be calculated as shown in Equation 3.

$$VOUT = 0.8V \cdot \left(1 + \frac{R_{FBTOP}}{R_{FBBOT}}\right) \quad \text{(EQ. 3)}$$

Where:

- R_{FBTOP} is the top feedback resistor
- R_{FBBOT} is the bottom feedback resistor

The top resistor is typically a 100kΩ value, and a 1800pF capacitor is recommended to be connected in parallel if the output capacitors are all ceramic capacitors or bulk capacitors with low ESR (equivalent series resistance). The value of the bottom resistor for different output voltages is shown in Table 1.

TABLE 1. VALUE OF BOTTOM RESISTOR FOR DIFFERENT OUTPUT VOLTAGES (V_{OUT} vs R_{FBBOT})

R_{FBTOP} (kΩ)	VOUT (V)	R_{FBBOT} (kΩ)
100	0.8	open
100	1.0	402
100	1.2	200
100	1.5	113
100	1.8	80.6
100	2.5	47.5
100	3.3	32.4

Please note that the output voltage accuracy is also dependent on the resistor accuracy of R_{FBTOP} and R_{FBBOT}. The user needs to select high accuracy resistors (i.e., 0.5%) in order to achieve the overall output accuracy.

Input Capacitor Selection

Low Equivalent Series Resistance (ESR) ceramic capacitance is recommended to reduce input voltage ripple and decouple between the VIN and PGND of each channel. This capacitance

reduces voltage ringing created by the switching current across parasitic circuit elements. The ceramic capacitors should be placed as closely as possible to the module pins. A minimum of 22µF ceramic capacitance for each channel is recommended.

A bulk input capacitance may also be needed if the input source does not have enough output capacitance. A typical value of bulk input capacitor is 100µF. In such conditions, this bulk input capacitance can supply the current during output load transient conditions.

Output Capacitor Selection

Ceramic capacitors are typically used as the output capacitors for the ISL8203M. A minimum output capacitance of 2x22µF per phase is recommended. Bulk output capacitors that have adequately low Equivalent Series Resistance (ESR), such as low ESR polymer capacitors or a low ESR tantalum capacitor, may also be used in combination with the ceramic capacitors, depending on the output voltage ripple and transient requirements.

Thermal Consideration and Current Derating

Experimental power loss data (Figures 25 and 26), along with θ_{JA} from thermal modeling analysis, can be used as a guide for thermal consideration for the module. The ISL8203M's thermally enhanced package offers typical junction to ambient thermal resistance θ_{JA} of approximately 15°C/W at natural convection (13°C/W with 200LFM airflow) with a typical 4-layer PCB board. The derating curves (Figures 27 through 31) are derived from the maximum power dissipation allowed, while maintaining the junction temperature below a maximum junction temperature of +120°C; the derating curves take into consideration the increased power dissipation at elevated ambient temperatures. The maximum +120°C junction temperature is recommended for the module to load the current consistently and it provides the 5°C margin of safety from the rated junction temperature of +125°C.

All the derating curves are obtained based on tests on the ISL8203MEVAL2Z evaluation board (Refer to AN1941, "ISL8203MEVAL2Z Dual 3A/Single 6A Evaluation Board Set-Up Procedure"). If necessary, the customer can adjust the margin of safety according to the real application. In the actual application, other heat sources and design margins should be considered.

Power Loss Curves

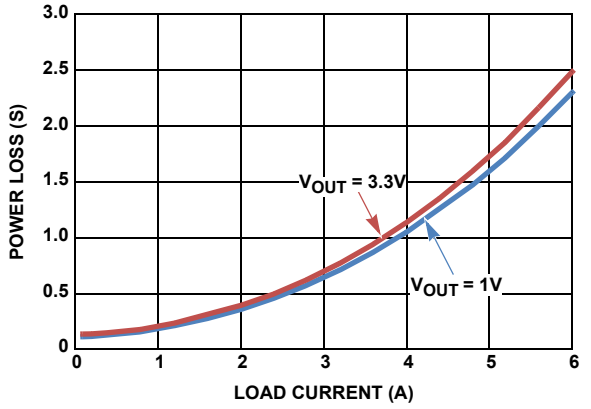


FIGURE 25. POWER LOSS AT V_{IN} = 5V, PARALLEL SINGLE OUTPUT, T_A = +25°C

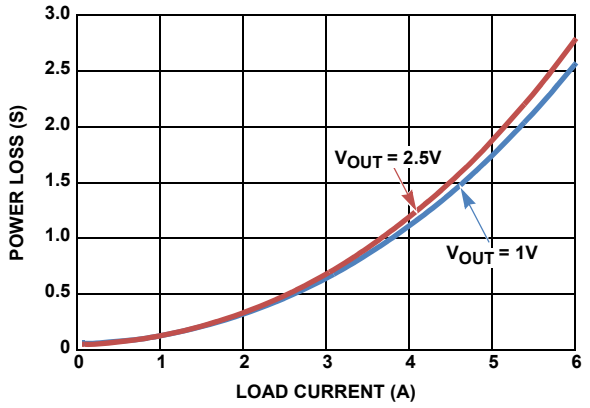


FIGURE 26. POWER LOSS AT V_{IN} = 3.3V, PARALLEL SINGLE OUTPUT, T_A = +25°C

Derating Curves

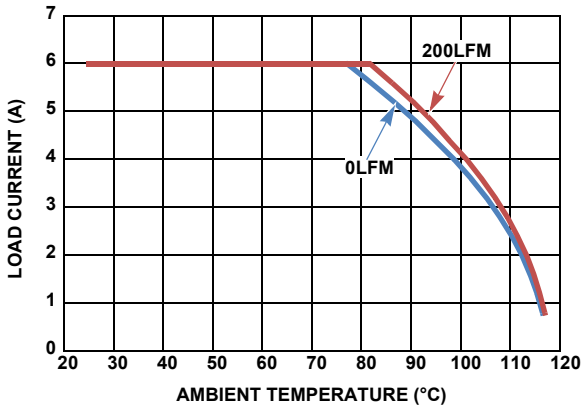


FIGURE 27. DERATING CURVES AT V_{IN} = 5V, V_{OUT} = 1V

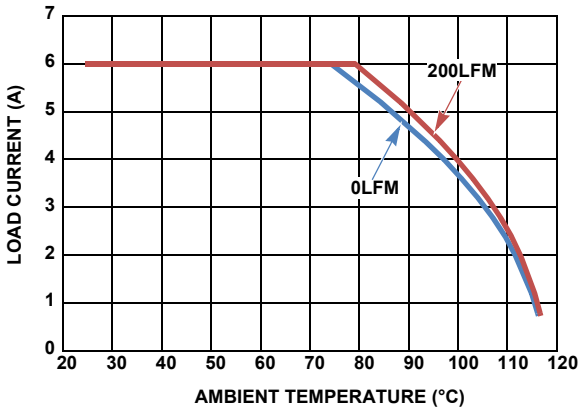


FIGURE 28. DERATING CURVES AT V_{IN} = 5V, V_{OUT} = 3.3V

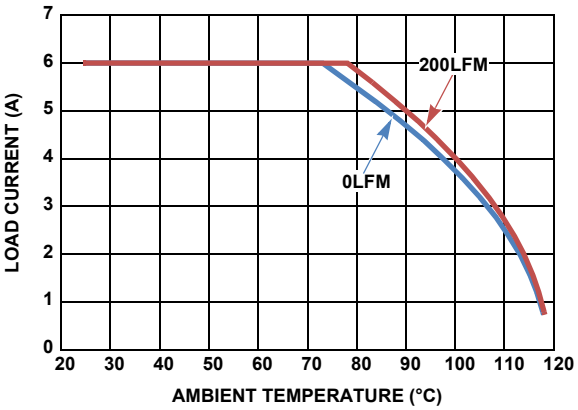


FIGURE 29. DERATING CURVES AT V_{IN} = 3.3V, V_{OUT} = 1V

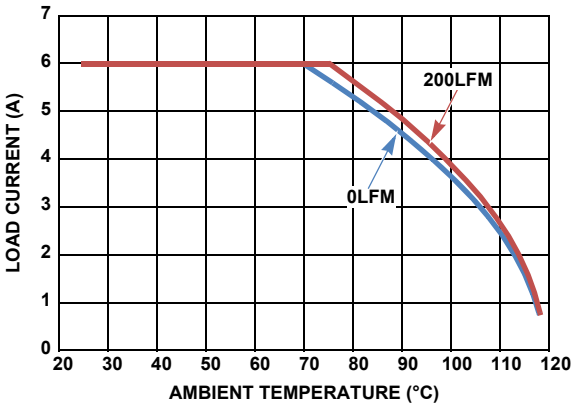


FIGURE 30. DERATING CURVES AT V_{IN} = 3.3V, V_{OUT} = 2.5V

PCB Layout Recommendation

To achieve stable operation, low losses and good thermal performance, some layout considerations are necessary (Figure 31).

- Use large copper areas for power path (VIN1, VIN2, SGND, PGND, VOUT1, VOUT2) to minimize conduction loss and thermal stress. Also, it is recommended to use multiple vias to connect the power planes in different layers. Use at least 5 vias on the SGND pad 23 connected to SGND plane(s) for the best thermal relief.
- Use a separate SGND ground copper area for components connected to signal ground pins. Connect SGND pad 23 to PGND pin 4 at a single location and SGND pad 23 to PGND pin 9 at a single location.
- The switching node of the module, the SW pins and the traces connected to the pins are very noisy. Keep these pads under the module. For noise sensitive applications, it is recommended to keep the SW pads only on the top and inner layers of the PCB. Do not expose the SW pads to the outside on the bottom layer of the PCB.
- Avoid routing noise-sensitive signal traces such as FB1, FB2, and COMP near the noisy SW pins.
- The feedback network should be placed as close as possible to the FB pins, and far away from the SW pins.
- Place high frequency ceramic capacitors between VIN, VOUT and PGND, as close to the module as possible in order to minimize high frequency noise. Place several vias close to the ceramic capacitors. The ground terminal of the input capacitors and output capacitors should be placed as close as possible.

Package Description

The ISL8203M is integrated into a quad flat-pack no-lead package (QFN). This package has such advantages as good thermal and electrical conductivity, low weight and small size. The QFN package is applicable for surface mounting technology and is becoming more common in the industry. The ISL8203M is a copper leadframe based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper leadframe and multicomponent assembly are overmolded with polymer mold compound to protect these devices.

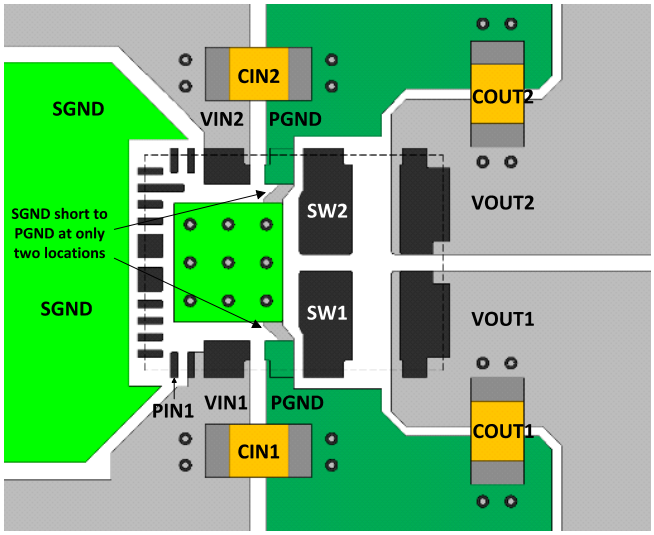


FIGURE 31. RECOMMENDED LAYOUT

The package outline, typical PCB layout pattern, and typical stencil pattern design are shown in the L23.6.5x9 "Package Outline Drawing" on page 17. TB493 shows typical reflow profile parameters. These guidelines are general design rules. Users can modify parameters according to specific applications.

PCB Layout Pattern Design

The bottom of ISL8203M is a leadframe footprint, which is attached to the PCB by surface mounting. The PCB layout pattern is shown in the L23.6.5x9 "Package Outline Drawing" on page 17. The PCB layout pattern is essentially 1:1 with the QFN exposed pad and the I/O termination dimensions, except that the PCB lands are slightly longer than the QFN terminations by about 0.2mm (0.4mm max). This extension allows for solder filleting around the package periphery and ensures a more complete and inspectable solder joint. The thermal lands on the PCB layout should match 1:1 with the package exposed die pads.

Thermal Vias

A grid of 1.0mm to 1.2mm pitched thermal vias, which drops down and connects to buried copper planes, should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter, with the barrel plated to about 2.0 ounce copper. Although adding more vias (by decreasing pitch) improves thermal performance, it also diminishes results as more vias are added. Use only as many vias as are needed for the thermal land size and as your board design rules allow.

Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joins. The stencil aperture size to land size ratio should typically be 1:1. Aperture width may be reduced slightly to help prevent solder bridging between adjacent I/O lands.

To reduce solder paste volume on the larger thermal lands, an array of smaller apertures instead of one large aperture is recommended. The stencil printing area should cover 50% to 80% of the PCB layout pattern. Consider the symmetry of the whole stencil pattern when designing the pads.

A laser-cut, stainless-steel stencil with electropolished trapezoidal walls is recommended. Electropolishing smooths the aperture walls, resulting in reduced surface friction and better paste release, which reduces voids. Using a trapezoidal section aperture (TSA) also promotes paste release and forms a brick-like paste deposit, which assists in firm component placement.

Reflow Parameters

Due to the low mount height of the QFN, "No Clean" Type 3 solder paste, per ANSI/J-STD-005, is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the QFN. The profile given in TB493 is provided as a guideline to customize for varying manufacturing practices and applications.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
January 19, 2015	FN8661.3	Updated “Package Outline Drawing” on page 17 with latest revision. Corrected/updated recommended PCB land pattern and added recommended stencil patterns.
August 28, 2014	FN8661.2	Added to sentence that is under “Programming the Output Voltage” on page 12 after “...in parallel.”, which reads “if the output capacitors are all ceramic capacitors or bulk capacitors with low ESR (equivalent series resistance)." Replaced Schematics on page 1 and page 10. Figure 2, added the XYZ dimension on the picture (9.0mmx6.5mmx1.83mm. Figure 23, changed the "113k" resistor to "200k".
July 23, 2014	FN8661.1	Added Evaluation Board to “Ordering Information” on page 4.
June 23, 2014	FN8661.0	Initial Release

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Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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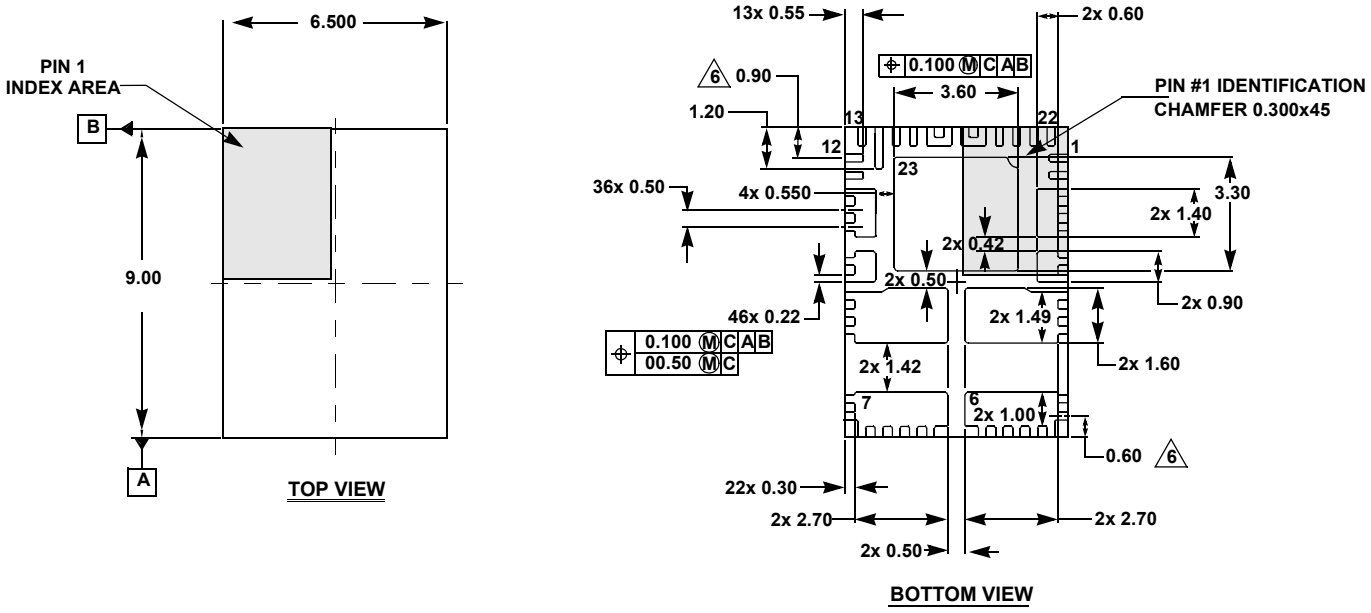
Package Outline Drawing

L23.6.5x9

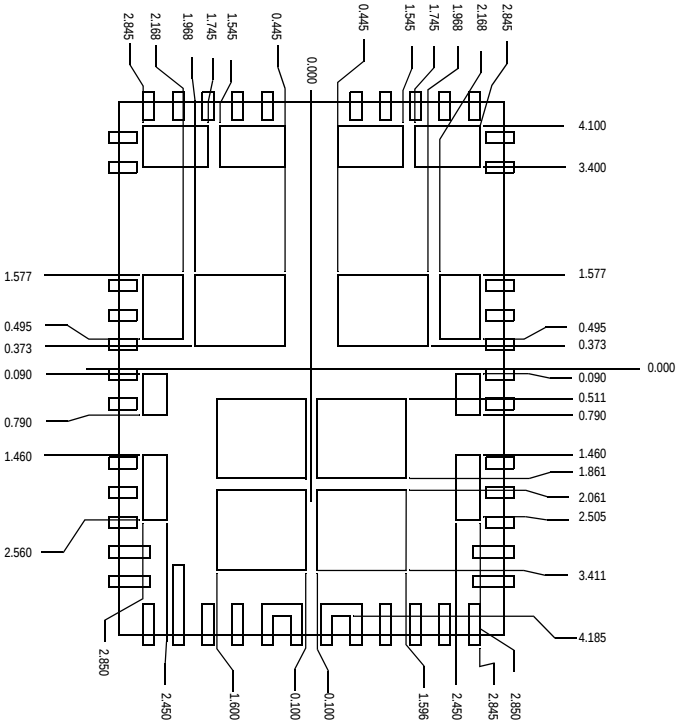
23 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 1, 10/14

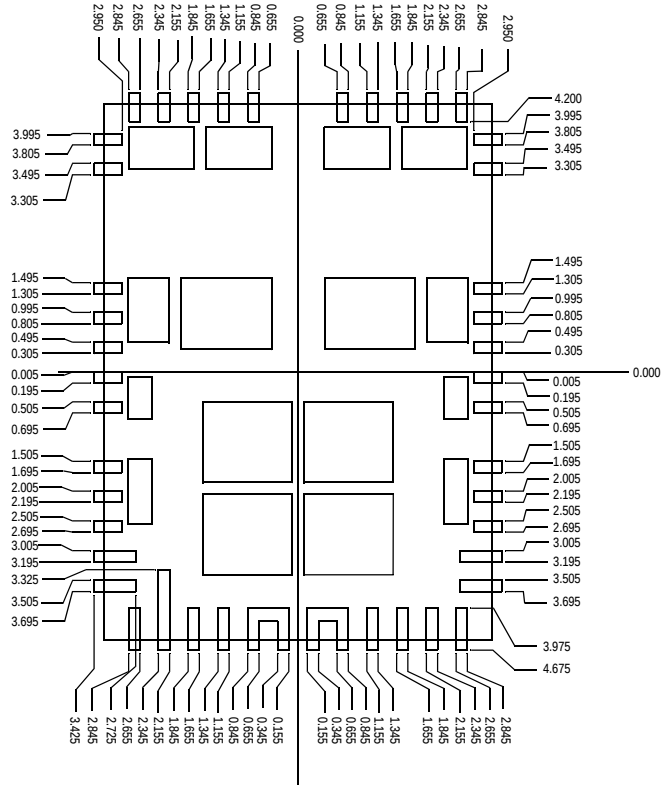


NOTES:

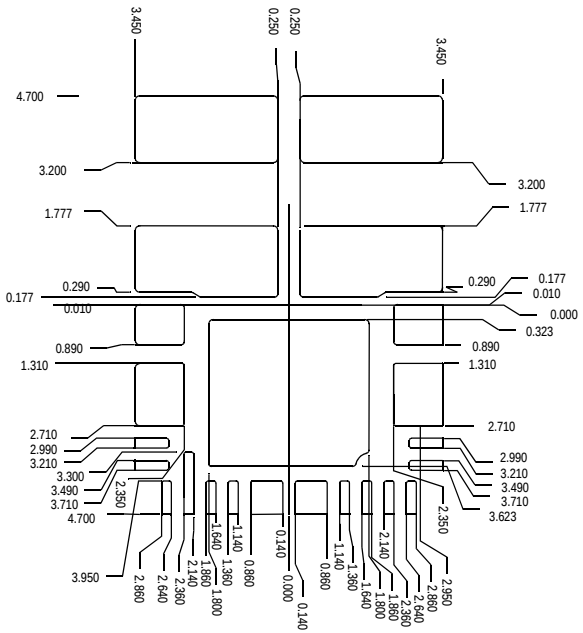
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to ASMEY 14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05.
4. Tiebar shown (if present) is a non-functional feature.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Lead pitches not centered in "y" direction.



STENCIL PATTERN WITH 23 MOSLP TOP VIEW



STENCIL PATTERN WITH 23 MOSLP TOP VIEW



TYPICAL RECOMMENDED LAND PATTERN

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  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com