TWO-PHASE, SYNCHRONOUS BUCK CONTROLLER WITH INTEGRATED MOSFET DRIVERS

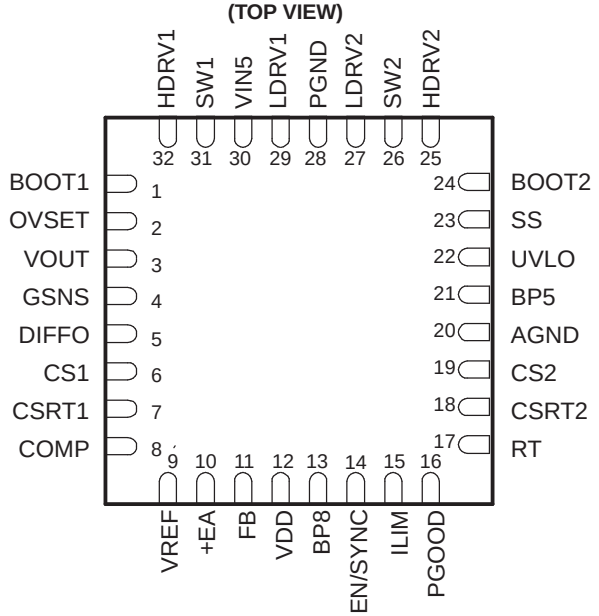
FEATURES

- **Supports 5-V Output**
- **Two-Phase Interleaved Operation**
- **Operates With Pre-Biased Outputs**
- **1-V to 40-V Power Stage Operation Range**
- **Requires VIN5 @ 50 mA (typ) Depending on External MOSFETs and Switching Frequency**
- **10-µA Shutdown Current**
- **Programmable Switching Frequency up to 1 MHz/Phase**
- **Current Mode Control with Forced Current Sharing**
- **Better than 1% Internal 0.7-V Reference**
- **Resistive Divider Sets Direct Output Over Voltage Threshold.**
- **Programmable Input Undervoltage Lockout**
- **True Remote Sensing Differential Amplifier**
- **Resistive or Inductor's DCR Current Sensing**
- **32-Pin QFN Package**
- **Can Be Used with TPS40120 to Provide a 6-Bit Digitally Controlled Output**

APPLICATIONS

- **Point-of-Load Converter**
- **Graphic Cards**
- **Internet Servers**
- **Networking Equipment**
- **Telecommunications Equipment**
- **DC Power Distributed Systems**

RHB PACKAGE
(TOP VIEW)



DESCRIPTION

The TPS40131 is a two-phase synchronous buck controller that is optimized for low-output voltage, high-output current applications powered from a supply between 1 V and 40 V. A multi-phase converter offers several advantages over a single power stage including lower current ripple on the input and output capacitors, faster transient response to load steps, improved power handling capabilities, and higher system efficiency.

Each phase can be operated at a switching frequency up to 1 MHz, resulting in an effective ripple frequency of up to 2 MHz at the input and the output. The two phases operates 180 degrees out-of-phase.

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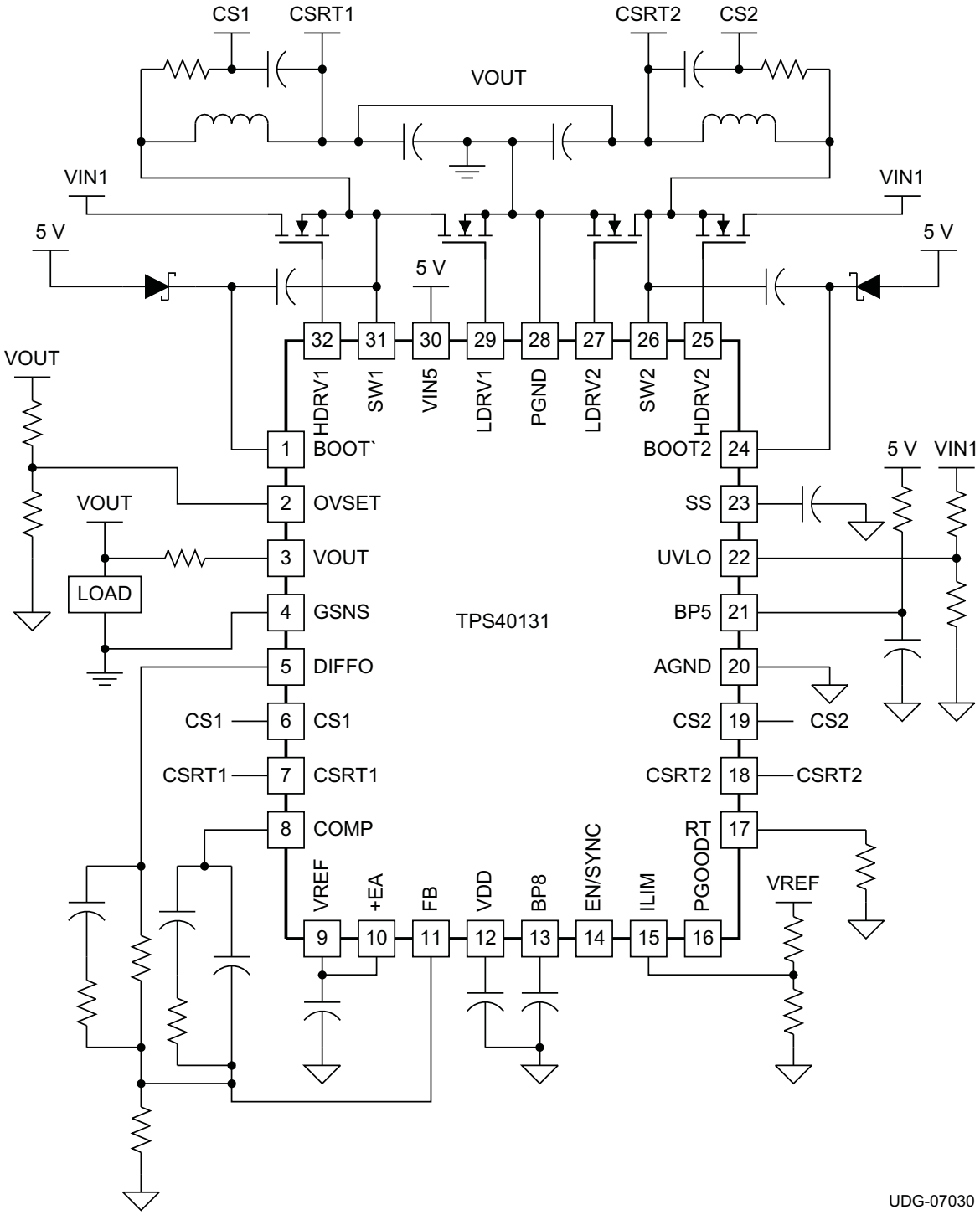
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SIMPLIFIED APPLICATION DIAGRAM



ORDERING INFORMATION

T_A	PACKAGE	PART NUMBER	TAPE AND REEL QUANTITY
-40°C to 85°C	Plastic QFN(RHB)	TPS40131RHBT	250
		TPS40131RHBR	3000

ABSOLUTE MAXIMUM RATING

over operating free-air temperature range unless otherwise noted

			TPS40131	UNITS
	Input voltage range	VDD	-1 to 30	V
		DIFFO, VOUT	V_{BP8}	
		SW1, SW2	-1 to 44	
		BP8	-1 to 10	
		BOOT1, BOOT2, HDRV1, HDRV2	-0.3 to V_{SW} + 6.0	
		All other pins	-0.3 to 6.0	
	Sourcing current	RT	200	µA
T_J	Operating junction temperature range		-40 to 125	°C
T_{stg}	Storage temperature		-55 to 150	
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted(1)

			TPS40131	UNITS
	Input voltage range	VDD	4.5 to 28	V
		DIFFO, VOUT	(V_{BP8}-1)	
		SW1, SW2	-1 to 44	
		BP8	-1 to 8	
		BOOT1, BOOT2, HDRV1, HDRV2	-0.3 to V_{SW} + 5.5	
		All other pins	-0.3 to 5.5	
	Sourcing current	RT	200	µA
T_J	Operating junction temperature range		-40 to 85	°C
T_{stg}	Storage temperature		-55 to 150	
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = -40°C to 85°C, V_{IN} = 5.0 V, V_{DD} = 12.0 V, R_{RT} = 64.9 kΩ, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN5 INPUT SUPPLY						
V_{IN}	Operating voltage range, VIN5		4.5	5.0	5.8	V
I_{IN}	Shutdown current, VIN5	EN/SYNC = GND			5	µA
	Operating current	Outputs switching, No load		1.0	2.0	mA
BP5 INPUT SUPPLY						
	Operating voltage range		4.3	5.0	5.5	V
I_{BP5}	Operating current	Outputs switching, no external FETs		3	5	mA
	Turn-on BP5 rising		3.90	4.25	4.45	V
	Turn-off hysteresis (1)			150		mV
VDD	**INPUT SUPPLY**		4.5		28	V
$BP8_{VBP8}$	Output Voltage	Internal load < 1 mA, No external load		7.5		V
OSCILLATOR/SYNCHRONIZATION						
	Phase frequency accuracy	R_T = 64.9 kΩ	355	400	455	kHz
		R_T = 64.9 kΩ, 0°C ≤ T_J ≤ 85°C	360	400	440	
	Phase frequency set range (1)		100		1200	
	Synchronization frequency range (1)		800		9600	
	Synchronization input threshold (1)			V_{BP5}/2		V
EN/SYNC						
	Enable threshold	Pulse width > 50 ns	0.8	1.0	1.5	V
	Voltage capability (1)			V_{BP5}		
PWM						
	Maximum duty cycle per channel (1)			87.5%		
	Minimum duty cycle per channel (1)			0		
VREF						
	Voltage reference	I_{LOAD} = 100 uA	0.687	0.700	0.709	V
ERROR AMPLIFIER						
V_{FB}	Voltage feedback, trimmed (including differential amplifier)		0.691	0.700	0.705	V
V_{FB}	Voltage feedback, without differential amplifier		0.687	0.700	0.710	
CMRR	Input common mode range (1)		0.0	0.7	2.0	
	Input bias current	V_{FB} = 0.7 V		55	200	nA
	Input offset voltage			0		V
I_{SRC}	Output source current	V_{COMP} = 1.1 V, V_{FB} = 0.6 V	1	2		mA
I_{SINK}	Output sink current	V_{COMP} = 1.1 V, V_{FB} =V_{BP5}	1	2		
V_{OH}	High-level output voltage	I_{COMP} = -1 mA	2.5	2.9		V
V_{OL}	low-level output voltage	I_{COMP} = 1 mA		0.5	0.8	
G_{BW}	Gain bandwidth (1)		3	5		MHz
A_{VOL}	Open loop gain (1)		60	90		dB

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_A = -40°C to 85°C, V_{IN} = 5.0 V, V_{DD} = 12.0 V, R_{RT} = 64.9 kΩ, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START						
I_{SS}	Soft-start source current	32 clocks after EN/SYNC before SS current begins	3.0	5.0	7.0	µA
R_{SS}	Soft-start pull down resistance				500	Ω
V_{SS}	Fault enable threshold voltage		0.95	1.00	1.05	V
CURRENT SENSE AMPLIFIER						
	Input offset voltage	CS1, CS2	-15	-3	10	mV
	Gain transfer to PWM comparator	-100 mV ≤ V_{CS} ≤ 100 mV, V_{CSRT} = 1.5 V		5		V/V
	Gain variance between phases	V_{CS} - V_{CSRTn} = 100 mV	-6%	0	6%	
	Input offset variance between phases	V_{CS} = 0 V	-6	0	6	mV
	Input common mode (1)		0	1	V_{BP8}-0.7	V
	Bandwidth (1)		18			MHz
DIFFERENTIAL AMPLIFIER						
	Gain			1		V/V
	Gain tolerance	V_{OUT} = 5.5 V vs V_{OUT} = 0.7 V, V_{GSNS} = 0 V	-0.5%		0.5%	
CMRR	Common mode rejection ratio	0.7 V ≤ V_{OUT} ≤ 5.5 V	50			dB
	Output source current	V_{OUT} - V_{GSNS} = 2.0 V, V_{DIFFO} ≥ 1.95 V	2	4		mA
	Output sink current	V_{OUT} - V_{GSNS} = 2.0 V, V_{DIFFO} ≥ 2.05 V	2	4		
	Bandwidth (1)		5			MHz
	Input impedance, non-inverting (1)	V_{OUT} to GND		40		kΩ
	Input impedance, inverting (1)	V_{GSNS} to V_{DIFFO}		40		
GATE DRIVERS						
	Source on-resistance, HDRV1, HDRV2	V_{BOOT1} = 5 V, V_{BOOT2} = 5 V, V_{SW1} = 0 V, V_{SW2} = 0 V, Sourcing 100 mA	1.0	2.0	3.5	Ω
	Sink on-resistance, HDRV1, HDRV2	V_{BOOT1} = 5 V, V_{BOOT2} = 5 V, V_{VIN5} = 5 V, V_{SW1} = 0 V, V_{SW2} = 0 V, Sinking 100 mA	0.5	1.0	2.0	
	Source on-resistance, LDRV1, LDRV2	V_{VIN5} = 5 V, V_{SW1} = 0 V, V_{SW2} = 0 V, Sourcing 100 mA	1	2	3.5	Ω
	Sink on-resistance, LDRV1, LDRV2	V_{VIN5} = 5 V, V_{SW1} = 0 V, V_{SW2} = 0 V, Sinking 100 mA	0.30	0.75	1.50	
t_{RISE}	Rise time, HDRV (1)	C_{LOAD} = 3.3 nF		25	75	ns
t_{FALL}	Fall time, HDRV (1)	C_{LOAD} = 3.3 nF		25	75	
t_{RISE}	Rise time, LDRV (1)	C_{LOAD} = 3.3 nF		25	75	
t_{FALL}	Fall time, LDRV (1)	C_{LOAD} = 3.3 nF		25	60	
t_{DEAD}	Dead time (1)	SW falling to LDRV rising		50		
		LDRV falling to SW rising		30		
t_{ON}	Minimum controllable on-time (1)	C_{LOAD} = 3.3 nF		150		
OUTPUT UNDERVOLTAGE FAULT						
	Undervoltage fault threshold	V_{FB} relative to GND	560	588	610	mV
		V_{FB} relative to V_{VREF}	-20%	-16%	-13%	
OUTPUT OVERVOLTAGE SET						
	Overvoltage threshold	V_{OVSET} relative to GND	800	820	840	mV
		V_{OVSET} relative to V_{VREF}	15%	16%	20%	

(1) Ensured by design. Not production tested.

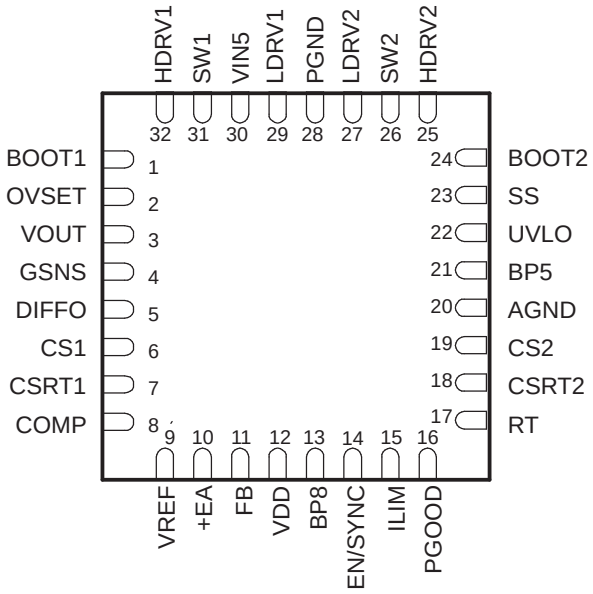
ELECTRICAL CHARACTERISTICS (continued)

T_A = -40°C to 85°C, V_{IN} = 5.0 V, V_{DD} = 12.0 V, R_{RT} = 64.9 kΩ, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RAMP						
	Ramp amplitude (1)		0.4	0.5	0.6	V
	Ramp valley(1)			1.4		
POWER GOOD						
	PGOOD high threshold	V_{FB} relative to V_{REF}	10%		14%	
	PGOOD low threshold	V_{FB} relative to V_{REF}	-14%		-10%	
V_{OL}	Low-level output voltage	I_{PGOOD} = 4 mA		0.35	0.60	V
I_{LEAK}	PGOOD bias current	V_{PGOOD} = 5.0 V		50	80	µA
INPUT UVLO PROGRAMMABLE						
	Input threshold voltage, turn-on		0.9	1.0	1.1	V
	Input threshold voltage, turn-off			0.810		

(1) Ensured by design. Not production tested.

RHB PACKAGE
(TOP VIEW)



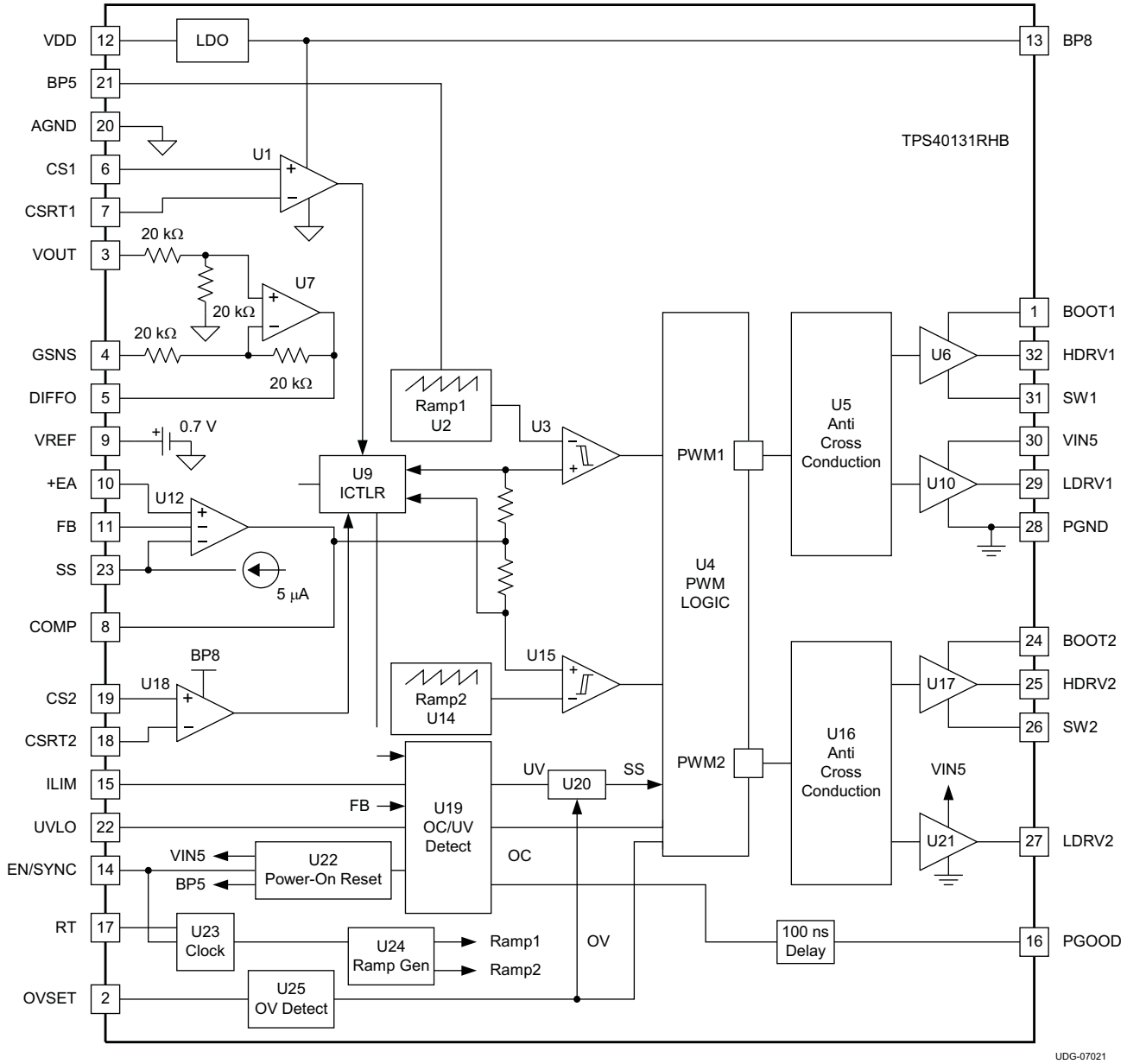
Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	20	-	Low noise ground connection to the device.
BOOT1	1	I	Provides a bootstrapped supply for the high-side FET driver for PWM1, enabling the gate of the high-side FET to be driven above the input supply rail. Connect a capacitor from this pin to SW1 pin and a Schottky diode from this pin to VIN5.
BOOT2	24	I	Provides a bootstrapped supply for the high-side FET driver for PWM2, enabling the gate of the high-side FET to be driven above the input supply rail. Connect a capacitor from this pin to SW2 pin and a Schottky diode from this pin to VIN5.
BP5	21	O	Filtered input from the VIN5 pin. A 10-Ω resistor should be connected between VIN5 and BP5 and a 1.0-µF ceramic capacitor should be connected from this pin to ground.
BP8	13	O	Output of the LDO that powers the differential amplifer and the current sense amplifiers. The voltage is approximately (V_{VDD} -0.2 V) until the output regulates at approximately 7.5 V. Decouple this pin with a minimum capacitance of 1.0-µF to GND.
COMP	8	O	Output of the error amplifier. The voltage at this pin determines the duty cycle for the PWM.
CS1	6	I	These pins are used to sense the inductor phase current. Inductor current can be sensed with an external current sense resistor or by using an external R-C circuit and the inductor's DC resistance. The traces for these signals must be connected directly at the current sense element. See Layout Guidelines for more information.
CS2	19	I	
CSRT1	7	O	Return point of current sense voltage. The traces for these signals must be connected directly at the current sense element. See Layout Guidelines for more information.
CSRT2	18	O	
DIFFO	5	O	Output of the differential amplifier. The voltage at this pin represents the true output voltage without IR drops that result from high-current in the PCB traces. The VOUT and GSNS pins must be connected directly at the point of load where regulation is required. See Layout Guidelines for more information.
+EA	10	I	This is the input to the non-inverting input of the Error Amplifier. This pin is normally connected to the VREF pin and is the voltage that the feedback loop regulates to.
EN/SYNC	14	I	A logic high signal on this input enables the controller operation. A pulsing signal to this pin synchronizes the rising edge of SW to the falling edge of an external clock source.
FB	11	I	Inverting input of the error amplifier. In closed loop operation, the voltage at this pin is the internal reference level of 700 mV. This pin is also used for the PGOOD and undervoltage comparators.
GSNS	4	I	Inverting input of the differential amplifier. This pin should be connected to ground at the point of load.
HDRV1	32	O	Gate drive output for the high-side N-channel MOSFET switch for PWM1. Output is referenced to SW1 and is bootstrapped for enhancement of the high-side switch.

Terminal Functions (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
HDRV2	25	O	Gate drive output for the high-side N-channel MOSFET switch for PWM2. Output is referenced to SW2 and is bootstrapped for enhancement of the high-side switch
ILIM	15	I	Used to set the cycle-by-cycle current limit threshold. If ILIM threshold is reached, the PWM cycle is terminated and the converter delivers limited current to the output. The relationship between ILIM and the maximum phase current is described in Equation 2 and Equation 3. See the Overcurrent Protection section for more details.
LDRV1	29	O	Gate drive output for the low-side synchronous rectifier (SR) N-channel MOSFET for PWM1. See *Layout Considerations* section.
LDRV2	27	O	Gate drive output for the low-side synchronous rectifier (SR) N-channel MOSFET for PWM2. See *Layout Considerations* section.
OVSET	2	I	A resistor divider, on this pin connected to the output voltage sets the overvoltage sense point.
PGOOD	16	O	Power good indicator of the output voltage. This open-drain output connects to a voltage via an external resistor. When the FB pin voltage is between 0.616 V to 0.784 V (88% to 112% of VREF), the PGOOD output is in a high impedance state.
PGND	28	-	Power ground reference for the controller lower gate drivers. There should be a high-current return path from the sources of the lower MOSFETs to this pin.
RT	17	I	Connecting a resistor from this pin to ground sets the oscillator frequency.
SS	23	I	Provides user programmable soft-start by means of a capacitor connected to the pin. If an undervoltage or over current fault is detected the soft-start capacitor cycles 7 times with no switching before a normal soft-start sequence allowed.
SW1	31	I	Connect to the switched node on converter 1. Power return for the channel 1 upper gate driver. There should be a high-current return path from the source of the upper MOSFET to this pin. It is also used by the adaptive gate drive circuits to minimize the dead time between upper and lower MOSFET conduction.
SW2	26	I	Connect to the switched node on converter 2. Power return for the channel 2 upper gate driver. There should be a high-current return path from the source of the upper MOSFET to this pin. It is also used by the adaptive gate drive circuits to minimize the dead time between upper and lower MOSFET conduction.
UVLO	22	O	A voltage divider from VIN to this pin, set to 1V, determines the input voltage that starts the controller.
VDD	12	I	Power input for the LDO linear regulator that powers the differential amplifer and the current sense amplifiers.
VOUT	3	I	Non-inverting input of the differential amplifier. This pin should be connected to VOUT at the point of load.
VREF	9	O	Output of an internal reference voltage. The load may be up to 100-μA DC.
VIN5	30	I	Power input for the device. A 1.0-μF ceramic capacitor should be connected from this pin to ground.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The TPS40131 uses programmable fixed-frequency, peak current mode control with forced phase current balancing. Phase current is sensed by using either the DCR (direct current resistance) of the filter inductors or current sense resistors installed in series with output. The first method involves generation of a current signal with an R-C circuit (shown in the applications diagram). The R-C values are selected by matching time constants of the RC circuit and the inductor time constant, R×C = L/DCR. With either current sense method, the current signal is amplified and superimposed on the amplified voltage error signal to provide current mode PWM control.

Other features include: a true differential output sense amplifier, programmable current limit, programmable output over-voltage set-point, capacitor set soft-start, power good indicator, programmable input undervoltage lockout (UVLO), user programmable operation frequency for design flexibility, external synchronization capability, programmable pulse-by-pulse overcurrent protection, output undervoltage shutdown and restart.

FUNCTIONAL DESCRIPTION (continued)

Startup Sequence

Figure 1 shows a typical start up with the VIN5 and BP5 applied to the controller and then the EN/SYNC being enabled. Shut down occurs when the VIN5 is removed

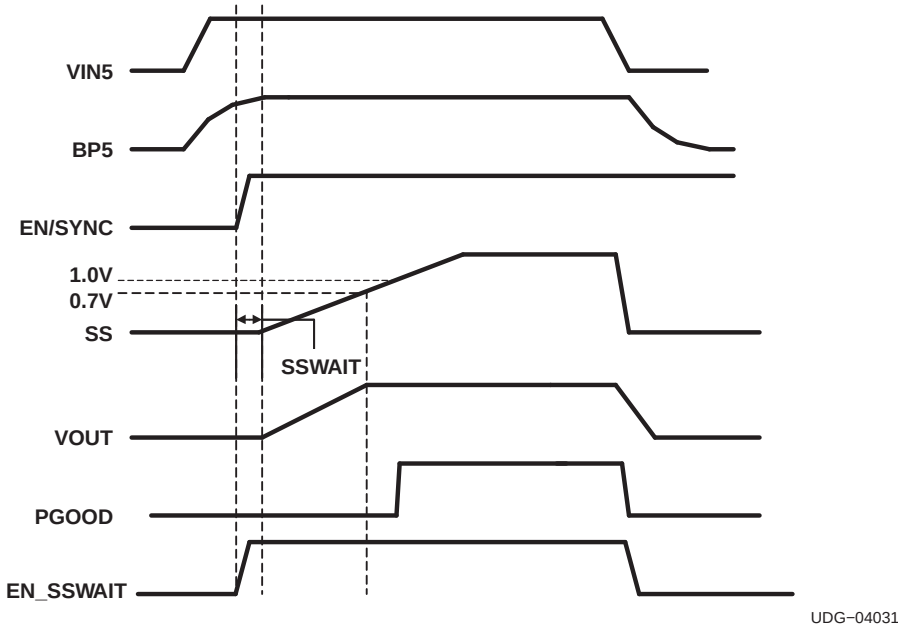


Figure 1. Startup and Shutdown Sequence

Differential Amplifier (U7)

The unity gain differential amplifier with high bandwidth allows improved regulation at a user-defined point and eases layout constraints. The output voltage is sensed between the VOUT and GSNS pins. The output voltage programming divider is connected to the output of the amplifier (DIFFO).

If there is no need for a differential amplifer, the differential amplifier can be disabled by connecting the GSNS pin to the BP5 pin and leaving VOUT and DIFFO open. The voltage programming divider in this case should be connected directly to the output of the converter.

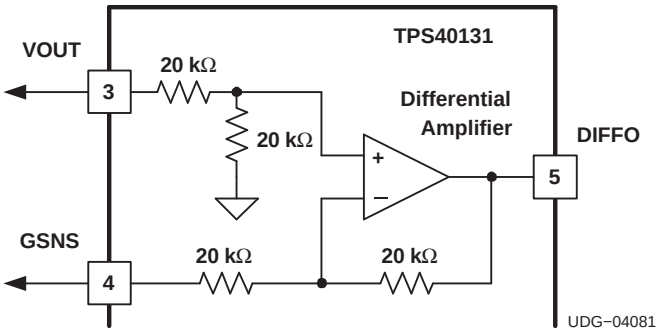


Figure 2. Differential Amplifier Configuration

Because of the resistor configuration of the differential amplifier, the input impedance must be kept very low or there will be error in setting the output voltage.

FUNCTIONAL DESCRIPTION (continued)

Current Sensing and Balancing (U1, U9 and U18)

The controller employs peak current mode control scheme, thus naturally provides certain degree of current balancing. With current mode, the level of current feedback should comply with certain guidelines depending on duty factor known as “slope compensation” to avoid the sub-harmonic instability. This requirement can prohibit achieving a higher degree of phase current balance. To avoid the controversy, a separate current loop that forces phase currents to match is added to the proprietary control scheme. This effectively provides high degree of current sharing independent of the controller’s small signal response and is implemented in U9, I_{CTLR}. The useable range of the controller bandwidth is also extended.

High bandwidth current amplifiers, U1 and U18 can accept as an input voltage either the voltage drop across dedicated precise current sense resistors, or inductor’s DCR voltage derived by an RC network. The wide range of current sense arrangements ease the cost/complexity constraints and provides superior performance compared to controllers utilizing the low-side MOSFET current sensing. See the *Inductor DCR Current Sense* section for more information on selecting component values for the R-C network.

Hiccup Mode

Hiccup mode is a feature that is invoked when certain faults are detected. Hiccup mode allows a time for a fault to clear itself,for instance, a momentary short circuit on the output. The hiccup mode consists of 7 cycles of charging and discharging the soft-start capacitor and then attempting a re-start. If the fault has been cleared, the re-start will cause the output to come up in regulation. If the fault has not been cleared, Hiccup mode is initiated again and another restart will occure after another 7 soft-start cycles.

PowerGood

The PGOOD pin indicates when the inputs and output are within their specified ranges of operation. Also monitored are the EN/SYNC and SS pins. PGOOD has high impedance when indicating inputs and outputs are within specified limits and is pulled low to indicate an out-of-limits condition. .

Soft-Start

A capacitor connected to the soft start pin (SS) sets the power-up time. When EN is high and POR is cleared, the calibrated current source starts charging the external soft start capacitor. The PGOOD pin is held low during the start up. The rising voltage across the capacitor serves as a reference for the error amplifier, U12. When the soft-start voltage reaches the level of the reference voltage, the converter’s output reaches the regulation point and further voltage rise of the soft start voltage has no effect on the output. When the soft start voltage reaches 1.0 V, the power good (PGOOD) function is cleared to be reported on the PGOOD pin. Normally the PGOOD pin goes high at this time. Equation 1 is used to calculate the value of the soft-start capacitor.

$$t_{SS} = \frac{0.7 \times C_{SS}}{5 \times 10^{-6}} \tag{1}$$

Overcurrent Protection

The overcurrent function, U19, monitors the output of current sense amplifiers U1 and U18. These currents are converted to voltages and compared to the voltage on the ILIM pin. The relationship between the maximum phase current and the current sense resistance is given in the following equation. In case a threshold of $V_{ILIM}/3.75$ is exceeded the PWM cycle on the associated phase is terminated. The overcurrent threshold, $I_{PH(max)}$, and the voltage to set on the ILIM pin is determined by Equation 2 and Equation 3.

$$V_{ILIM} = 3.75 \times I_{PH(max)} \times R_{CS} \tag{2}$$

$$I_{PH(max)} = \frac{I_{OUT}}{2} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L_{OUT} \times f_{SW} \times V_{IN}} \tag{3}$$

where

- $I_{PH(max)}$ is a maximum value of the phase current allowed
- I_{OUT} is the total maximum DC output current
- R_{CS} is a value of the current sense resistor used or the DCR value of the output inductor, L_{OUT}

FUNCTIONAL DESCRIPTION (continued)

If the overcurrent condition persists, both phases have PWM cycles terminated by the overcurrent signals. This puts a converter in a constant current mode with the output current programmed by the ILIM voltage. A counter is incremented for each PWM cycle in which an overcurrent event is detected. The counter is reset every 32 PWM cycles. If the counter accumulates a count of 7 before being reset, the converter enters a hiccup mode. The HDRV and LDRV signals are set low during the hiccup mode.

The SS capacitor serves as a hiccup timing capacitor controlled by U20, the fault control circuit. The soft-start pin is periodically charged and discharged by U20. After seven hiccup cycles, the controller attempts another soft-start cycle to restore normal operation. If the overload condition persists, the controller returns to the hiccup mode. This condition may continue indefinitely. In such conditions the average current delivered to the load is approximately 1/8 of the set overcurrent value.

Overvoltage Protection, Non-Latching

The voltage on OVSET is compared with 0.817 V, 16% higher than VREF, in U25 to determine the output overvoltage point. When an overvoltage is detected, the output drivers command the upper MOSFETs off and the lower MOSFETs on. If the overvoltage condition has been cleared, the output comes up and normal operation continues. Turning the lower MOSFET on may cause the output to reach an undervoltage condition and enter the hiccup mode. Using a voltage divider with the same ratio, that sets the output voltage, an output overvoltage is declared when the output rises 16% above nominal.

Output Undervoltage Protection

If the output voltage, as sensed by U19 on the FB pin becomes less than 0.588 V, the undervoltage protection threshold (84% of VREF), the controller enters the hiccup mode.

Programmable Input Undervoltage Lockout Protection

A voltage divider that sets 1V on the UVLO pin determines when the controller starts operating. Operation commences when the voltage on the UVLO pin exceeds 1.0 V. If the voltage on the UVLO pin falls to 0.81 V, the controller is turned off and the HDRV and LDRV signals are set low.

Power-On Reset (POR)

The power-on reset (POR) function, U22, insures the VIN5 and BP5 voltages are within their regulation windows before the controller is allowed to start.

Fault Masking Operation

If the SS pin voltage is externally limited below the 1-V threshold, the controller does not respond to most faults and the PGOOD output is always low. Only the overcurrent function remains active. The overcurrent protection still continues to terminate PWM cycle every time when the threshold is exceeded but the hiccup mode is not entered.

Fault Conditions and MOSFET Control

Table 1 shows a summary of the fault conditions and the state of the MOSFETs.

Table 1. Fault Condifions

FAULT MODE	UPPER MOSFET	LOWER MOSFET
EN/SYNC = LOW	OFF	OFF
FIXED UVLO, V_{BP5} < 4.25 V	OFF	OFF
Programmable UVLO, < 1.0 V	OFF	OFF
Output undervoltage	OFF, Hiccup mode	OFF, Hiccup mode
Output overvoltage	OFF	ON
Output overcurrent	OFF, Hiccup mode	OFF, Hiccup mode

Setting the Switching Frequency

The clock frequency is programmed by the value of the timing resistor connected from the RT pin to ground. See Equation 4.

$$R_T = 0.8 \times \left[\left(\frac{36 \times 10^3}{f_{PH}} \right) - 9 \right] \tag{4}$$

f_{PH} is a single phase frequency, kHz. The RT resistor value is expressed in kΩ. See Figure 3.

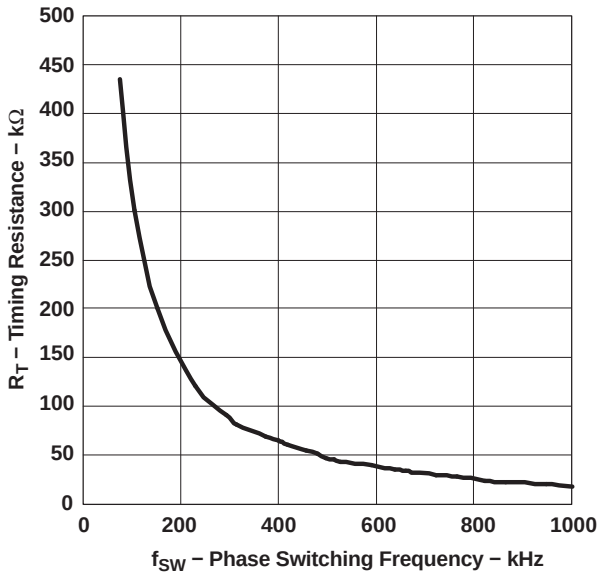


Figure 3. Phase Switching Frequency vs. Timing Resistance

EN/SYNC Function

The output ripple frequency is twice that of the single-phase frequency. The switching frequency of the controller can be synchronized to an external clock applied to the EN/SYNC pin. The external clock synchronizes the rising edge of HDRV and the falling edge of an external clock source. The switching frequency is one-eighth of the external clock frequency.

Setting Overcurrent Protection

Setting the overcurrent protection is given in the following equations. Care must be taken when calculating V_{ILIM} to include the increase in R_{CS} caused by the output current as it approaches the overcurrent trip point. The DCR (R_{CS} in the equation) of the inductor increases approximately 0.39% per degree Centigrade.

$$V_{ILIM} = 3.75 \times I_{PH(max)} \times R_{CS} \tag{5}$$

$$I_{PH(max)} = \frac{I_{OUT}}{2} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L_{OUT} \times f_{SW} \times V_{IN}} \tag{6}$$

where

- $I_{PH(max)}$ is a maximum value of the phase current allowed
- I_{OUT} is the total maximum DC output current
- L_{OUT} is the output inductor value
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- R_{CS} is a value of the current sense resistor used or the DCR value of the output inductor, L_{OUT}

Resistor Divider Calculation for VOUT, ILIM, OVSET and UVLO

Use Figure 4 for setting the output voltage, current limit voltage and overvoltage setting voltage. Select R_{BIAS} using Equation 7. With a voltage divider from V_{REF}, select R6 using Equation 8. WIth a voltage from DIFFO select R4 using Equation 9. With a voltage divider from V_{IN}, select R8 using Equation 10.

$$R_{BIAS} = 0.7 \times \frac{R1}{\left(V_{OUT} - 0.7\right)} \tag{7}$$

$$R6 = R5 \times \frac{V_{ILIM}}{\left(0.7 - V_{ILIM}\right)} \tag{8}$$

$$R4 = 0.812 \times \frac{R3}{\left(V_{OUT(ov)} - 0.812\right)} \tag{9}$$

$$R8 = 1.0 \times \frac{R7}{\left(V_{IN} - 1.0\right)} \tag{10}$$

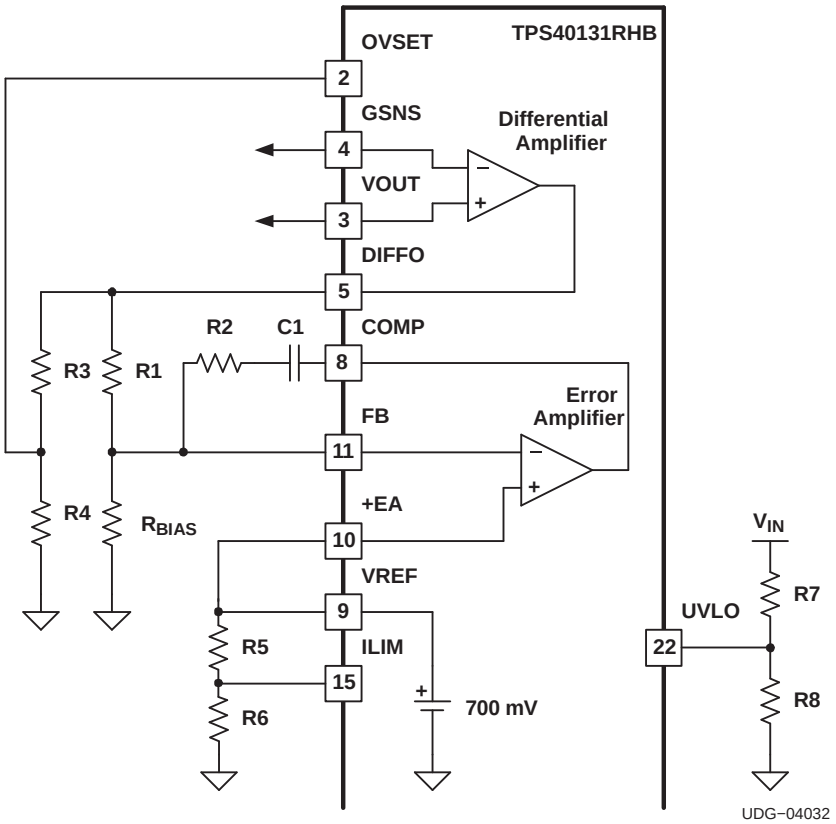


Figure 4. Use for Resistor Divider Calculations

INDUCTOR DCR CURRENT SENSE

The preferred method for sampling the output current for the TPS40131 is known as the *inductor DCR* method. This is a *lossless* approach, as opposed to using a discrete current sense resistor which occupies board area and impacts efficiency as well. The inductor DCR implementation is shown in Figure 5.

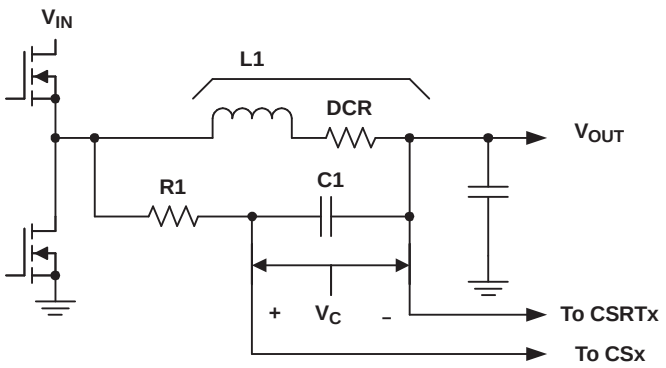


Figure 5. Inductor DCR Current Sense Approach

The inductor L1 consists of inductance, L, and resistance, DCR. The time constant of the inductor: L / DCR should equal the R1×C1 time constant. Then choosing a value for C1 (0.1 µF is a good choice) solving for R1 is shown in Equation 11.

$$R1 = \frac{L1}{DCR \times C1} \tag{11}$$

The voltage into the current sense amplifier of the controller , V_C, is calculated in Equation 12.

$$V_C = \left(V_{IN} - V_{OUT}\right) \times \frac{V_{OUT}}{R1 \times C1 \times f_{SW} \times V_{IN}} + I_{OC} \times DCR \tag{12}$$

As the DC load increases the majority of the voltage, V_C, is determined by (I_{OC} ×DCR), where I_{OC} is the per phase DC output current. It is important that at the overcurrent set point that the peak voltage of V_C does not exceed 60 mV, the maximum differential input voltage. If the voltage V_C exceeds 60 mV, a resistor, R2,can be added in parallel with C1 as shown in Figure 6. Adding R2 reduces the equivalent inductor DCR by the ratio shown in Equation 14

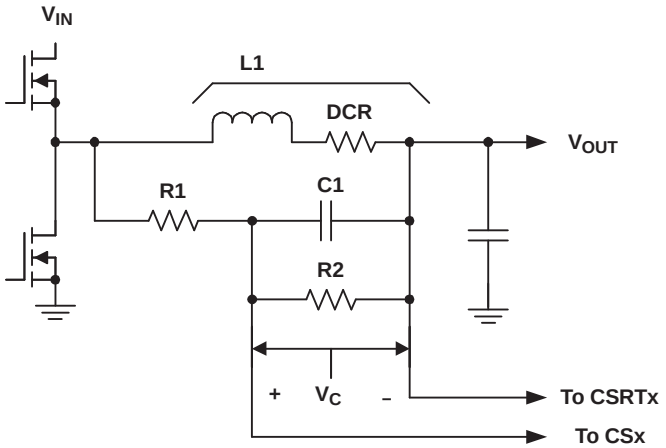


Figure 6. Using Resistor R2 to Reduce the Current Sense Amplifier Voltage

The parallel combination of R1 and R2 is shown in Equation 13.

$$R1 \parallel R2 = \frac{L1}{DCR \times C1} \tag{13}$$

The ratio shown in Equation 14 provides the required voltage attenuation.

$$\frac{R2}{R1 + R2} \tag{14}$$

APPLICATION INFORMATION

LAYOUT CONSIDERATIONS

Power Stage

A synchronous BUCK power stage has two primary current loops. One is the input current loop that carries high AC discontinuous current . The other is the output current loop that carries high DC continuous current.

The input current loop includes the input capacitors, the main switching MOSFET, the inductor, the output capacitors and the ground path back to the input capacitors. To keep this loop as small as possible, it is generally good practice to place some ceramic capacitance directly between the drain of the main switching MOSFET and the source of the synchronous rectifier (SR) through a power ground plane directly under the MOSFETs.

The output current loop includes the SR MOSFET, the inductor, the output capacitors, and the ground return between the output capacitors and the source of the SR MOSFET. As with the input current loop, the ground return between the output capacitor ground and the source of the SR MOSFET should be routed under the inductor and SR MOSFET to minimize the power loop area.

The SW node area should be as small as possible to reduce the parasitic capacitance and minimize the radiated emissions. The gate drive loop impedance (HDRV-gate-source-SW and LDRV-gate-source- GND) should be kept to as low as possible. The HDRV and LDRV connections should widen to 20 mils as soon as possible out from the device's pin.

Device Peripheral

The TPS40131 provides separate signal ground (GND) and power ground (PGND) pins. It is required to separate properly the circuit grounds. The return path for the pins associated with the power stage should be through PGND. The other pins especially for those sensitive pins such as FB, RT and ILIM should be through the low noise GND. The GND and PGND plane are suggested to be connected at the output capacitor with single 20 mil trace.

A minimum 0.1-µF ceramic capacitor must be placed as close to the VDD pin and GND as possible with at least 15-mil wide trace from the bypass capacitor to the GND. A 1-µF ceramic capacitor should be placed as close to VIN5 pin and GND as possible.

BP5 is the filtered input from the VIN5 pin. A 10 Ω resistor should be connected between VIN5 and BP5 and a 1-µF ceramic capacitor should be connected from BP5 to GND. Both components should be as close to BP5 pin as possible.

When DCR sensing method is applied, the sensing resistor is placed close to the SW node. It is connected to the inductor with Kelvin connection. The sensing traces from the power stage to the device should be away from the switching components. The sensing capacitor should be placed very close to the CS and CSRT pins. The frequency setting resistor should be placed as close to RT pin and GND as possible.

The VOUT and GSNS pins should be directly connected to the point of load where the voltage regulation is required. A parallel pair of 10-mil traces connects the regulated voltage back to the chip. They should be away from the switching components. The PowerPAD should be electrically connected to GND. Figure 7 shows the device peripheral schematic and Figure 8 shows the suggested layout.

APPLICATION INFORMATION (continued)

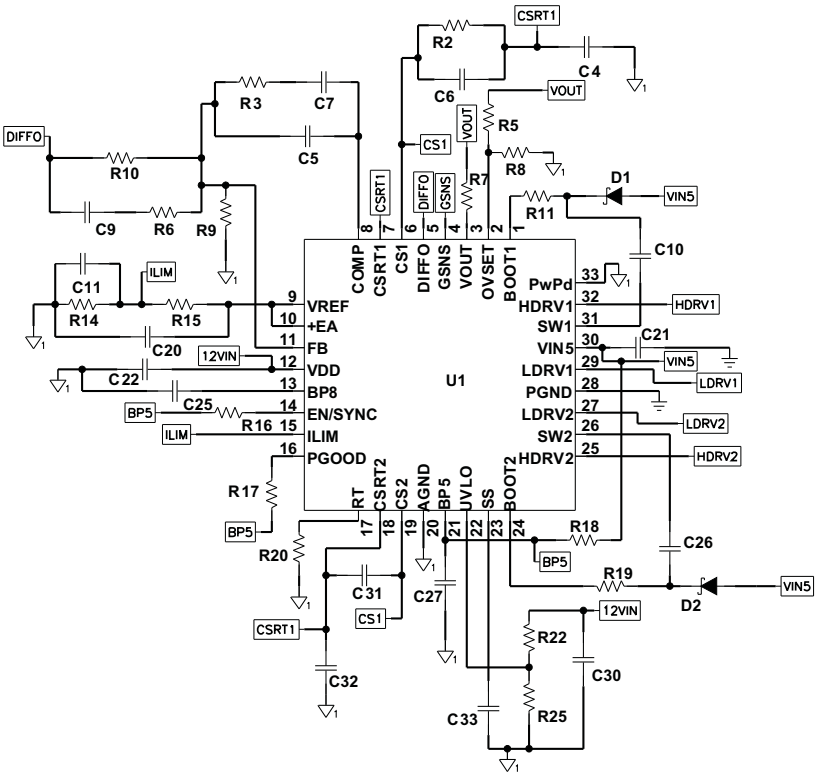


Figure 7. TPS40131 Peripheral Schematic

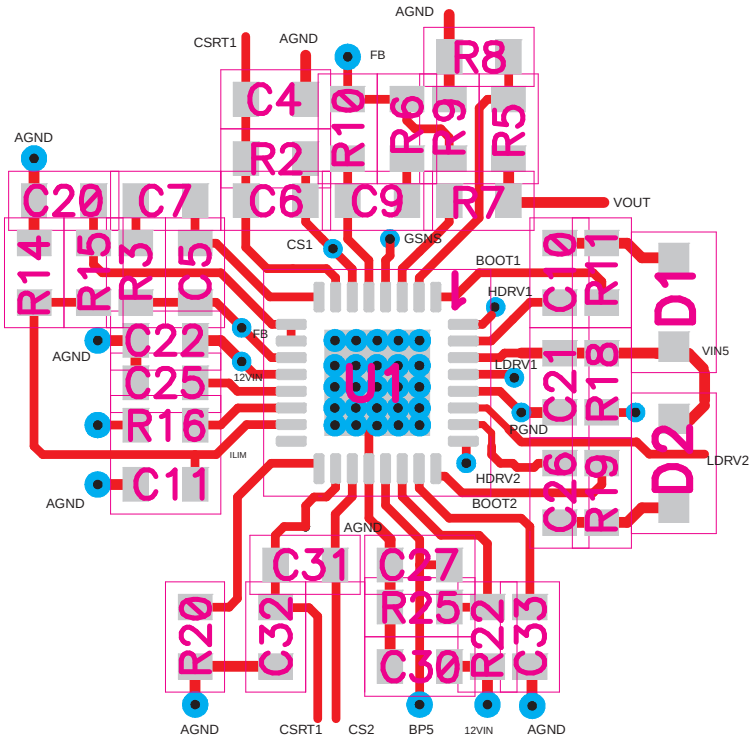


Figure 8. TPS40131 Recommended Layout for Peripheral Components

APPLICATION INFORMATION (continued)

PowerPAD™ Layout

The PowerPAD™ package provides low thermal impedance for heat removal from the device. The PowerPAD™ derives its name and low thermal impedance from the large bonding pad on the bottom of the device. The circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depend on the size of the PowerPAD™ package.

Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0.33 mm (13 mils) works well when 1-oz. copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter plus 0.1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. Refer to *PowerPAD™ Thermally Enhanced Package* (SLMA002) for more information on the PowerPAD™ package.

DESIGN EXAMPLE

Two Phase Single Output Configuration from 12 V to 1.5 V DC/DC Converter Using a TPS40131

The following example illustrates the design process and component selection for a two phase single output synchronous buck converter using TPS40131. The design goal parameters are given in the table below.

Design Goal Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		10.8	12.0	13.2	V
V_{OUT}	Output voltage			1.5		
V_{RIPPLE}	Output ripple	I_{OUT} = 40 A		30		mV
I_{OUT}	Output current			40		A
f_{SW}	Switching frequency			350		kHz

Setp 1: Inductor Selection

The inductor is determined by the desired ripple current. The required inductor is calculated using Equation 15.

$$L = \frac{V_{IN(max)} - V_{OUT}}{I_{RIPPLE}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{f_{SW}} \tag{15}$$

Typically the peak-to-peak inductor current I_{RIPPLE} is selected to be around 20% of the rated output current. In this design, I_{RIPPLE} is targeted at 23% of I_{PHASE}. The calculated inductor is 0.815 µH and in practical a 0.82-µH, 30-A inductor with 2-mΩ DCR from Vishay is selected. The real inductor ripple current is 4.63 A.

Step 2: Output Capacitor Slection

The output capacitor is typically selected by the output load transient response requirement. Equation 16 estimates the minimum capacitor to reach the undervoltage requirement with load step up. Equation 17 estimates the minimum capacitor for overvoltage requirement with load step down. When $V_{IN(min)} < 2 \times V_{OUT}$, the minimum output capacitance can be calculated using Equation 16. Otherwise, Equation 17 is used.

$$C_{OUT(min)} = \frac{\frac{1}{2} \times \left(I_{TRAN(max)}\right)^2 \times L}{\left(V_{IN(min)} - V_{OUT}\right) \times V_{UNDER}} \tag{16}$$

$$C_{OUT(min)} = \frac{\frac{1}{2} \times \left(I_{TRAN(max)}\right)^2 \times L}{\left(V_{OUT} \times V_{OVER}\right)} \tag{17}$$

In this design, $V_{IN(min)}$ is much larger than $2 \times V_{OUT}$, so Equation 17 is used to determine the minimum capacitance. Based on a 15-A load transient with a maximum of 80-mV deviation, a minimum 1-mF output capacitor is required. In the design, six 180-µF, 6.3-V SP capacitors are selected to meet this requirement. Each capacitor has an ESR of 5 mΩ.

Due to the interleaving of channels, the total output ripple current is smaller than the ripple current from a single phase. The ripple cancellation factor is expressed in Equation 18.

$$\Delta I_{OUT}(D) = \frac{|1 - 2 \times D| \times |2 - 2 \times D|}{|1 - 2 \times D| + 1} \tag{18}$$

where

- D is the duty cycle for a single phase

The maximum output ripple current is calculated in Equation 19.

$$I_{RIPPLE} = \frac{V_{OUT}}{L \times f_{sw}} \times \Delta I_{OUT}(D) = 4.04\,A \tag{19}$$

With 1.08-mF output capacitance, the ripple voltage at the capacitor is calculated to be 1.34 mV. In the specification, the output ripple voltage should be less than 30 mV, so based on the following equation, the required maximum ESR is 7.1 mΩ. The selected capacitors can meet this requirement.

$$ESR_{Co} = \frac{V_{RIPPLE(TotOUT)} - V_{RIPPLE(COUT)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(TotOUT)} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times f_{SW}}\right)}{I_{RIPPLE}} \tag{20}$$

Step 3: Input Capacitor Selection

The input voltage ripple depends on input capacitance and ESR. The minimum capacitor and the maximum ESR can be estimated using Equation 21.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{RIPPLE(CIN)} \times V_{IN} \times f_{SW}} \tag{21}$$

$$ESR_{Cin} = \frac{V_{RIPPLE(CinESR)}}{I_{OUT} + \left(\left(\frac{1}{2}\right) \times I_{RIPPLE}\right)} \tag{22}$$

For this design, assume $V_{RIPPLE(Cin)}$ is 60 mV and $V_{RIPPLE(CinESR)}$ is 30 mV, so the calculated minimum capacitance is 120-µF and the maximum ESR is 1.35 mΩ. Choosing six 22-µF, 16V, 2-mΩ ESR ceramic capacitors meets this requirement.

Another important thing for the input capacitor is the RMS ripple current rating. Due to the interleaving of multi-phase, the input RMS current is reduced. The input ripple current RMS value over load current is calculated using Equation 23.

$$\Delta I_{IN}(D) = \sqrt{D \times (0.5 - D)} \times I_{OUT} \tag{23}$$

So in this design, the maximum input ripple RMS current is calculated to be 8.96 A with the minimum input voltage. It is about 35% reduction compared with a 40-A single-phase converter design. Each selected ceramic capacitor has a RMS current rating of 4.3 A, so it is sufficient to meet this requirement.

Step 4: MOSFET Selection

The MOSFET selection determines the converter efficiency. In this design, the duty cycle is very small so that the high-side MOSFET is dominated with switching losses and the low-side MOSFET is dominated with conduction loss. To optimize the efficiency, choose smaller gate charge for the high-side MOSFET and smaller $R_{DS(on)}$ for the low-side MOSFET. Renesas HAT2167H and HAT2164H are selected as the high-side and low-side MOSFET respectively.

In the following calculations, only the losses for one phase are shown. The power losses in the high-side MOSFET is calculated with the following equations.

The RMS current in the high-side MOSFET is shown in Equation 24.

$$I_{SWrms} = \sqrt{D \times \left((I_{OUT})^2 + \frac{(I_{RIPPLE})^2}{12}\right)} = 7.08 \tag{24}$$

The $R_{DS(on)(sw)}$ is 9.3 mΩ when the MOSFET gate voltage is 4.5 V. The conduction loss is shown in Equation 25.

$$P_{SWcond} = (I_{SWrms})^2 \times R_{DS(on)(sw)} = 0.467\,W \tag{25}$$

The switching loss is shown in Equation 26.

$$P_{SW(sw)} = \frac{I_{PK} \times V_{IN} \times f_{SW} \times R_{DRV} \times (Qgd_{sw} + Qgs_{sw})}{Vgtdrv} = 0.438\,W \tag{26}$$

The calculated total loss is the high-side MOSFET is shown in Equation 27.

$$P_{SW(tot)} = Psw_{(cond)} + P_{SW(SW)} = 0.935\,W \tag{27}$$

The power losses in the low-side SR MOSFET is calculated using <CR>.

The RMS current in the low-side MOSFET is calculated using Equation 28.

$$I_{SRrms} = \sqrt{(1-D) \times \left((I_{OUT})^2 + \frac{(I_{RIPPLE})^2}{12} \right)} = 18.7A \tag{28}$$

The $R_{DS(on)(sr)}$ of each HAT2164H is 4.4mΩ when the gate voltage is 4.5 V. Two HAT2164H are used in parallel to reduce the conduction loss. The conduction loss in the low-side MOSFETs is shown in Equation 29.

$$P_{SR(cond)} = (I_{SRrms})^2 \times \left(\frac{R_{DS(on)(sr)}}{2} \right) = 0.77\,W \tag{29}$$

The total power loss in the body diode is shown in Equation 30.

$$P_{DIODE} = 2 \times I_{OUT} \times t_D \times V_f \times f_{SW} = 0.49\,W \tag{30}$$

Therefore, the calculated total loss in the SR MOSFETs is as described in Equation 31.

$$P_{SR(tot)} = P_{SR(cond)} + P_{DIODE} = 1.26\,W \tag{31}$$

Step 5: Peripheral Component Design

RT (Pin 17) Switching Frequency Setting

$$R_T = 0.8 \times \left(\frac{36 \times (10)^3}{f_{SW}} - 9 \right) = 75k\Omega \tag{32}$$

In Equation 32, the phase switching frequency and it is 350 kHz here.

SS (Pin 23) Soft-Start

To obtain a 3-ms soft-start time, calculate C_{SS} which is connected between SS and GND.

$$C_{SS} = \frac{t_{SS}}{140 \times (10)^3} = \frac{3 \times (10)^{-3}}{140 \times (10)^3} = 21nF \tag{33}$$

FB (Pin 11) Output Voltage Setting

Select the top resistor to be 10 kΩ, calculate the bottom resistor R_{BAIS} using Equation 34.

$$R_{BIAS} = 0.7 \times \left(\frac{10 \times (10)^3}{(V_{OUT} - 0.7)} \right) = 8.75k\Omega \tag{34}$$

(Pin 6, Pin 7, Pin 18 and Pin 19) Current Sensing Network Design

In this design, the lossless inductor DCR sensing is applied. Choose the sense capacitor a value for 0.1 µF, and calculate the sense resistor R with Equation 35 and Equation 36.

$$R = \frac{L}{DCR \times C} = 6\,k\Omega \tag{35}$$

The simplified equation to determine if the design produces sub-harmonics is shown in Equation 35.

$$\frac{L}{DCR} > \frac{V_{IN} \times 6}{2 \times V_{RAMP} \times f_{SW}} \tag{36}$$

This condition is satisfied in this design. Both CSRT1 and CSRT2 are recommended to connect to GND with a 1-µF capacitor for the purpose of eliminating noise.

ILIM (Pin 15) Current Limit

The overcurrent protection level is calculated with equations below.

$$I_{PK} = I_{OC(dc)} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} = 27.32\,A \tag{37}$$

$$V_{ILIM} = 3.75 \times I_{PK} \times DCR = 205\,mV \tag{38}$$

$I_{OC(dc)}$ is the DC overcurrent protection level for each phase. In this design, it is 25 A per phase. DCR is 2 mΩ. A resistor divider is connected from V_{REF} (pin 9) to GND to provide an accurate V_{ILIM} voltage. Choose a value of 10 kΩ for the top resistor, and then the bottom resistor is calculated using Equation 39.

$$R_B = V_{LIM} \times \left(\frac{10 \times (10)^3}{V_{REF} - V_{LIM}} \right) = 4.02\,k\Omega \tag{39}$$

OVSET (Pin 2) Output Voltage Setting

A resistor divider is connected from V_{OUT} to GND to set the overvoltage protection threshold. In this design, the resistor divider is the same as the output voltage setting resistor divider, so the OVSET level is 16% of the set output voltage.

UVLO (Pin 22) Undervoltage Lockout

UVLO is connected to the input voltage and GND with a resistor divider. The resistor connected to V_{IN} is chosen to be 10 kΩ and the resistor connected to GND is selected to be a value of 2.49 kΩ. When the input voltage is higher than 5 V, the chip is enabled.

PGOOD (Pin 16) Powergood

PGOOD is connected to BP5 with a 10-kΩ resistor.

VOUT, GSNS and DIFFO (Pin 3) (Pin 4) (Pin 5)

VOUT and GSNS are connected to the remote sensing output connector. DIFFO is connected to the feedback resistor divider. If the differential amplifier is not used, VOUT and GSNS should be grounded, and DIFFO is left open.

BOOT1, BOOT2, SW1, SW2 (Pin 1) (Pin 24) (Pin 31) (Pin 26)

A bootstrap capacitor is connected between the BOOT1 and SW1 pin or between BOOT2 and SW2 pin. The bootstrap capacitor depends on the total gate charge of the high-side MOSFET and the amount of droop allowed on the bootstrap capacitor.

$$C_{BOOT} = \frac{Qg}{\Delta V} = 85\,nF \tag{40}$$

where

- Qg is 17nC
- ΔV is 0.2 V

For this application, a 0.1-µF capacitor is selected. To reduce the turn on speed of the high-side MOSFET and control the ringing, a 2-Ω resistor is placed in series with the BOOT pin.

EN/SYNC (Pin 14) Enable and Synchronization

This pin is either tied to BP5 to enable the chip or connected to an external clock.

VREF EA+ (Pin 9) (Pin 10) Voltage Reference and Error Amplifier

VREF and EA+ are directly connected together. A 0.1-µF decoupling capacitor is recommended.

VDD, VIN5, BP5, BP8, AGND, PGND, PwPd (Pin 12) (Pin 30) (Pin 21) (Pin 13) (Pin 20) (Pin 28) (Pin 33)

VDD is directly connected to VIN and a 0.1-µF decoupling capacitor is recommended.

VIN5 is connected to external +5 V and a 100-µF bulk capacitor and a 1-µF decoupling capacitor are recommended.

BP5 is filtered from VIN5. A 10-Ω resistor and a 0.1-µF capacitor are recommended for the low pass filter.

BP8 is decoupled with a 0.1-µF capacitor to GND. A

GND and PwPd are tied to analog GND and PGND is tied to power GND.

Feedback Compensator Design

Peak current mode control method is employed in the controller. A small signal model is developed from the COMP signal to the output.

$$G_{VC(s)} = \frac{1}{DCR \times Ac} \times \frac{1}{s \times \tau_s + 1} \times \frac{(s \times C_{OUT} \times ESR + 1) \times R_{OUT}}{s \times C_{OUT} \times R_{OUT} + 1} \tag{41}$$

The time constant, τ_S, is defined by Equation 42.

$$\tau_s = \frac{T}{\ell n\left(\frac{\left(\left(\frac{V_{RAMP}}{T}\right) + \left(\frac{V_{IN} - V_{OUT}}{L}\right) \times DCR \times Ac\right)}{\left(\frac{V_{RAMP}}{T}\right) - \left(\frac{V_{OUT}}{L}\right) \times DCR \times Ac}\right)} \tag{42}$$

The low frequency pole is calculated in Equation 43.

$$f_{VCP1} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{OUT}} = 3.84\,kHz \tag{43}$$

Another pole from control to output is calculated in Equation 44.

$$f_{VCP2} = \frac{1}{2 \times \pi \times \tau_S} = 46.3\,kHz \tag{44}$$

The ESR zero is calculated in Equation 45.

$$f_{ESR} = \frac{1}{2 \times \pi \times C_{OUT} \times ESR} = 176.8\,kHz \tag{45}$$

In this design, a Type III compensator is employed to compensate the loop.

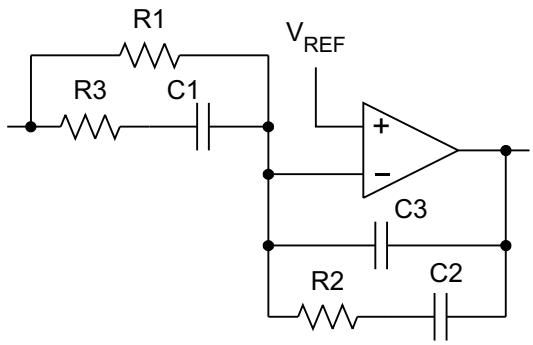


Figure 9. Type III Compensator

The compensator transfer function is shown in Equation 46.

$$G_{C(s)} = \left(\frac{1}{(R1 \times (C2 + C3))}\right) \times \frac{(s \times (R1 + R3) \times C1 + 1) \times (s \times R2 \times C2 + 1)}{s \times (s \times R3 \times C1 + 1) \times \left(s \times R2 \times \left(\frac{C2 \times C3}{C2 + C3}\right) + 1\right)} \tag{46}$$

The loop gain transfer function is shown in Equation 47.

$$T_{V(s)} = G_{C(s)} \times G_{VC(s)} \tag{47}$$

Assume the desired crossover frequency is 20 kHz. Place one zero at f_{VCP1} and another zero at f_{VCP2}, then place one pole at $f_{ESR}$and another pole at f_{SW}. The compensator gain is then calculated to achieve the desired bandwidth. In this design, the compensator gain, pole and zero are selected using the following equations:

$$f_{P1} = \frac{1}{2 \times \pi \times R3 \times C1} = f_{ESR} \tag{48}$$

$$f_{P2} = \frac{1}{2 \times \pi \times R2 \times \left(\frac{C2 \times C3}{C2 + C3}\right)} = f_{SW} \tag{49}$$

$$f_{Z1} = \frac{1}{2 \times \pi \times R2 \times C2} = f_{VCP1} \tag{50}$$

$$f_{Z2} = \frac{1}{2 \times \pi \times (R1 + R3) \times C1} = f_{VCP2} \tag{51}$$

$$\left|T_V(j \times 2 \times \pi \times f_C)\right| = 1 \tag{52}$$

From Equation 52 the compensator gain is solved as 2.09×10^4.

$$A_{CM} = \left(\frac{1}{R1 \times (C2 + C3)}\right) = 2.09 \times (10)^4 \tag{53}$$

Set R1 equal to 10 kΩ, and then calculate all the other components.

- R2 = 8.4 kΩ
- R3 = 3.5 kΩ
- C1 = 260 pF
- C2 = 4.7 nF
- C3 = 50 pF

In the real lab practice, the final components are selected as following to increase the phase margin and reduce PWM jitter.

- R1 = 10 kΩ
- R2 = 5 kΩ
- R3 = 3 kΩ
- C1 = 470 pF
- C2 = 4.7 nF
- C3 = 47 pF

Design Example Summary

Figure 10 shows the schematic summarizes the above design.

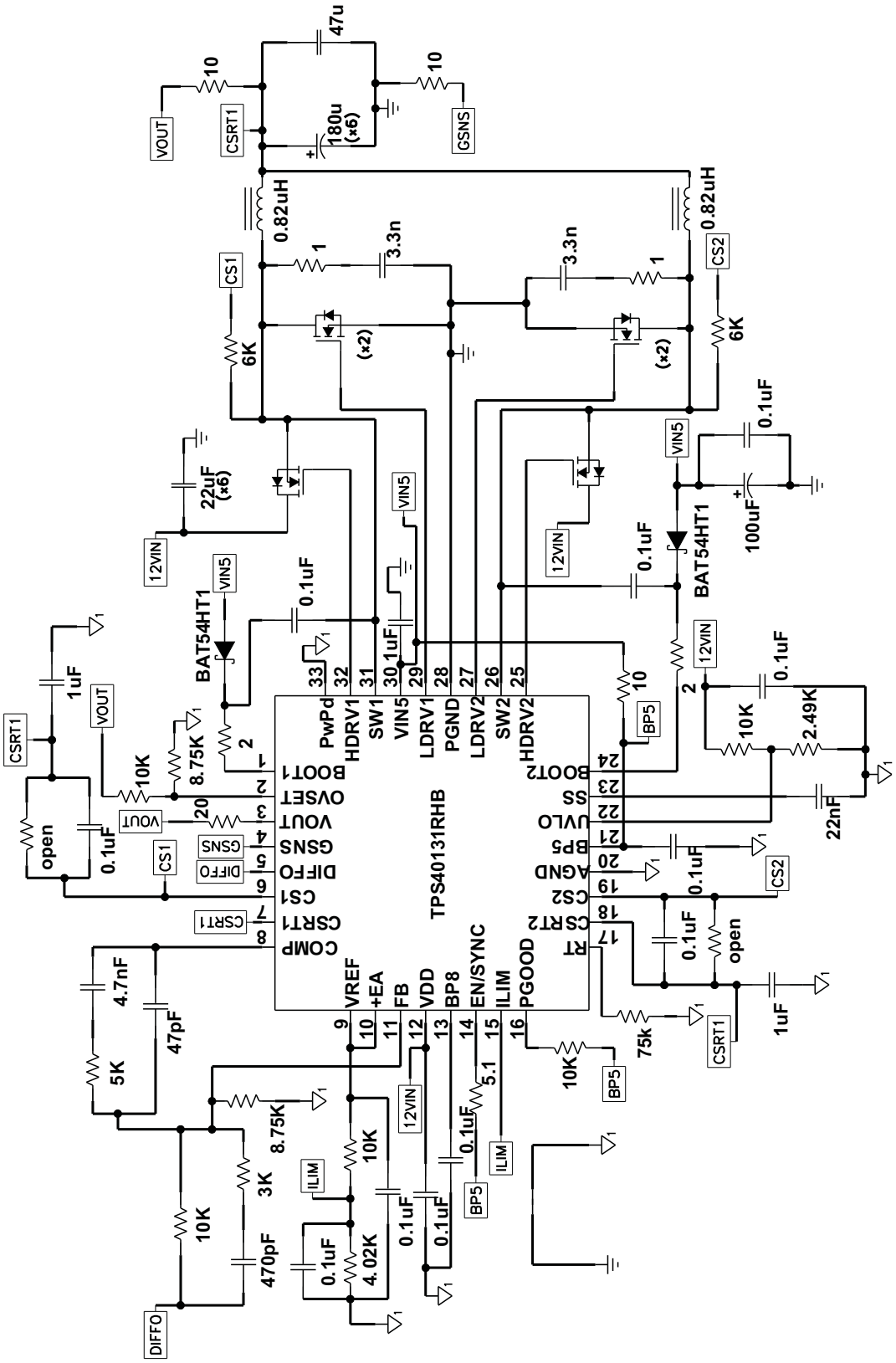


Figure 10. Converting from 12 V to 1.5 V Output for I_{OUT} = 40 A

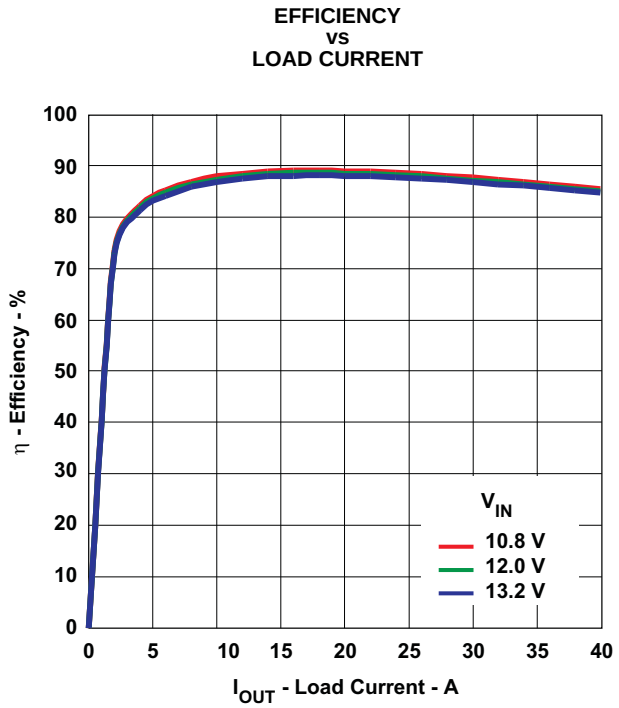


Figure 11. Efficiency vs. Load

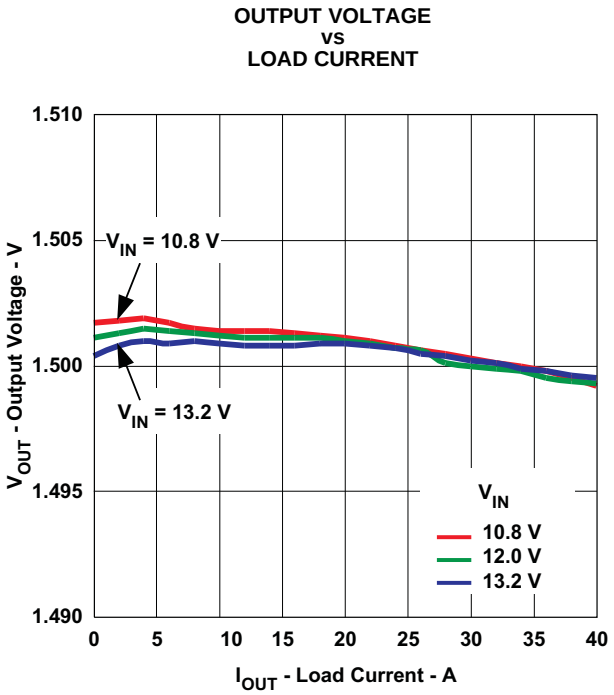


Figure 12. Load Regulation

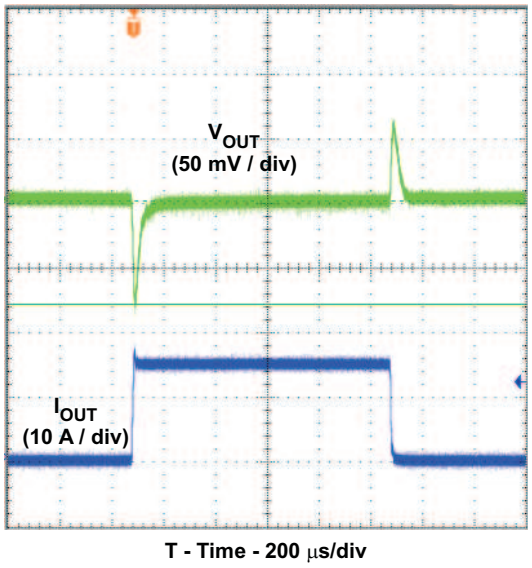


Figure 13. 0 A to 15 A Load Step

12 V to 5 V Converter Application

The following schematic shows an application that converts 12 V to 5 V. The 5-V output is used to power up the device after start up.

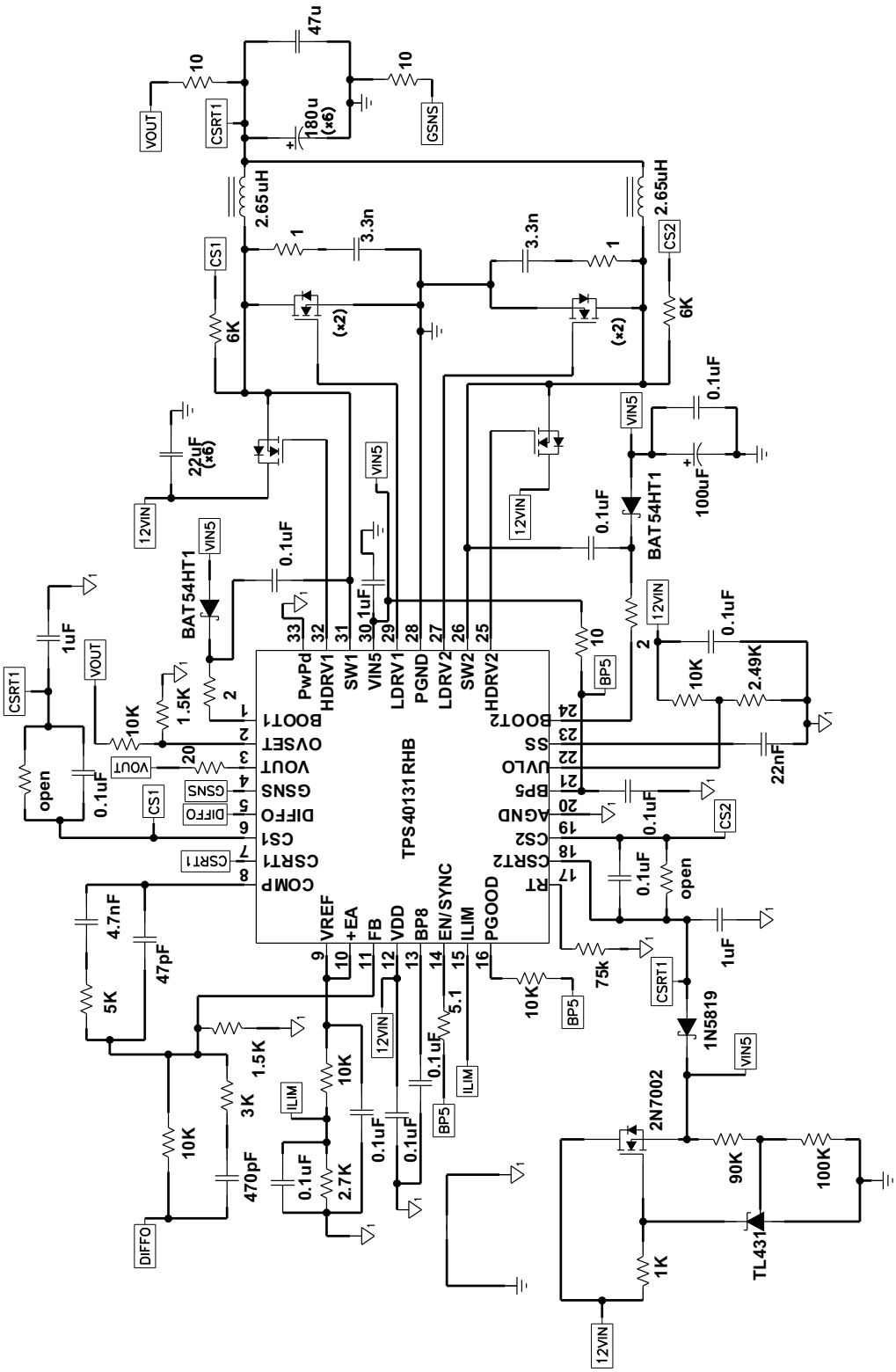


Figure 14. Converting from 12 V to 5 V Output for I_{OUT} = 20 A

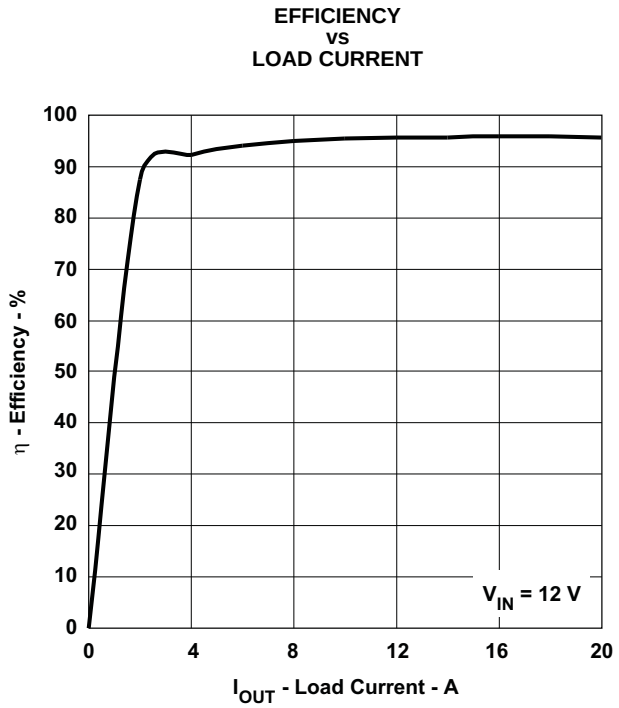


Figure 15. Efficiency vs. Load Current

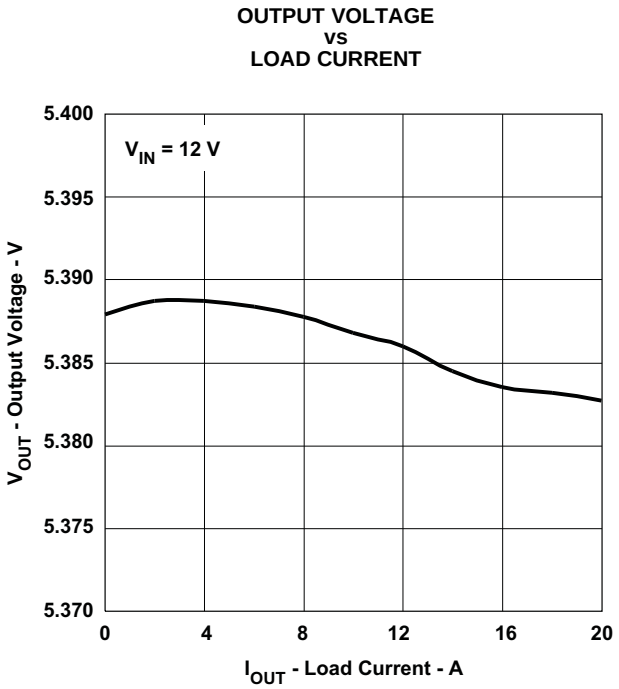


Figure 16. Load Regulation

5 V to 1.5 V Converter Application

The following schematic shows an application that converts 5 V to 1.5 V.

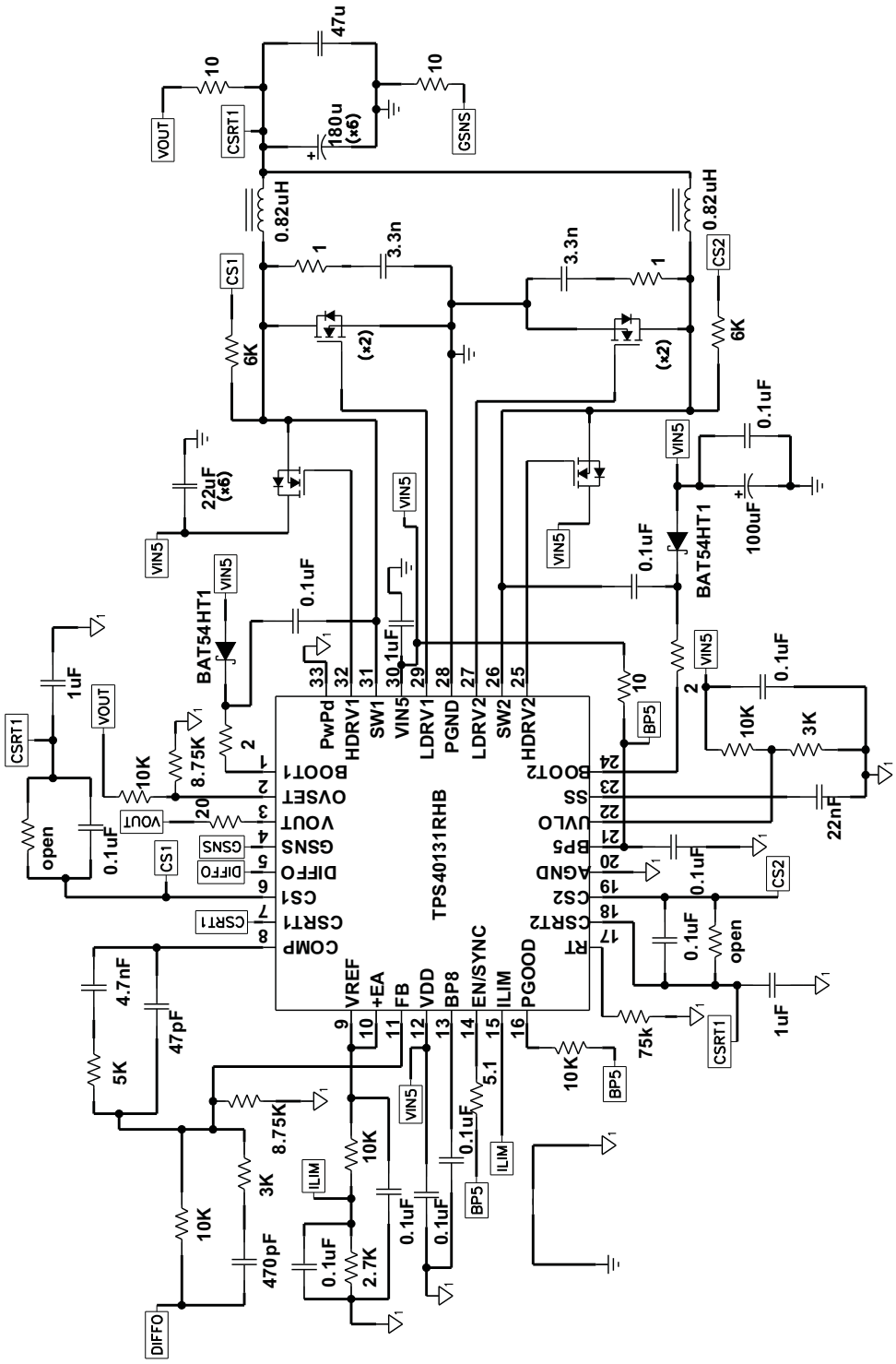


Figure 17. Converting from 5 V to 1.5 V Output for I_{OUT} = 30 A

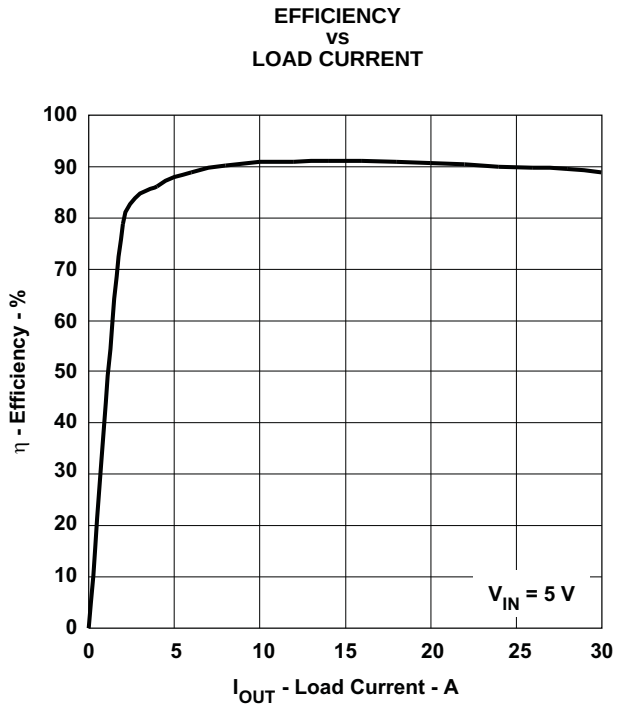


Figure 18. Efficiency vs. Load Current

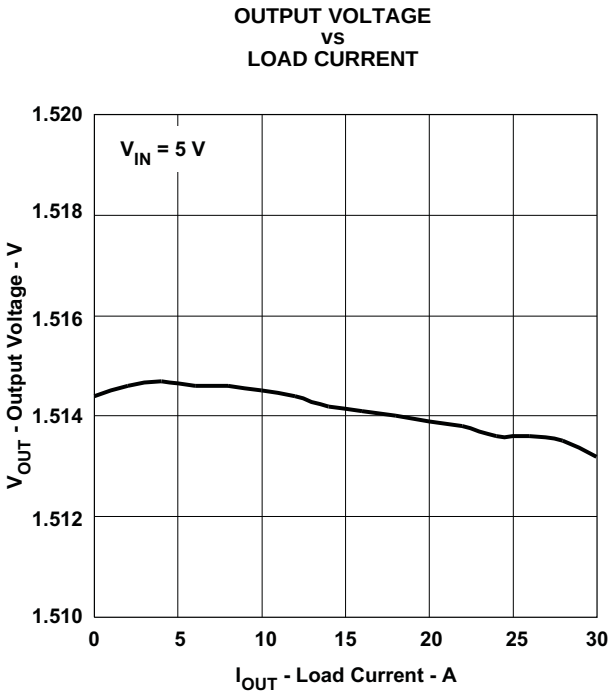


Figure 19. Load Regulation

Table 2. Definitions

SYMBOL	DESCRIPTION
$V_{IN(min)}$	Minimum Operating Input Voltage
$V_{IN(max)}$	Maximum Operating Input Voltage
V_{OUT}	Output Voltage
I_{RIPPLE}	Inductor Peak-Peak Ripple Current
$I_{TRAN(max)}$	Maximum Load Transient
V_{UNDER}	Output Voltage Undershot
V_{OVER}	Output Voltage Overshot
$V_{RIPPLE(totOUT)}$	Total Output Ripple
$V_{RIPPLE(Cout)}$	Output Voltage Ripple Due to Output Capacitance
$V_{RIPPLE(Cin)}$	Input Voltage Ripple Due to Input Capacitance
$V_{RIPPLE(CinESR)}$	Input Voltage Ripple Due to the ESR of Input Capacitance
$P_{SW(cond)}$	High-Side MOSFET Conduction Loss
$I_{SW(rms)}$	RMS Current in the High-Side MOSFET
$R_{DS(on)(sw)}$	"ON" Drain-Source Resistance of the High-Side MOSFET
$P_{SW(sw)}$	High-Side MOSFET Switching Loss
I_{PK}	Peak Current Through the High-Side MOSFET
R_{DRV}	Driver Resistance of the High-Side MOSFET
$Q_{gd(SW)}$	Gate to Drain Charge of the High-Side MOSFET
$Q_{gs(SW)}$	Gate to Source Charge of the High-Side MOSFET
VqSW	Gate Drive Voltage of the High-Side MOSFET
$P_{SW(gate)}$	Gate Drive Loss of the High-Side MOSFET
$Q_{g(SW)}$	Gate Charge of the High-Side MOSFET
$P_{SW(tot)}$	Total Losses of the High-Side MOSFET
$P_{SR(cond)}$	Low-Side MOSFET Conduction Loss
I_{SRrms}	RMS Current in the Low-Side MOSFET
$R_{DS(on)(sr)}$	"ON" Drain-Source Resistance of the Low-Side MOSFET
$P_{SR(gate)}$	Gate Drive Loss of the Low-Side MOSFET
Q_{gSR}	Gate Charge of the Low-Side MOSFET
V_{qSW}	Gate Drive Voltage of the Low-Side MOSFET
P_{DIODE}	Power Loss in the Diode
t_D	Dead Time Between the Conduction of High and Low-Side MOSFET
V_F	Forward Voltage Drop of the Body Diode of the Low-Side MOSFET
$P_{SR(tot)}$	Total Losses of the Low-Side MOSFET
DCR	Inductor DC Resistance
A_C	The Gain of the Current Sensing Amplifier, typically it is 13
R_{OUT}	Output Load Resistance
V_{RAMP}	Ramp Amplitude, typically it is 0.5V
T	Switching Period
$G_{VC(s)}$	Control to Output Transfer Function
$G_{C(s)}$	Compensator Transfer Function
$T_{V(s)}$	Loop Gain Transfer Function
A_{CM}	Gain of the Compensator
f_{P1}, f_{P2}	Pole Frequency of the Compensator
f_{Z1}, f_{Z2}	Zero Frequency of the Compensator

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS40131RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40131RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40131RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40131RHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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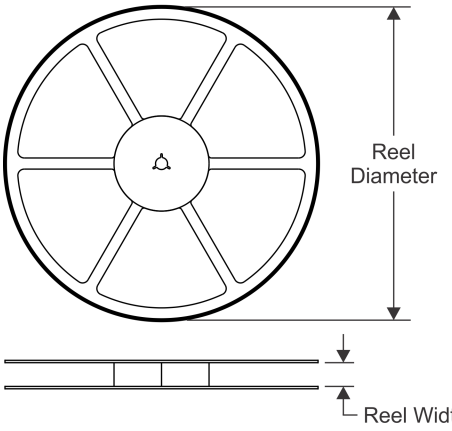
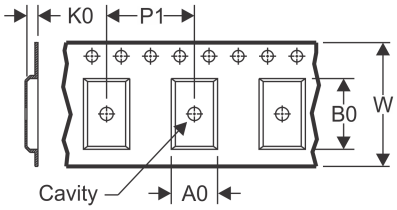
REEL DIMENSIONS

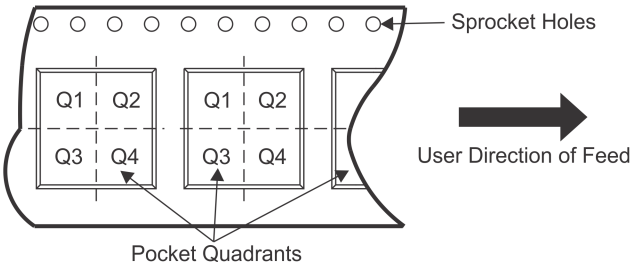


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

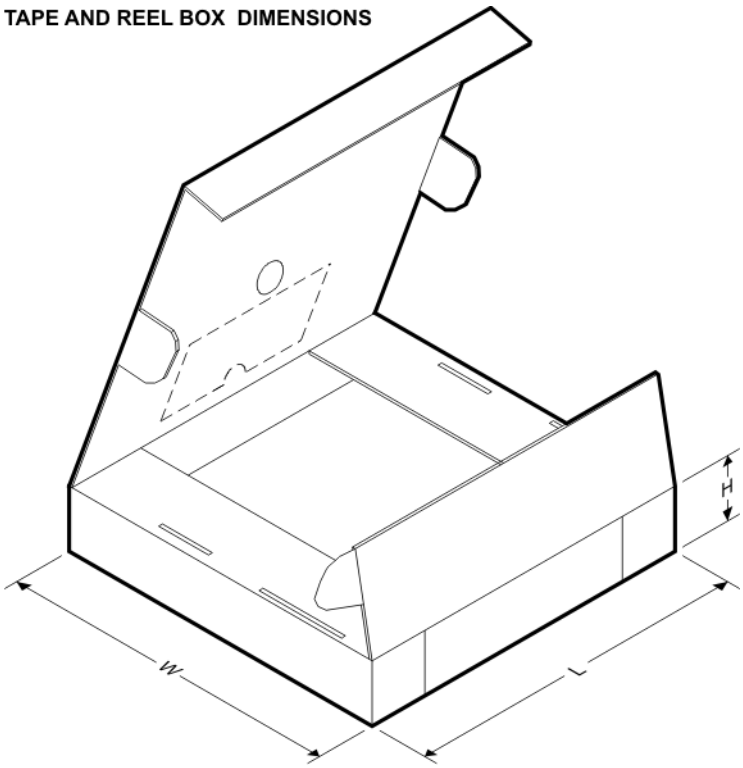
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40131RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS40131RHBT	QFN	RHB	32	250	180.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
TPS40131RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

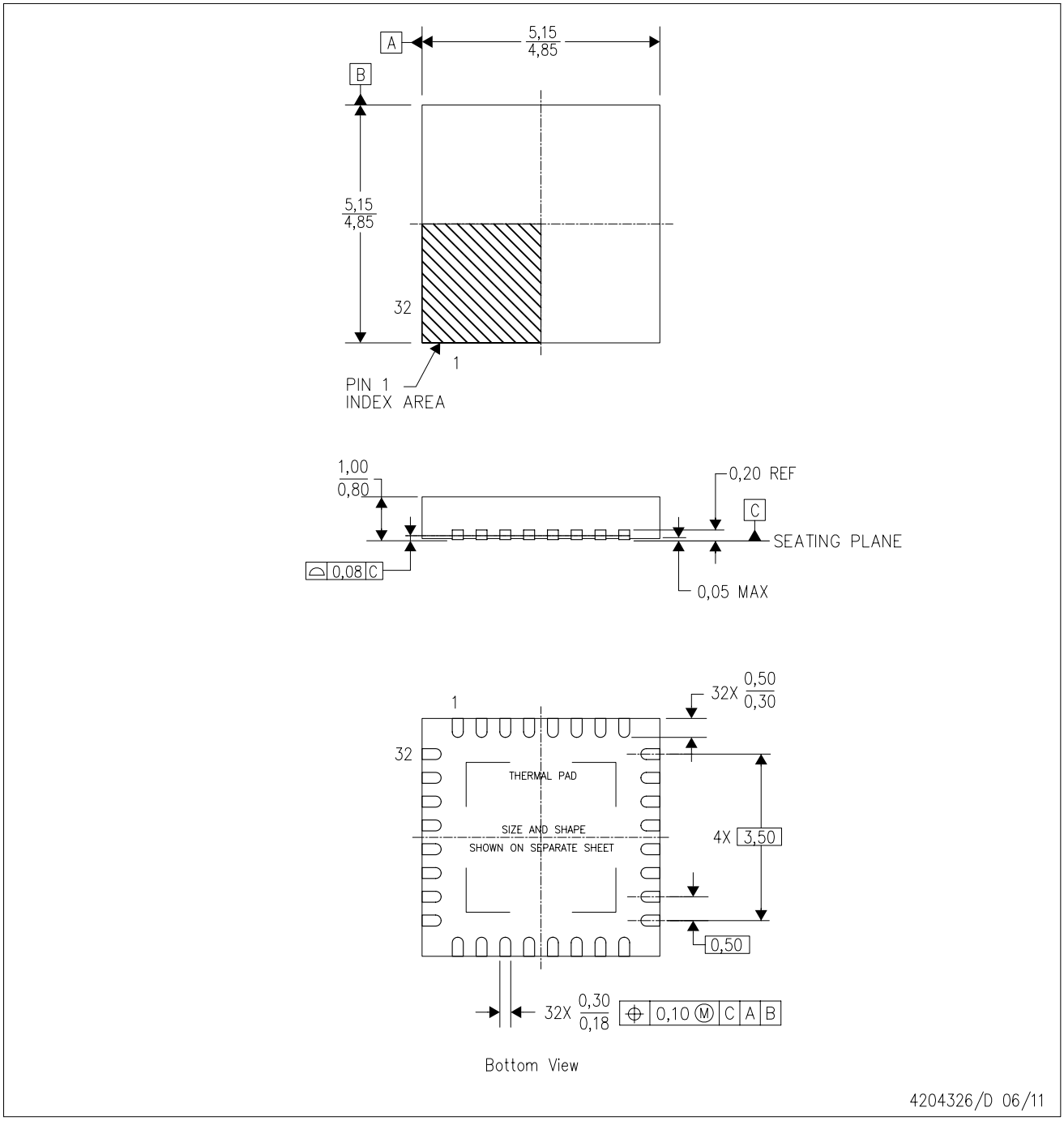
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40131RHBR	QFN	RHB	32	3000	367.0	367.0	35.0
TPS40131RHBT	QFN	RHB	32	250	195.0	200.0	45.0
TPS40131RHBT	QFN	RHB	32	250	210.0	185.0	35.0

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

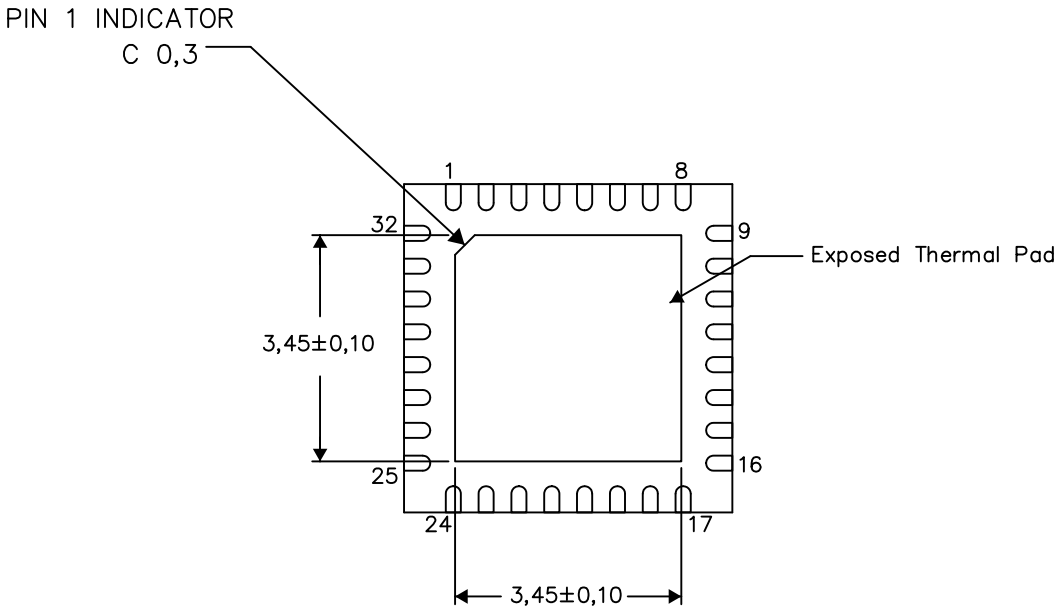
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



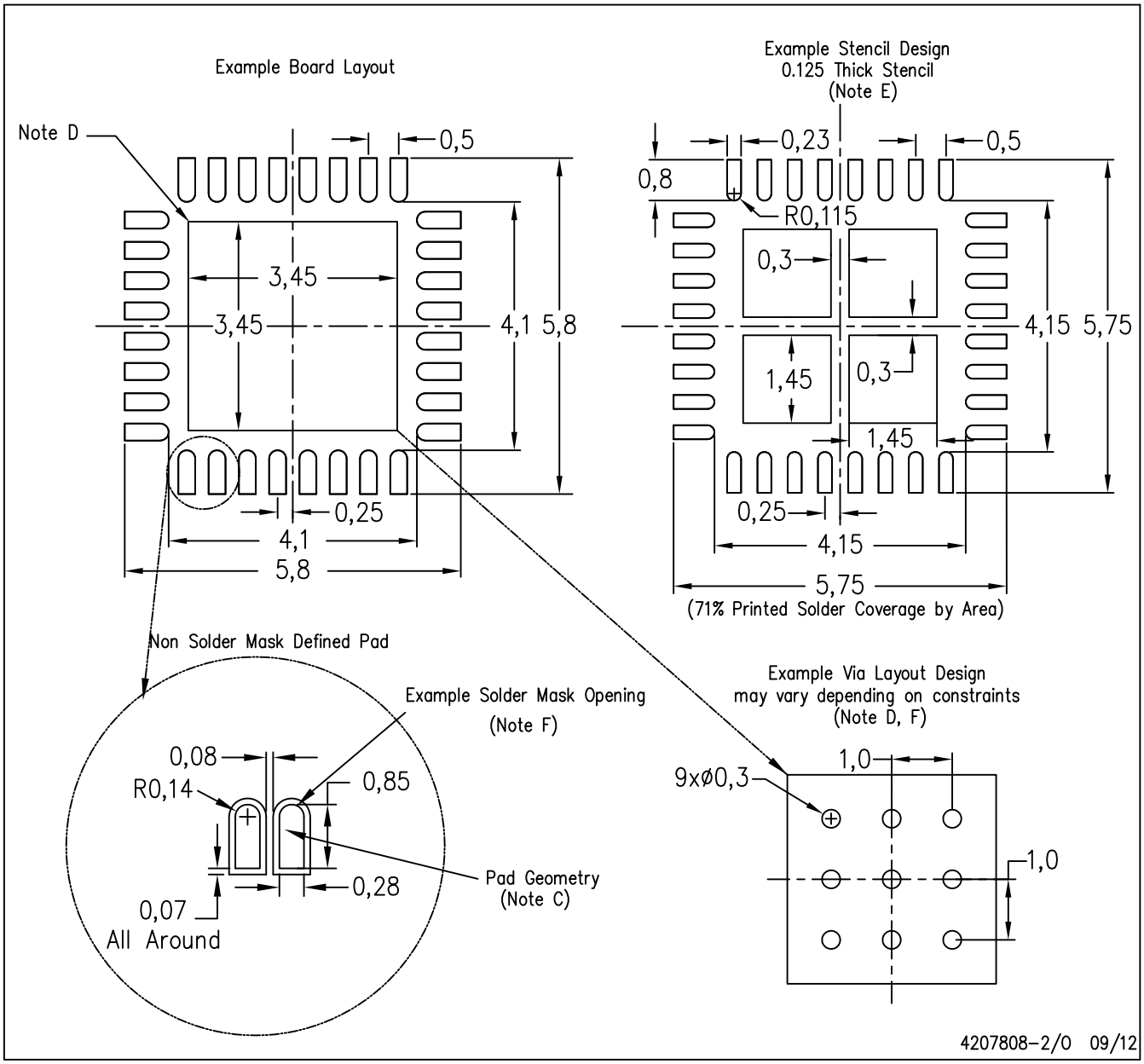
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/W 09/12

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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