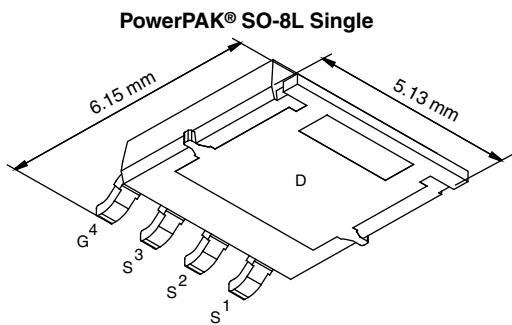


## N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY			
<b>V<sub>DS</sub> (V)</b>	<b>R<sub>DS(on)</sub> (Ω) Max.</b>	<b>I<sub>D</sub> (A)<sup>a</sup></b>	<b>Q<sub>g</sub> (Typ.)</b>
100	0.0091 at V <sub>GS</sub> = 10 V	58.8	
	0.0100 at V <sub>GS</sub> = 7.5 V	54.6	28.5 nC



**Ordering Information:**  
SiJ470DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

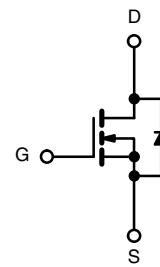
### FEATURES

- ThunderFET® Technology Optimizes Balance of R<sub>DS(on)</sub>, Q<sub>g</sub>, Q<sub>sw</sub> and Q<sub>oss</sub>
- 100 % R<sub>g</sub> and UIS Tested
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



### APPLICATIONS

- Primary Side Switching
- Synchronous Rectification
- DC/AC Inverters
- LED Backlighting
- High Current Switching



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	100		
Gate-Source Voltage	V <sub>GS</sub>	± 20	V	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C	I <sub>D</sub>	58.8	
	T <sub>C</sub> = 70 °C		47	
	T <sub>A</sub> = 25 °C		17.4 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		13.9 <sup>b, c</sup>	
Pulsed Drain Current (t = 100 µs)	I <sub>DM</sub>	150		A
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	I <sub>S</sub>	51.6	
	T <sub>A</sub> = 25 °C		4.5 <sup>b, c</sup>	
Single Pulse Avalanche Current	I <sub>AS</sub>	40		
Single Pulse Avalanche Energy	E <sub>AS</sub>	80	mJ	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	56.8	W
	T <sub>C</sub> = 70 °C		36.3	
	T <sub>A</sub> = 25 °C		5 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		3.2 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	R <sub>thJA</sub>	20	25	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	1.8	2.2	

#### Notes

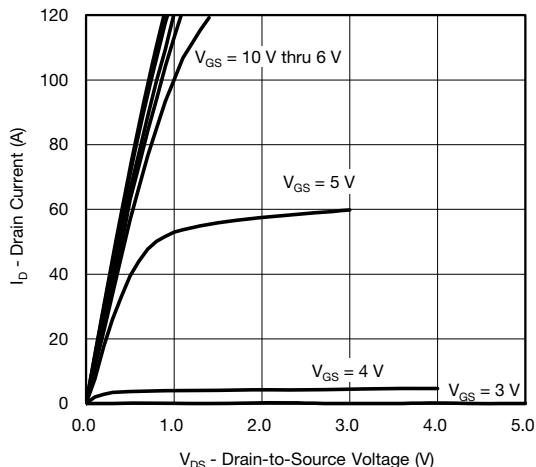
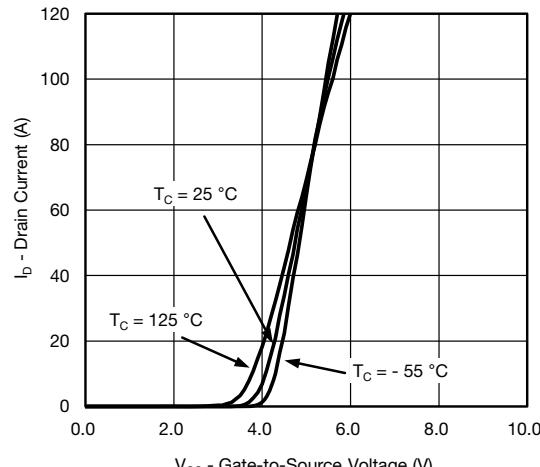
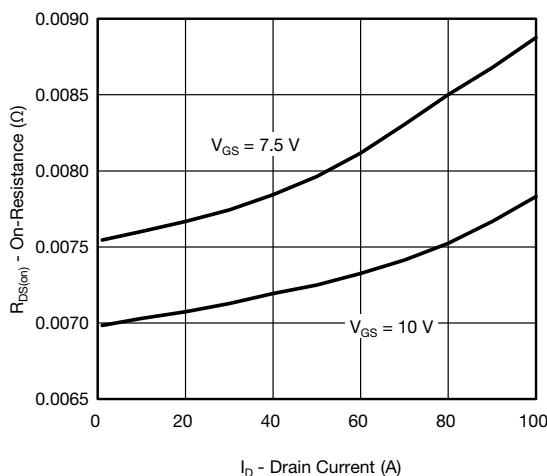
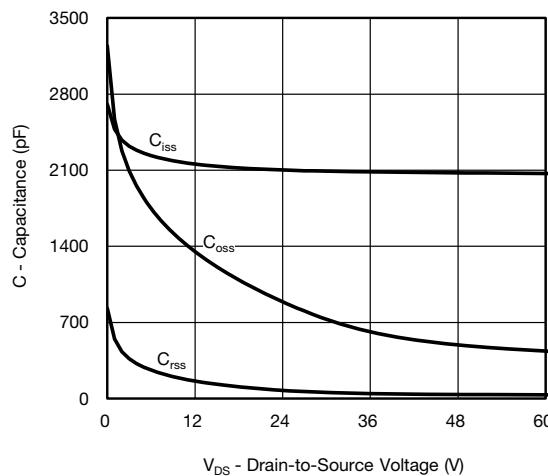
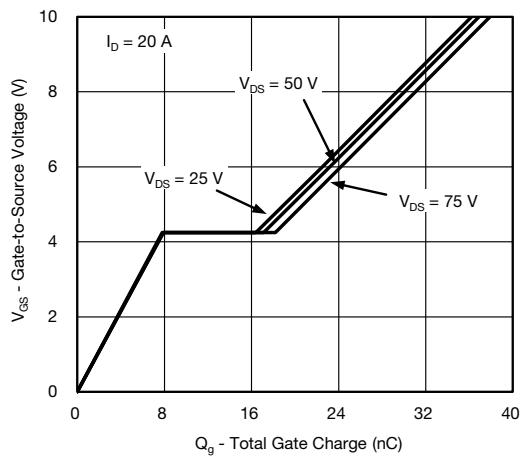
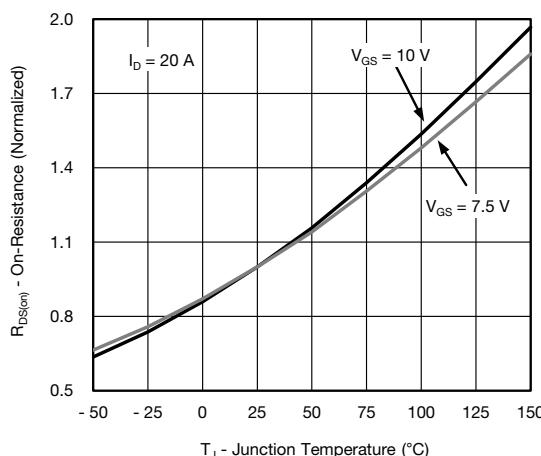
- a. T<sub>C</sub> = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 65 °C/W.

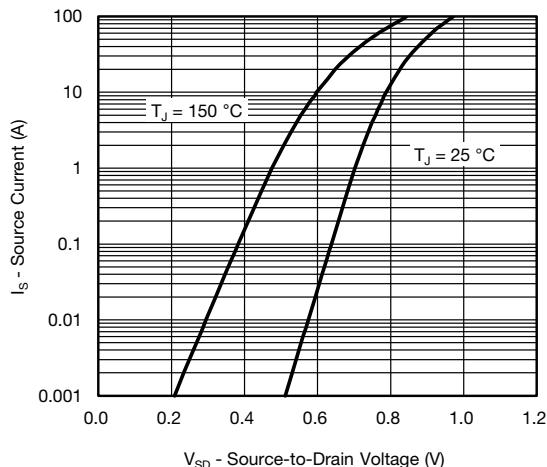
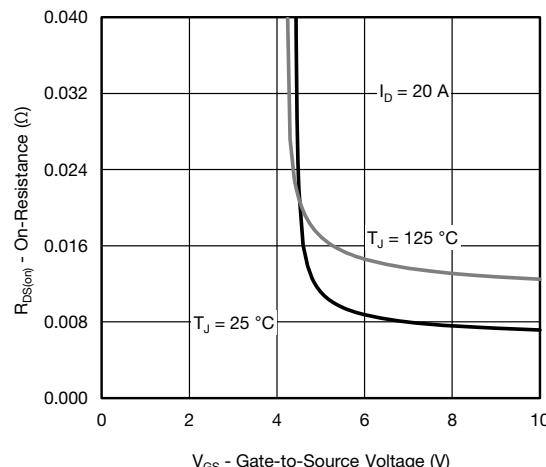
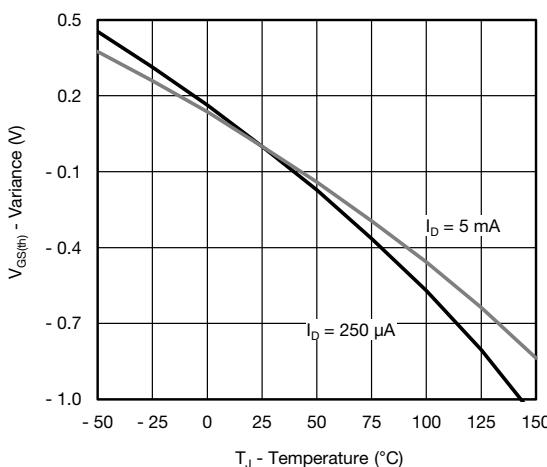
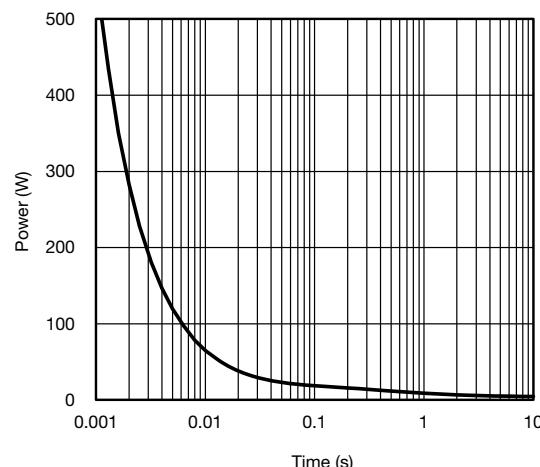
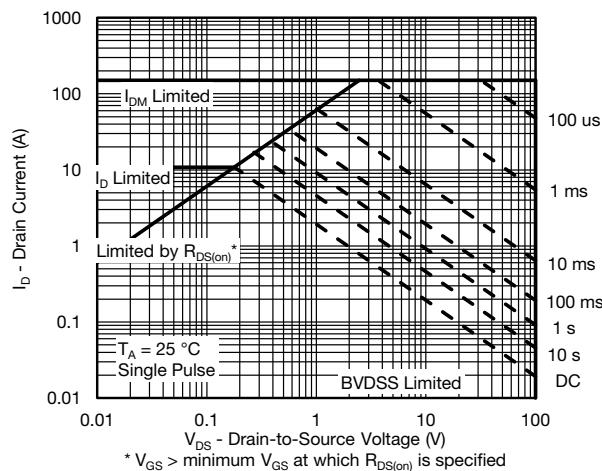
<b>SPECIFICATIONS</b> ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$	100	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$	-	63	-	mV/°C
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$		-	-7.2	-	
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$	2.3	-	3.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}$ , $V_{GS} = \pm 20 \text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100 \text{ V}$ , $V_{GS} = 0 \text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 55^\circ\text{C}$	-	-	10	
On-State Drain Current <sup>a</sup>	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$ , $V_{GS} = 10 \text{ V}$	30	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$ , $I_D = 20 \text{ A}$	-	0.0076	0.0091	$\Omega$
		$V_{GS} = 7.5 \text{ V}$ , $I_D = 15 \text{ A}$	-	0.0083	0.0100	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10 \text{ V}$ , $I_D = 20 \text{ A}$	-	60	-	S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 50 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$	-	2050	-	pF
Output Capacitance	$C_{oss}$		-	470	-	
Reverse Transfer Capacitance	$C_{rss}$		-	40	-	
Total Gate Charge	$Q_g$	$V_{DS} = 50 \text{ V}$ , $V_{GS} = 10 \text{ V}$ , $I_D = 20 \text{ A}$	-	36.9	56	nC
			-	28.5	43	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 50 \text{ V}$ , $V_{GS} = 7.5 \text{ V}$ , $I_D = 20 \text{ A}$	-	7.9	-	
Gate-Drain Charge	$Q_{gd}$		-	9.2	-	
Output Charge	$Q_{oss}$	$V_{DS} = 50 \text{ V}$ , $V_{GS} = 0 \text{ V}$	-	52	80	
Gate Resistance	$R_g$	$f = 1 \text{ MHz}$	0.5	1.35	2.2	$\Omega$
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 50 \text{ V}$ , $R_L = 2.5 \Omega$ $I_D \approx 20 \text{ A}$ , $V_{GEN} = 10 \text{ V}$ , $R_g = 1 \Omega$	-	12	24	ns
Rise Time	$t_r$		-	8	16	
Turn-Off Delay Time	$t_{d(\text{off})}$		-	22	24	
Fall Time	$t_f$		-	7	14	
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 50 \text{ V}$ , $R_L = 2.5 \Omega$ $I_D \approx 20 \text{ A}$ , $V_{GEN} = 7.5 \text{ V}$ , $R_g = 1 \Omega$	-	13	26	
Rise Time	$t_r$		-	12	24	
Turn-Off Delay Time	$t_{d(\text{off})}$		-	22	44	
Fall Time	$t_f$		-	8	16	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	-	-	51.6	A
Pulse Diode Forward Current ( $t = 100 \mu\text{s}$ )	$I_{SM}$		-	-	150	
Body Diode Voltage	$V_{SD}$	$I_S = 5 \text{ A}$	-	0.76	1.1	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10 \text{ A}$ , $dl/dt = 100 \text{ A}/\mu\text{s}$ , $T_J = 25^\circ\text{C}$	-	44	85	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	67	130	
Reverse Recovery Fall Time	$t_a$		-	27	-	ns
Reverse Recovery Rise Time	$t_b$		-	17	-	

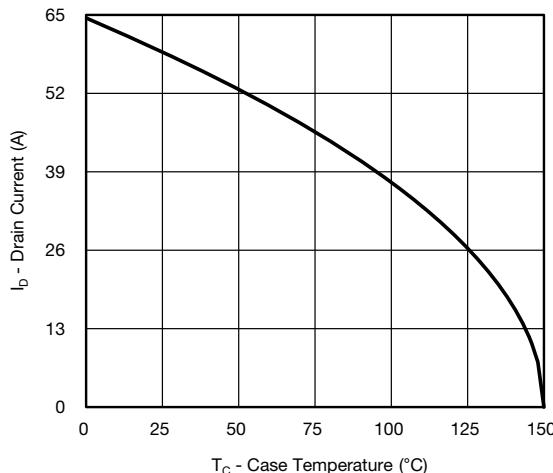
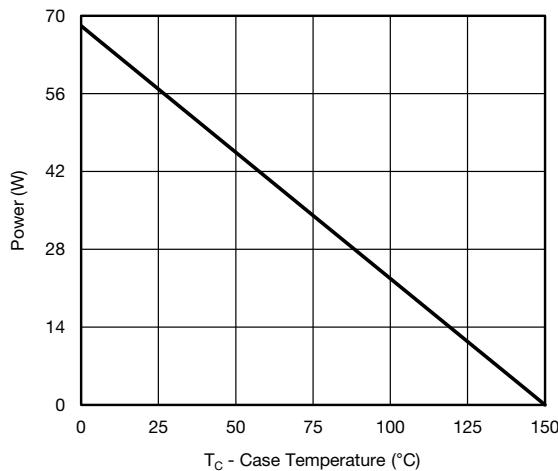
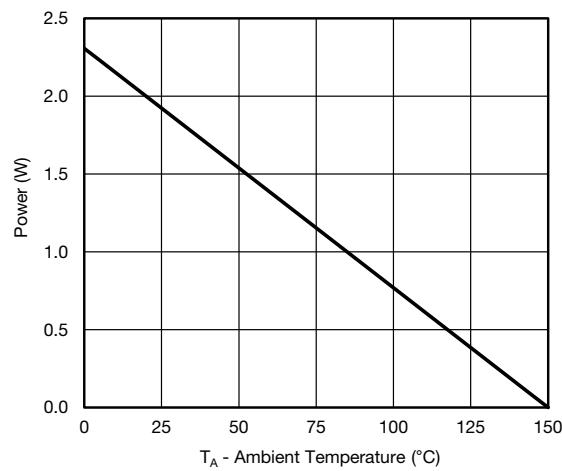
**Notes**

- a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

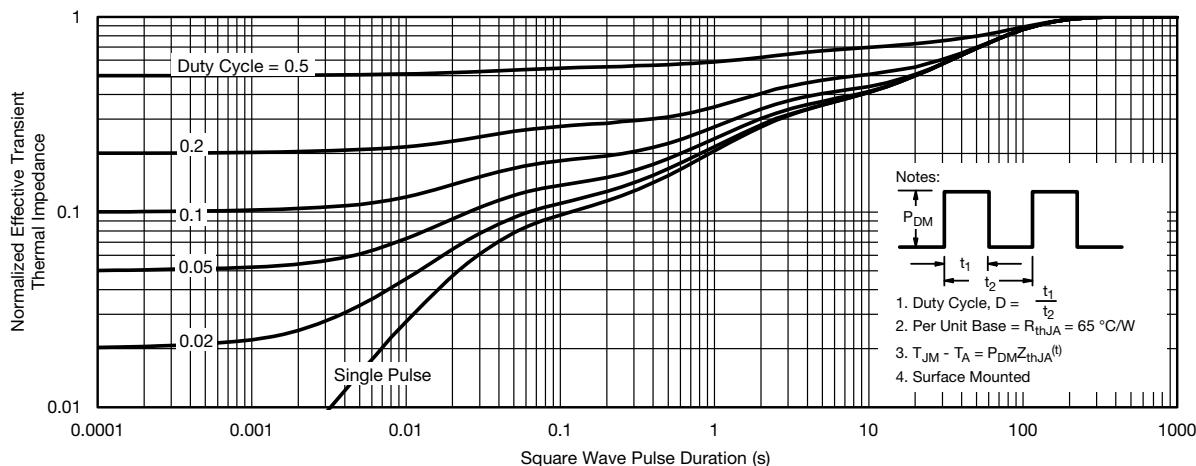
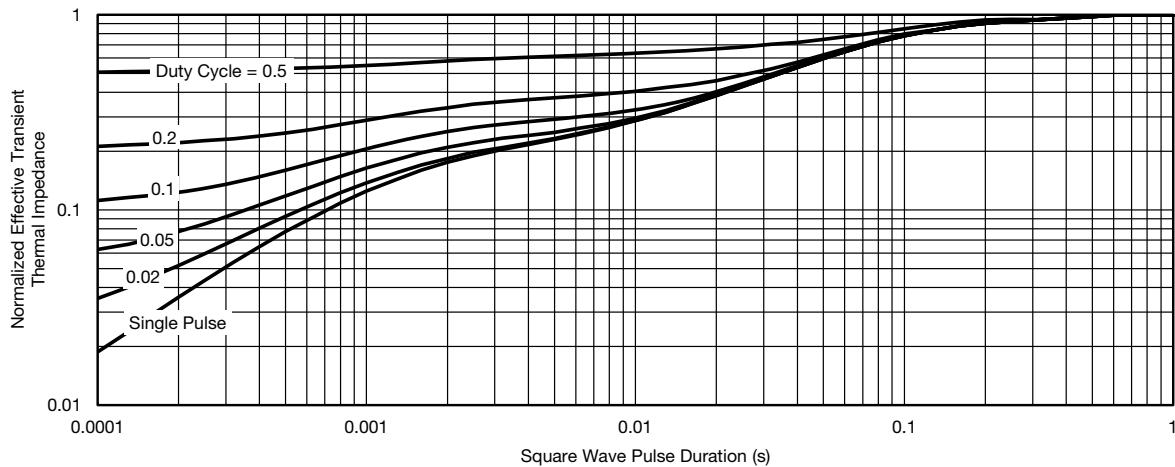
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Source-Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**Threshold Voltage**

**Single Pulse Power, Junction-to-Ambient**

**Safe Operating Area, Junction-to-Ambient**

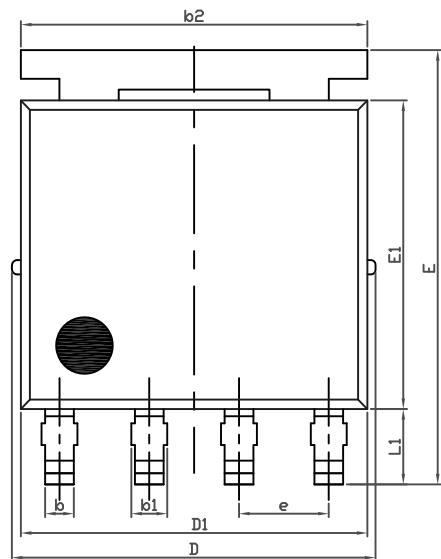
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Current Derating\***

**Power, Junction-to-Case**

**Power, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

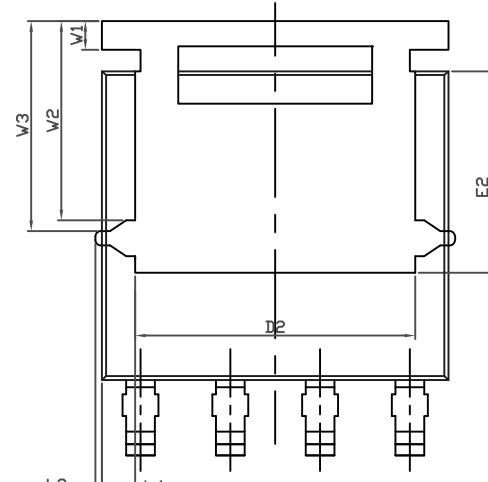
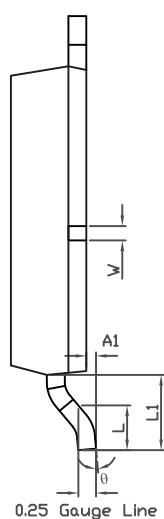
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Ambient**


Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?62883](http://www.vishay.com/ppg?62883).

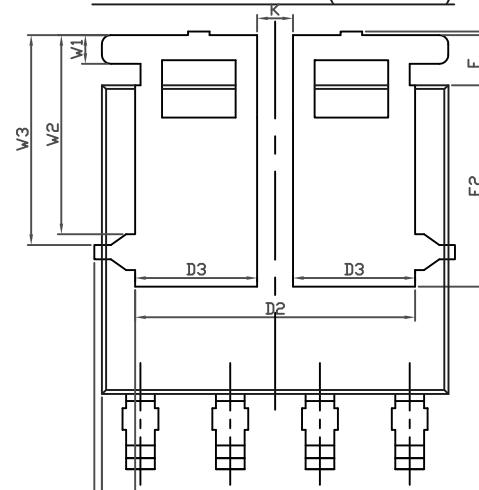
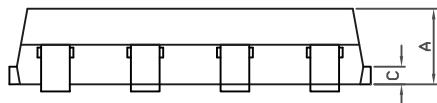
## PowerPAK® SO-8L Case Outline



TOPSIDE VIEW



BACKSIDE VIEW(SINGLE)

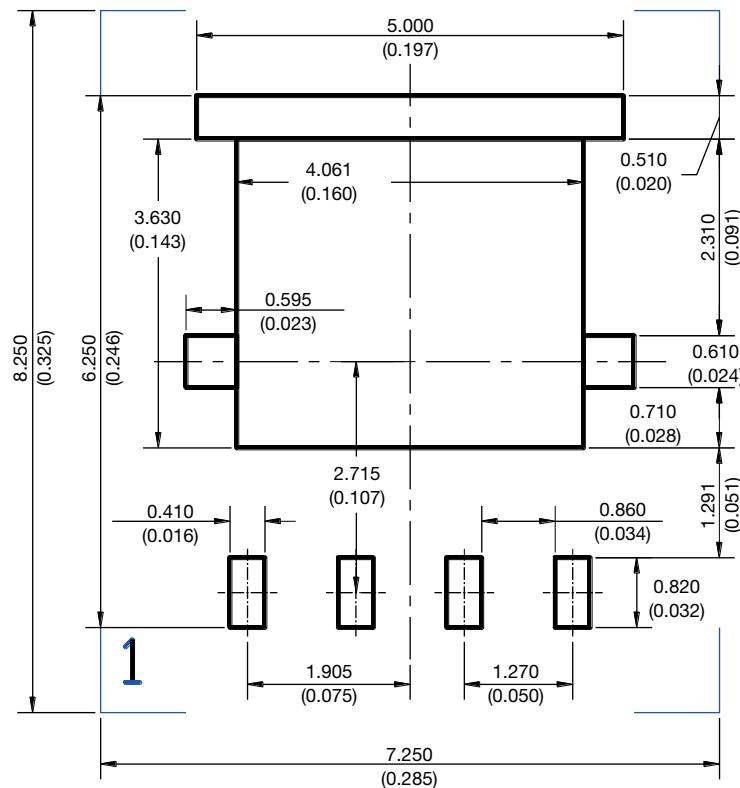


BACKSIDE VIEW(DUAL)

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2 (for AI product)	2.75	2.85	2.95	0.108	0.112	0.116
E2 (for other product)	3.18	3.28	3.38	0.125	0.129	0.133
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°
ECN: C12-0026-Rev. B, 27-Aug-12						
DWG: 5976						

### Note

- Millimeters will gover

**RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE**


Recommended Minimum Pads  
Dimensions in mm (inches)

## Disclaimer

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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**

# AMEYA360

Components Supply Platform

Authorized Distribution Brand :



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