Low Voltage, 0.7 Ω, Triple SPDT Analog Switch

DESCRIPTION

The DG2753 is a low voltage, low on-resistance, triple single-pole/double-throw (SPDT) monolithic CMOS analog switch. The device is designed for operation from 1.65 V to 4.3 V single supply. The device is 1.8 V logic compatible within the full operation voltage range to interface with low voltage DSP or MCU control logic. These traits make it ideal for one cell Li-ion battery direct power in portable applications.

The DG2753 fully guarantees operation when V+ is as low as 1.8 V. When powered from a 3 V power supply, it has a 0.9 Ω on-resistance, with 0.1 Ω R_{ON} matching between channels, and 0.2 Ω (Max) R_{ON} flatness.

Each switch conducts signals across power rails equally well in both directions when on, and blocks up to the power supply level when off. It offers 30 nS T_{on} and 10 nS T_{off}. Break-before-make is guaranteed.

The DG2753 is built on Vishay Siliconix's low voltage process. An epitaxial layer prevents latchup.

It is available in QFN16 3 x 3 mm and TSSOP16 packages. As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device terminations. For analog switching products manufactured in QFN packages, the lead (Pb)-free "-E4" suffix is being used as a designator for nickel-palladium-gold. The TSSOP-16 package is offered in lead (Pb)-free with 100 % matte Tin terminations. The "-E3" suffix is the designator. Both the 100 % matte Tin and nickel-palladium gold device terminations meet all JEDEC standards for reflow and MSL ratings.

FEATURES

- Low Voltage Operation (1.65 to 4.3 V)
- Low On-Resistance - r_{ON}: 0.9 Ω at 2.7 V
- Fast Switching: T_{ON} = 30 ns
- T_{OFF} = 10 ns
- QFN-16 (3 x 3) Package
- Latch-Up Current > 300 mA (JESD78)

BENEFITS

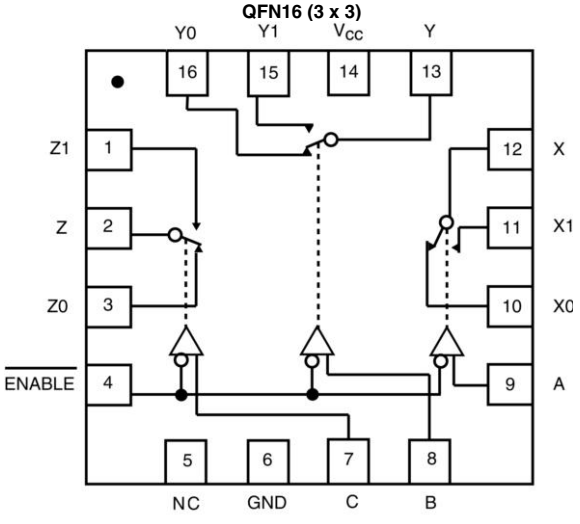
- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- TTL/1.8 V Logic Compatible

APPLICATIONS

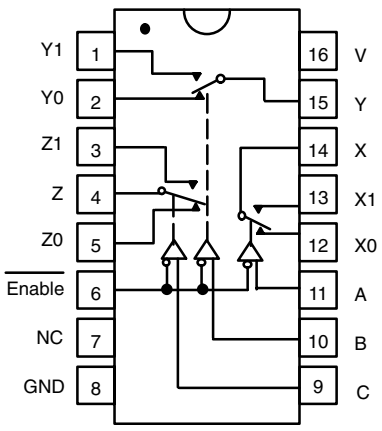
- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

QFN16 (3 x 3)



TSSOP16



ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
- 40 to 85 °C	TSSOP-16	DG2753DQ-T1-E3
	16-Pin QFN (3 mm x 3 mm) Variation 2	DG2753DN-T1-E4

TRUTH TABLE

Enable Input	Select Inputs			ON Switches
	C	B	A	DG2753
H	X	X	X	All switches open
L	X	X	L	X - X0
L	X	X	H	X - X1
L	X	L	X	Y - Y0
L	X	H	X	Y - Y1
L	L	X	X	Z- Z0
L	H	X	X	Z - Z1

X = Do not care

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Limit	Unit
Reference to GND	V+	- 0.3 to 5.0	V
	IN, COM, NC, NO[a]	- 0.3 to (V+ + 0.3)	
Current (Any terminal except NO, NC or COM)		30	mA
Continuous Current (NO, NC, or COM)		± 300	
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 500	
Storage Temperature (D Suffix)		- 65 to 150	°C
Package Solder Reflow Conditions[d]	16-Pin QFN (3 x 3 mm)	250	
Power Dissipation (Packages)[b]	QFN-16[c]	1385	mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 17.3 mW/°C above 70 °C.
d. Manual soldering with iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+, ± 10 %, V_{IN} = 0.4 or 1.8 V[e]	Temp[a]	Limits - 40 to 85 °C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	$r_{DS(on)}$	V+ = 2.7 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 1.7 V	Room		0.9	1.3	Ω
		V+ = 2.7 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 1.7 V	Full			1.5	
		V+ = 4.2 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 2.1 V	Room		0.7	1.2	
		V+ = 4.2 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 2.1 V	Full			1.4	
r_{ON} Match	$\Delta r_{(on)}$	V+ = 2.7 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 1.7 V	Room			0.4	
		V+ = 4.3 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 2.1 V	Room			0.6	
r_{ON} Resistance Flatness	$r_{(on)\ Flatness}$	V+ = 2.7 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 1.7 V	Room			0.2	
Switch Off Leakage Current	$I_{NO(off)}$	V+ = 4.3 V, V_{NO}, V_{NC} = 4 V/0.3 V, V_{COM} = 0.3 V/4 V	Room	- 2		2	nA
			Full	- 25		25	
	$I_{COM(off)}$		Room	- 2		2	
			Full	- 25		25	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 4.3 V, V_{COM} = V_{NO}, V_{NC} = 0.3 V/4 V	Room	- 2		2	
			Full	- 10		10	

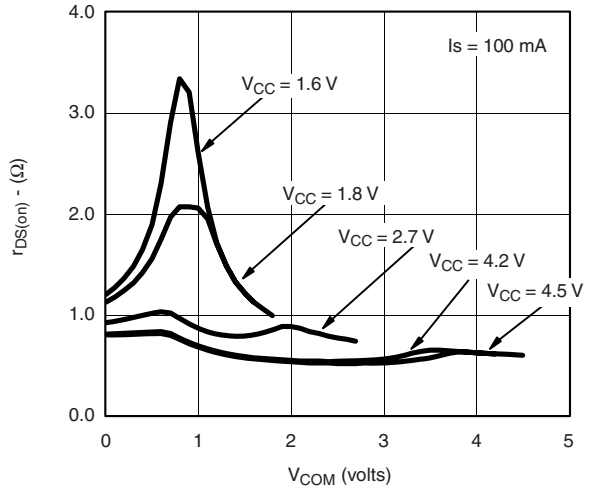
SPECIFICATIONS

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+, ± 10 %, V_{IN} = 0.4 or 1.8 V[e]	Temp[a]	Limits - 40 to 85 °C Min[b]	Typ[c]	Max[b]	Unit
Digital Control							
Input High Voltage	V_{INH}	V+ = 1.8 V	Full	1			V
		V+ = 3 V	Full	1.4			
		V+ = 4.3 V	Full	1.8			
Input Low Voltage	V_{INL}	V+ = 1.8 V	Full			0.4	
		V+ = 3 V	Full			0.5	
		V+ = 4.3 V	Full			0.5	
Input Current	I_{INL}, I_{INH}	V_{IN} = 0 V or V+	Full	- 1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V+ = 2.7 V V_{NO}, V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room		30	60	ns
			Full			65	
Turn-Off Time	t_{OFF}		Room		10	30	
			Full			40	
Break-Before-Make	t_{OPEN}	V+ = 2.7 V V_{NO}, V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Full	5	30		
Adress Transistion Time	t_{TRANS}		Full		40	80	pC
Charge Injection[d]	Q_{INJ}	V+ = 2.7 V, C_L = 1 nF, R_{GEN} = 0 Ω, f = 500 kHz V_{NC}, V_{NO} = 2 V (test at $_{COM}$ side)	Room		- 25		
Off-Isolation[d]	O_{IRR}	V+ = 2.7 V, C_L = 1 nF, R_{GEN} = 0 Ω, f = 500 kHz V_{NC}, V_{NO} = 2 V (test at $_{COM}$ side)	Room		- 90		dB
Crosstalk[d]	X_{TALK}	V+ = 2.7 V, C_L = 1 nF, R_{GEN} = 0 Ω V_{NC}, V_{NO} = 2 V (test at $_{COM}$ side)	Room		- 90		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		35		pF
	$C_{NC(off)}$		Room		35		
Channel/On Capacitance[d]	$C_{NO(on)}$		Room		80		
	$C_{NC(on)}$		Room		80		
Power Supply							
Power Supply Current	I+	V_{IN} = 0 or V+	Full			1	µA

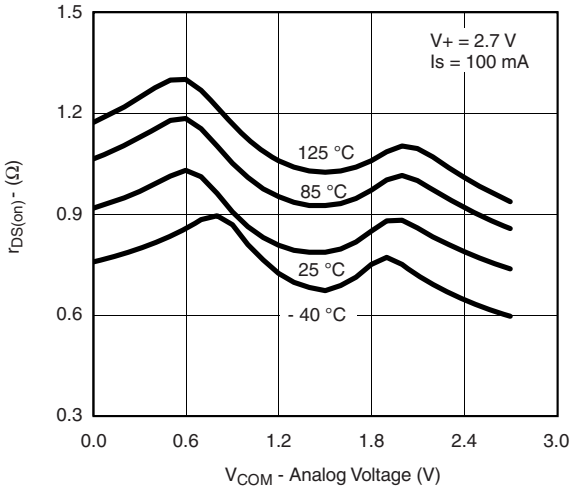
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention where by the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, not subjected to production test.
e. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

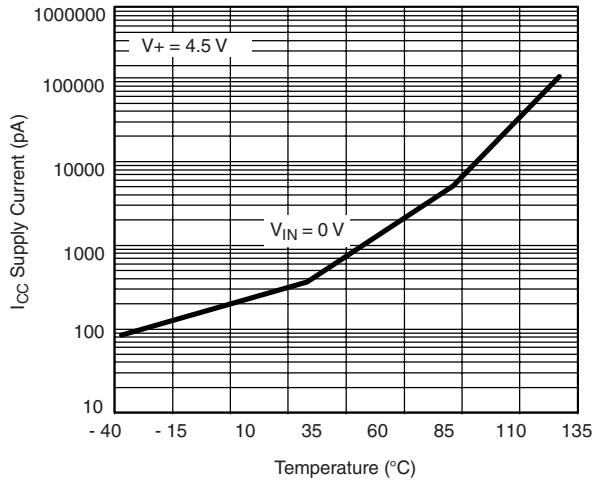
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



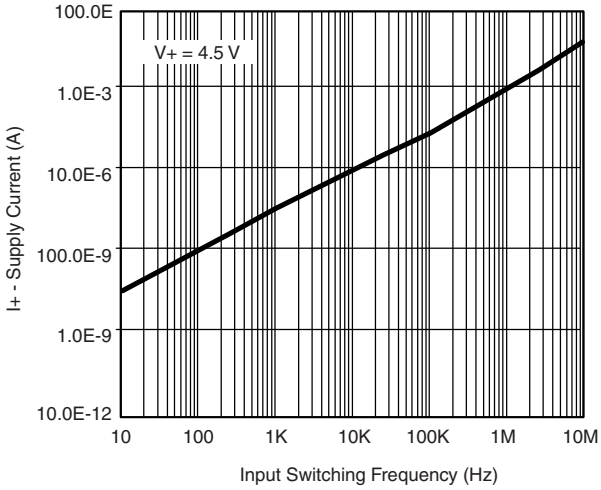
r_{ON} vs. V_{COM} and Supply Voltage



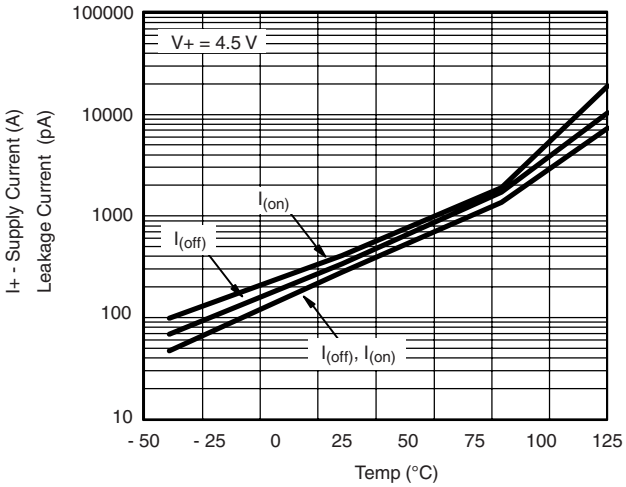
r_{ON} vs. Analog Voltage and Temperature



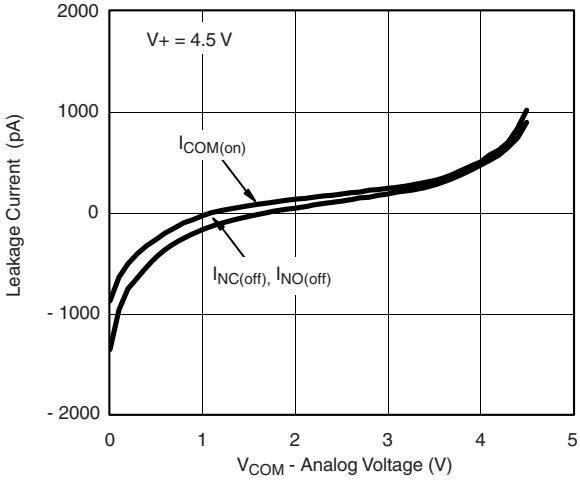
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

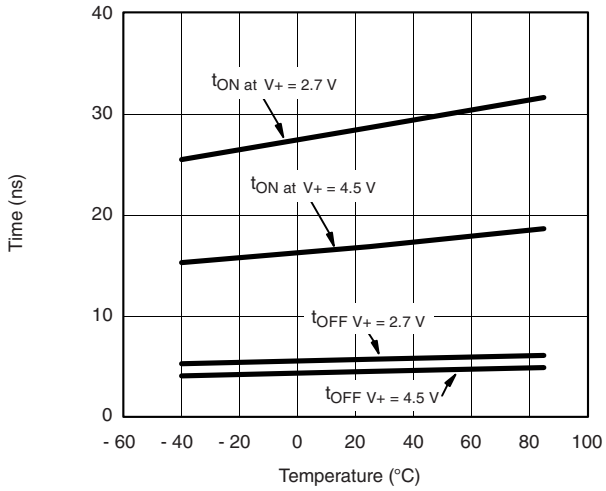


Leakage Current vs. Temperature

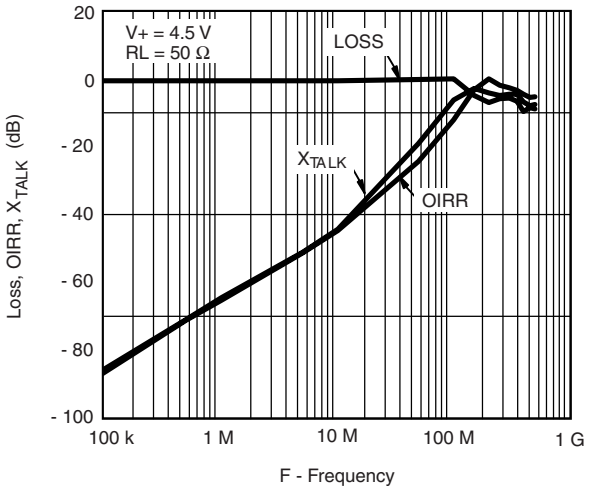


Leakage Current vs. Analog Voltage

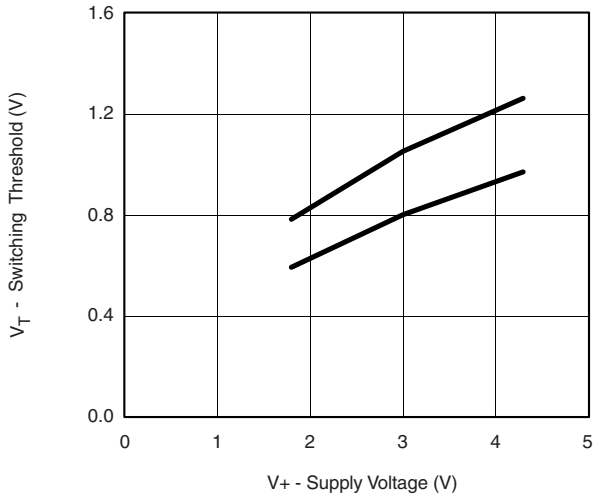
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



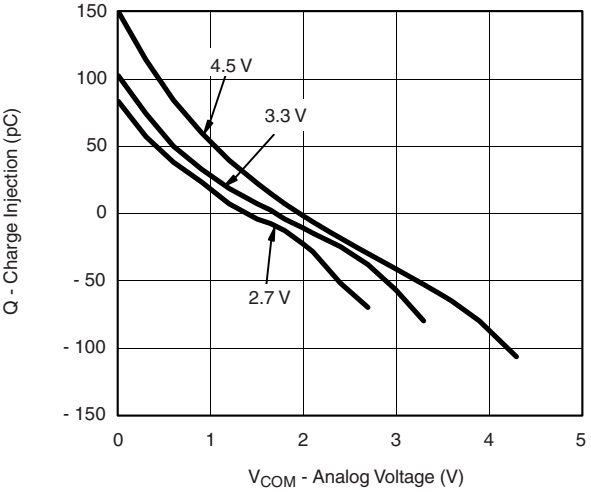
Switching Time vs Temperature



Insertion Loss, Off Isolation, Cross Talk vs. Frequency

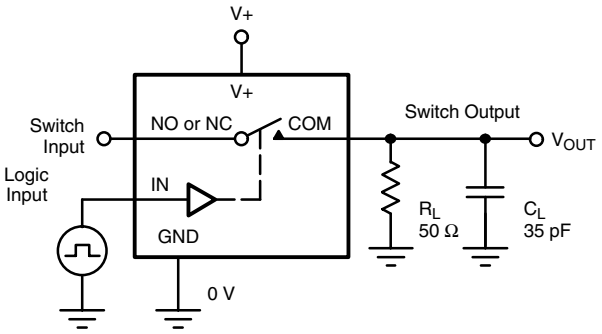


Switching Threshold vs. Supply Voltage



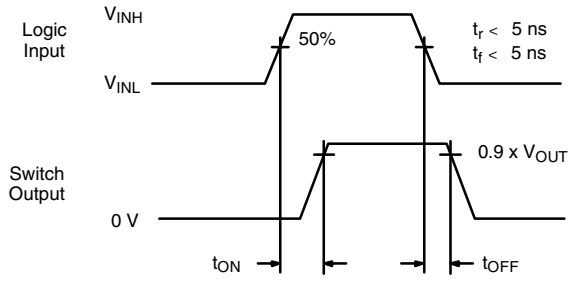
Charge Injection vs. Analog Voltage

TEST CIRCUITS



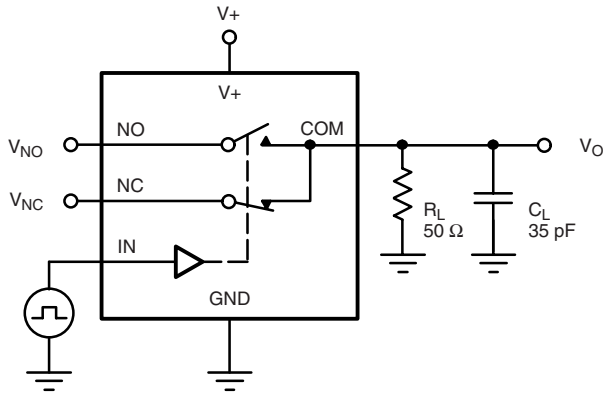
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

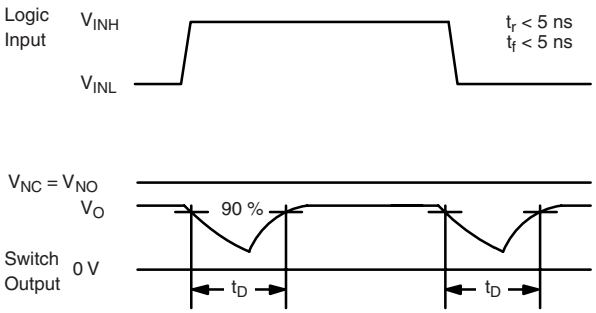
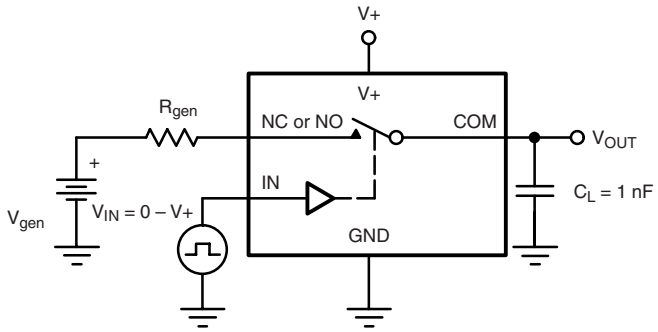
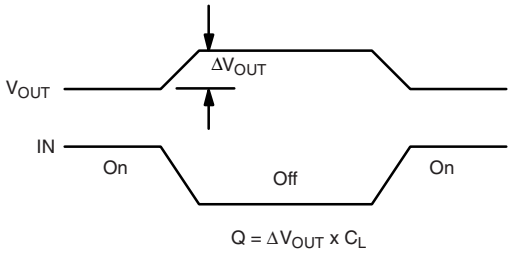


Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

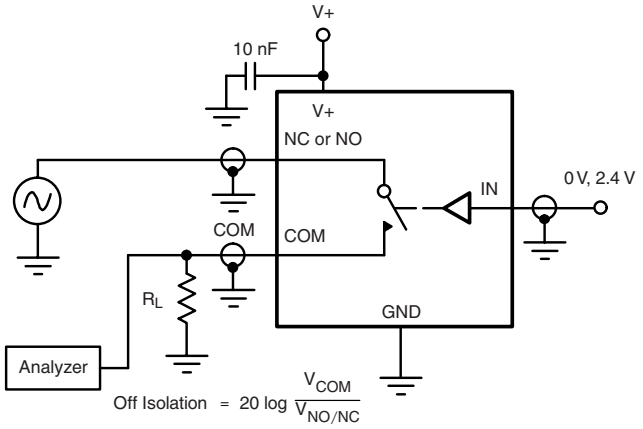


Figure 4. Off-Isolation

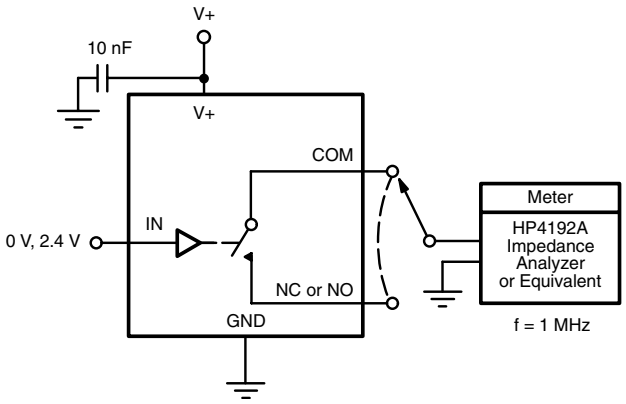


Figure 5. Channel Off/On Capacitance

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