



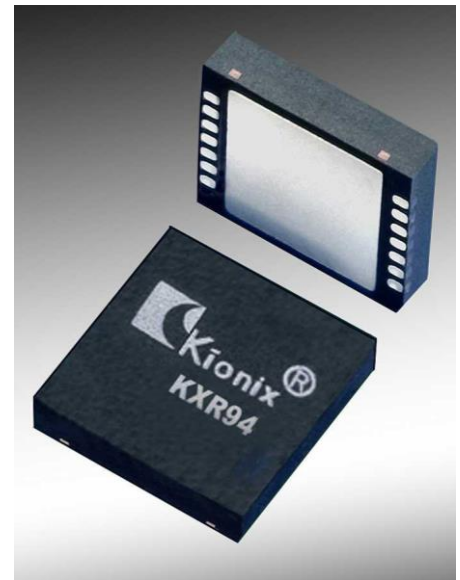
± 2g Tri-axis Accelerometer Specifications

PART NUMBER:

KXR94-7050
Rev. 3
May-2014

Product Description

The KXR94-7050 is a Tri-axis, silicon micromachined accelerometer with a full-scale output range of +/-2g (19.6 m/s/s). The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit. A separate ASIC device packaged with the sense element provides signal conditioning and self-test. The accelerometer is delivered in a 5 x 5 x 1.2 mm DFN plastic package operating from a 2.5 – 5.25V DC supply.



There are 4 factory programmable modes of operation for the KXR94:

- Mode 00** – The three outputs (X, Y, Z) are read through the **digital** SPI interface, which is also used to command Selftest and Standby Mode. The digital I/O pads are powered from a separate power pin, and will interface to 1.8V logic.
- Mode 01** – The three outputs (X, Y, Z) are provided on three **analog** output pins. The KXR94 also features an integrated **3-channel multiplexer** (X, Y, Z). The Enable pin must be **high** for normal operation and **low** for power shutdown.
- Mode 10** – The three outputs (X, Y, Z) are provided on three **analog** output pins. The KXR94 also features an integrated **4-channel multiplexer** (X, Y, Z, Aux In). The Enable pin must be **high** for normal operation and **low** for power shutdown.
- Mode 11** – The three outputs (X, Y, Z) are provided on three **analog** output pins. The KXR94 also features an integrated **4-channel multiplexer** (X, Y, Z, Aux In). The Enable pin must be **low** for normal operation and **high** for power shutdown.

The KXR94-7050 is factory programmed to be in MODE 10.

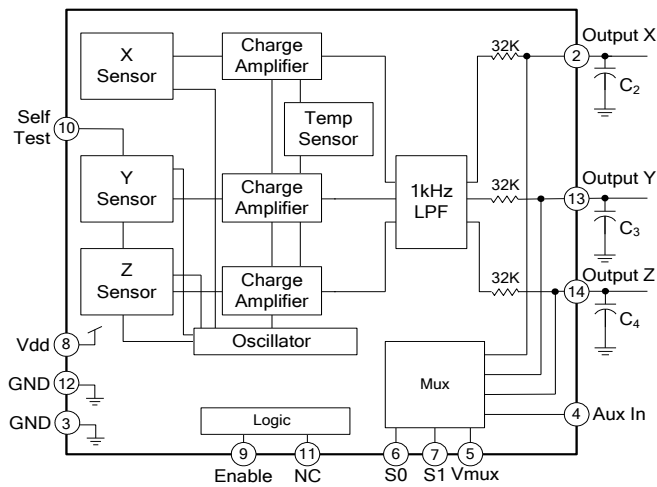


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Functional Diagram



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Product Specifications

Table 1. Mechanical

(specifications are for operation at 3.3V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		°C	-40	-	125
Zero-g Offset	!	V	1.584	1.65	1.716
Zero-g Offset Variation from RT over Temp.		mg/°C		0.2	1
Sensitivity	!	mV/g	647	660	673
Sensitivity Variation from RT over Temp.		%/°C		0.01 (xy) 0.02 (z)	0.015 0.04
Offset Ratiometric Error (Vdd = 3.3V ± 5%)		mg		4	15
Sensitivity Ratiometric Error (Vdd = 3.3V ± 5%)		%		1.25 (xy) 0.2 (z)	2.5 1
Non-Linearity		% of FS		0.2	0.5
Cross Axis Sensitivity		%		1.5	3
Self Test Output change on Activation		g	1.75 0.3	1.9 (xy) 0.5 (z)	2.1 0.6
Bandwidth (-3dB) ¹		Hz	560	700	840
Noise Density (on filter pins)		μg / √Hz	-10	40	90

! Denotes Special Characteristics: These characteristics have been identified as important to the customer.

Notes:

1. Internal 1 kHz low pass filter. Lower frequencies are user definable with external capacitors.

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Table 2. Electrical

(specifications are for operation at 3.3V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (V _{dd})	Operating	V	3.135	3.3	3.465
Current Consumption	Operating	! μA	820	950	1080
	Standby	μA		-	5
Analog Output Resistance(R _{out})		kΩ	24	32	40
Input Low Voltage		V	-	-	0.2 * V _{IO}
Input High Voltage		V	0.8 * V _{IO}	-	-
Multiplexer Response Time		μs		4.5	
Power Up Time ¹		ms		1	

! Denotes Special Characteristics: These characteristics have been identified as important to the customer.

Notes:

1. Power up time can also be determined by 5 times the RC time constant of the optional user defined low pass filter.

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Table 3. Environmental

Parameters		Units	Min	Target	Max
Supply Voltage (V _{dd})	Absolute Limits	V	-0.3	-	7.0
Maximum Operating Temperature Range		°C	-40	-	125
Storage Temperature Range		°C	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms
ESD	HBM	V	-	-	3000



Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.



This product conforms to Directive 2002/95/EC of the European Parliament and of the Council of the European Union (RoHS). Specifically, this product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are "of uniform composition throughout."



This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations available upon request or from www.kionix.com.



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Application Schematic

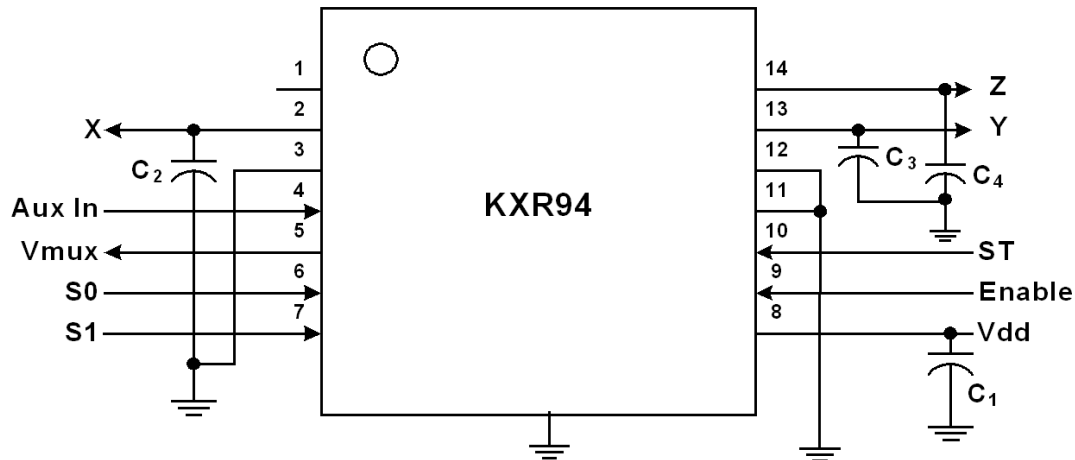


Table 4. KXR94 Pad Descriptions

Pad	Name	Description
1	NC	Not Connected Internally (can be connected to Vdd or Gnd)
2	X output	Analog output of the x-channel. Optionally, a capacitor (C ₂) placed between this pin and ground will form a low pass filter.
3	GND	Ground
4	Aux In	Auxiliary input for multiplexer. Connect to Vdd or Ground if not used.
5	Vmux	Multiplexed analog output. Do not connect if multiplexer is not used.
6	S0	MUX selector 0 (See Output Select Table). Connect to Vdd or Ground if not used.
7	S1	MUX selector 1 (See Output Select Table). Connect to Vdd or Ground if not used.
8	Vdd	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor (C ₁).
9	Enable	Enable: High - Normal operation; Low - Device is in standby, power down mode
10	ST	Self Test: Low - Normal operation; High - Device is in self-test mode
11	NC	Not Connected Internally (can be connected to Vdd or Gnd)
12	GND	Ground
13	Y Output	Analog output of y-channel. Optionally, a capacitor (C ₃) placed between this pin and ground will form a low pass filter.
14	Z Output	Analog output of z-channel. Optionally, a capacitor (C ₄) placed between this pin and ground will form a low pass filter.
	Center pad	Ground

Important Technical Note: Power Up / Power Down

Proper functioning of power-on reset (POR) is dependent on the specific Voff and Toff profile of individual applications. It is recommended to minimize Voff and maximize Toff. The application should be evaluated with the range of Voff and Toff expected within the application as POR performance can vary depending on these parameters. In order to guarantee proper reset regardless of Voff and Toff, a software reset can be issued via the SPI protocol. Please refer to Technical Note **KXR94 and KXD94 Accelerometer Reset Sequence** document to ensure proper POR function in your application.

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Application Design Equations

1. The bandwidth is determined by the internal 1kHz low pass filter. The user can lower the bandwidth by placing filter capacitors connected from pins 2, 13 and 14 to ground. The response is single pole. Given a desired bandwidth, f_{BW} , the filter capacitors are determined by:

$$C_2 = C_3 = C_4 = \frac{4.97 \times 10^{-6}}{f_{BW}}$$



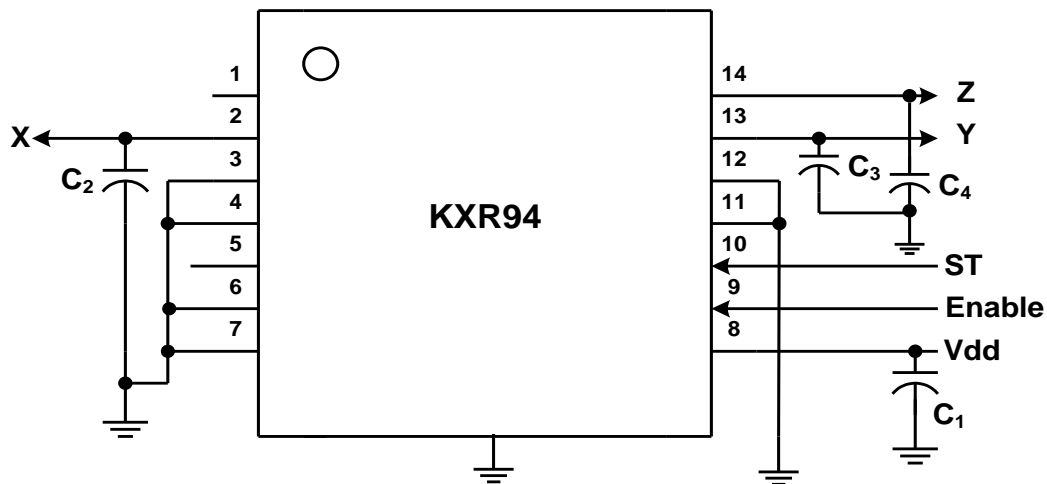
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2. When using not using the multiplexer, the KXR94 is a pin-compatible replacement for Kionix's KXM52 series of accelerometers. The following application schematic should be used:

- Pin 4 (Aux in) = Ground
- Pin 5 (Vmux) = Do Not Connect
- Pin 6 (S0) = Ground
- Pin 7 (S1) = Ground



3. When not connecting the self test pin to a digital I/O port of a microcontroller, Kionix recommends connecting the self test pin to ground.

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USING THE MULTIPLEXED OUTPUT OF THE KXR94

Multiplexer Data Select

The KXR94 features an integrated 4-channel multiplexer. This feature reduces system MCU requirements to only 1 ADC and 2 digital I/O's. The KXR94 uses two select inputs (S0, S1) to control the data flow from Vmux. When a microprocessor toggles the select inputs, the desired output is attained based on the select table. Note that logic 0 is GND and logic 1 is Vdd.

S1	S0	Vmux
0	0	X Output
0	1	Z Output
1	0	Y Output
1	1	Aux. In

Output Select Table

Data Sampling Rate

When operating in its multiplexed mode, the KXR94 has the ability to achieve very high data sampling rates. Internally, the sensor elements (X, Y, and Z) are sequentially sampled in a "round robin" fashion at a rate of 32kHz per axis. Note that this is a differential capacitance sampling of each sensor element, which stores an analog voltage on the filter cap for each axis. Combine this high sensor element sampling rate with the short 5µs settling time of the integrated multiplexer, and the user can achieve a performance very close to that of the 3 separate analog outputs. This is more than sufficient to eliminate any aliasing in the final application since the KXR94 will be operating with a typical bandwidth of ~50Hz and a maximum of 1000Hz.

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Test Specifications

Special Characteristics:

These characteristics have been identified as being critical to the customer. Every part is tested to verify its conformance to specification prior to shipment.

Table 5. Test Specifications

Parameter	Specification	Test Conditions
Zero-g Offset @ RT	1.65 +/- 0.066 V	25C, Vdd = 3.3 V
Sensitivity @ RT	660 +/- 13.2 mV/g	25C, Vdd = 3.3 V
Current Consumption -- Operating	820 <= Idd <= 1080 uA	25C, Vdd = 3.3 V



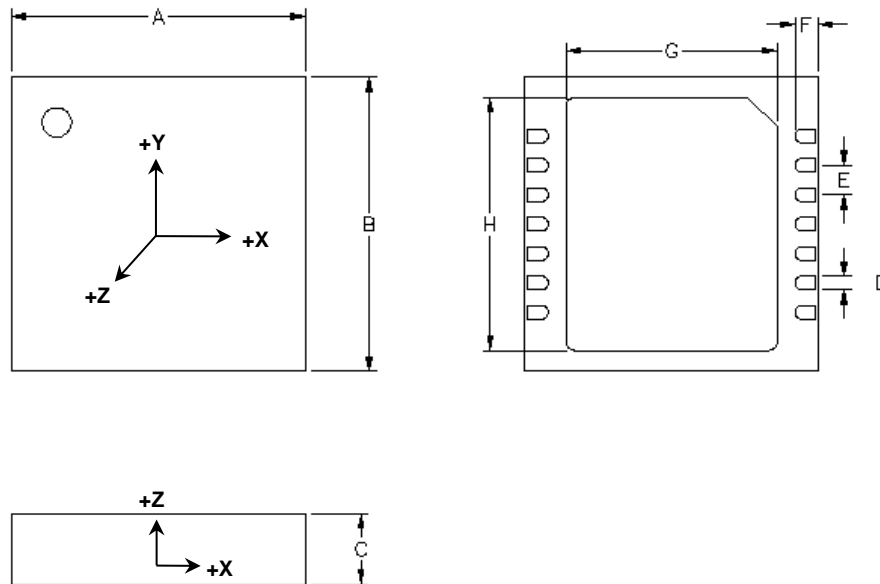
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Package Dimensions and Orientation

5 x 5 x 1.2 mm DFN



Dimension	mm			inch		
	Min	Nom	Max	Min	Nom	Max
A		5.00			0.197	
B		5.00			0.197	
C	1.10	1.20	1.30	0.043	0.047	0.051
D	0.18	0.23	0.28	0.007	0.009	0.011
E		0.50			0.020	
F	0.35	0.40	0.45	0.014	0.016	0.018
G	3.50	3.60	3.70	0.138	0.142	0.146
H	4.20	4.30	4.40	0.165	0.169	0.173

All dimensions and tolerances conform to ASME Y14.5M-1994



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Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

Position	1	2	3	4	5	6
Diagram					Top Bottom	Bottom Top
X	1.65 V	2.31 V	1.65 V	0.99 V	1.65 V	1.65 V
Y	2.31 V	1.65 V	0.99 V	1.65 V	1.65 V	1.65 V
Z	1.65 V	1.65 V	1.65 V	1.65 V	2.31 V	0.99 V
X-Polarity	0	+	0	-	0	0
Y-Polarity	+	0	-	0	0	0
Z-Polarity	0	0	0	0	+	-

↓ (1g)

Earth's Surface

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Revision History

REVISION	DESCRIPTION	DATE
2	Note 1 added to highlight Vdd must not be ramped. Added Digital Interface & SPI reset description	26-Jun-2008
3	Update POR design note	09-May-2014

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