LMV116/LMV118 Low Voltage, 45MHz, Rail-to-Rail Output Operational Amplifiers with Shutdown Option

Check for Samples: LMV116, LMV118

FEATURES

- **(V_S = 2.7V, T_A = 25°C, R_L = 1kΩ to V^+/2, A_V = +1. Typical Values Unless Specified).**
- **−3dB BW 45MHz**
- **Supply Voltage Range 2.7V to 12V**
- **Slew Rate 40V/µs**
- **Supply Current 600µA**
- **Power Down Supply Current 15µA**
- **Output Short Circuit Current 32mA**
- **Linear Output Current ±20mA**
- **Input Common Mode Voltage −0.3V to 1.7V**
- **Output Voltage Swing 20mV from Rails**
- **Input Voltage Noise 40nV/√Hz**
- **Input Current Noise 0.75pA/√Hz**

APPLICATIONS

- **High Speed Clock Buffer/Driver**
- **Active Filters**
- **High Speed Portable Devices**
- **Multiplexing Applications (LMV118)**
- **Current Sense Amplifier**
- **High Speed Transducer Amplifier**

DESCRIPTION

The LMV116 (single) rail-to-rail output voltage feedback amplifiers offer high speed (45MHz), and low voltage operation (2.7V) in addition to micro-power shutdown capability (LMV118).

Output voltage range extends to within 20mV of either supply rail, allowing wide dynamic range especially in low voltage applications. Even with low supply current of 600µA, output current capability is kept at a respectable ±20mA for driving heavier loads. Important device parameters such as BW, Slew Rate and output current are kept relatively independent of the operating supply voltage by a combination of process enhancements and design architecture.

For portable applications, the LMV118 provides shutdown capability while keeping the turn-off current to l5µA. Both turn-on and turn-off characteristics are well behaved with minimal output fluctuations during transitions. This allows the part to be used in power saving mode, as well as multiplexing applications. Miniature packages (SOT-23-5 & SOT-23-6) are further means to ease the adoption of these low power high speed devices in applications where board area is at a premium.

Typical Application

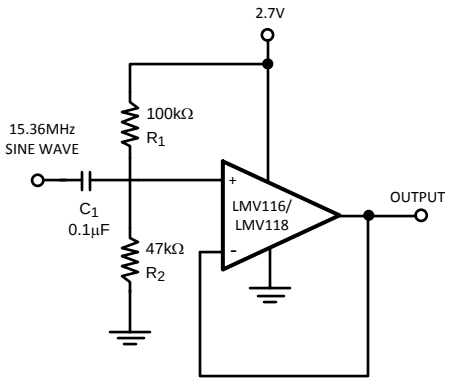


Figure 1. Non-Inverting Clock Buffer Amplifier

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance	Human Body	2KV (3)
	Machine Model	200V (4)
V_{IN} Differential		±2.5V
Output Short Circuit Duration		See (5), (6)
Supply Voltage (V^+ - V^-)		12.6V
Voltage at Input/Output pins		V^+ +0.8V, V^- −0.8V
Storage Temperature Range		−65°C to +150°C
Junction Temperature (7)		+150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead Temp. (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF.
(4) Machine Model, 0Ω in series with 200pF.
(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(6) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
(7) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings (1)

Supply Voltage (V^+ – V^-)		2.5V to 12V
Temperature Range (2)		−40°C to +85°C
Package Thermal Resistance (2) (θ_{JA})	SOT-23-5	265°C/W
	SOT-23-6	265°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

2.7V Electrical Characteristics

Unless otherwise specified, all limits specified for at T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_F = 2kΩ, and R_L = 1kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage	0V ≤ V_{CM} ≤ 1.7V		±1	±5 **±6**	mV
TC V_{OS}	Input Offset Average Drift	See (3)		±5		µV/C
I_B	Input Bias Current	See (4)	−2.0 **−2.2**	−0.40		µA
I_{OS}	Input Offset Current			1	500	nA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 1.55V	73	88		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 3.7V or V^- = 0V to −1V	72	85		dB
R_{IN}	Common Mode Input Resistance			3		MΩ
C_{IN}	Common Mode Input Capacitance			2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB	−0.3 **−0.1**		1.7	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.35V to 2.35V	73 **70**	87		dB
V_O	Output Swing High	R_L = 1kΩ to V^+/2	2.55	2.66		V
		R_L = 10kΩ to V^+/2		2.68		
	Output Swing Low	R_L = 1kΩ to V^+/2	150	40		mV
		R_L = 10kΩ to V^+/2		20		
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (5)	25	35		mA
		Sinking to V^+ V_{ID} = −200mV (5)	25	32		
I_{OUT}	Output Current	V_{OUT} = 0.5V from rails		±20		mA
I_S	Supply Current	Normal Operation		600	900	µA
		Shut-down Mode (LMV118)		15	50	
SR	Slew Rate (6)	A_V = +1, V_O = $1V_{PP}$		40		V/µs
BW	−3dB BW	A_V = +1, V_{OUT} = $200mV_{PP}$		45		MHz
e_n	Input -Referred Voltage Noise	f = 100kHz		40		nV/√Hz
		f = 1kHz		60		
i_n	Input-Referred Current Noise	f = 100kHz		0.75		pA/√Hz
		f = 1kHz		1.20		
t_{on}	Turn-on Time (LMV118)			250		ns
t_{off}	Turn-off Time (LMV118)			560		ns
TH_{SD}	Shut-down Threshold (LMV118)	I_S ≤ 50µA		1.95	2.3	V
I_{SD}	Shutdown Pin Input Current (LMV118)	See (4)		−20		µA

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) Short circuit test is a momentary test. See Absolute Maximum Ratings, Note 6.
(6) Slew rate is the average of the rising and falling slew rates.

5V Electrical Characteristics

Unless otherwise specified, all limits specified for at T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_F = 2kΩ, and R_L = 1kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage	0V ≤ V_{CM} ≤1.7V		±1	±5 **±6**	mV
TC V_{OS}	Input Offset Average Drift	See (3)		±5		µV/C
I_B	Input Bias Current	See (4)	−2.0 **−2.2**	−0.40		µA
I_{OS}	Input Offset Current			1	500	nA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.8V	77	85		dB
PSRR	Power Supply Rejection Ratio	V^+ = 5V to 6V or V^- = 0V to −1V	72	95		dB
R_{IN}	Common Mode Input Resistance			3		MΩ
C_{IN}	Common Mode Input Capacitance			2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB	−0.3 **−0.1**		4.0	V
A_{VOL}	Large Signal Voltage Gain	V_O = 1.5V to 3.5V	73 **70**	85		dB
V_O	Output Swing High	R_L = 1kΩ to V^+/2	4.80	4.95		V
		R_L = 10kΩ to V^+/2		4.98		
	Output Swing Low	R_L = 1kΩ to V^+/2	200	50		mV
		R_L = 10kΩ to V^+/2		20		
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (5)	35	45		mA
		Sinking to V^+ V_{ID} = −200mV (5)	35	43		
I_{OUT}	Output Current	V_{OUT} = 0.5V from rails		±20		mA
I_S	Supply Current	Normal Operation		600	900	µA
		Shut-down Mode (LMV118)		10	50	
SR	Slew Rate (6)	A_V = +1, V_O = 1V_{PP}		40		V/µs
BW	−3dB BW	A_V = +1, V_{OUT} = 200mV_{PP}		45		MHz
e_n	Input -Referred Voltage Noise	f = 100kHz		40		nV/√Hz
		f = 1kHz		60		
i_n	Input-Referred Current Noise	f = 100kHz		0.75		pA/√Hz
		f = 1kHz		1.20		
t_{on}	Turn-on Time (LMV118)			210		ns
t_{off}	Turn-off Time (LMV118)			500		ns
TH_{SD}	Shut-down Threshold (LMV118)	I_S ≤ 50µA		4.25	4.60	V
I_{SD}	Shutdown Pin Input Current (LMV118)	See (4)		−20		µA

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) Short circuit test is a momentary test. See Absolute Maximum Ratings, Note 6.
(6) Slew rate is the average of the rising and falling slew rates.

±5V Electrical Characteristics

Unless otherwise specified, all limits specified for at T_J = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0V, and R_F = 2kΩ, and R_L = 1kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage	−5V ≤ V_{CM} ≤ 1.7V		±1	±5 **±6**	mV
TC V_{OS}	Input Offset Average Drift	See (3)		±5		µV/C
I_B	Input Bias Current	See (4)	−2.0 **−2.2**	−0.40		µA
I_{OS}	Input Offset Current			3	500	nA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −5V to 3.5V	78	104		dB
PSRR	Power Supply Rejection Ratio	V^+ = 5V to 6V or V^- = −5V to −6V	72	95		dB
R_{IN}	Common Mode Input Resistance			3		MΩ
C_{IN}	Common Mode Input Capacitance			2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB	−5.3 **−5.1**		4.0	V
A_{VOL}	Large Signal Voltage Gain	V_O = −2V to 2V	74 **71**	85		dB
V_O	Output Swing High	R_L = 1kΩ	4.70	4.92		V
		R_L = 10kΩ		4.97		
	Output Swing Low	R_L = 1kΩ	−4.70	−4.93		mV
		R_L = 10kΩ		−4.98		
I_{SC}	Output Short Circuit Current	Sourcing to 0V V_{ID} = 200mV (5)	40	57		mA
		Sinking to 0V V_{ID} = −200mV (5)	40	54		
I_{OUT}	Output Current	V_{OUT} = 0.5V from rails		±20		mA
I_S	Supply Current	Normal Operation		600	900	µA
		Shut-down Mode (LMV118)		15	50	
SR	Slew Rate (6)	A_V = +1, V_O = $1V_{PP}$		35		V/µs
BW	−3dB BW	A_V = +1, V_{OUT} = $200mV_{PP}$		45		MHz
e_n	Input -Referred Voltage Noise	f = 100kHz		40		nV/√Hz
		f = 1kHz		60		
i_n	Input-Referred Current Noise	f = 100kHz		0.75		pA/√Hz
		f = 1kHz		1.20		
t_{on}	Turn-on Time (LMV118)			200		ns
t_{off}	Turn-off Time (LMV118)			700		ns
TH_{SD}	Shut-down Threshold (LMV118)	I_S ≤ 50µA		4.25	4.60	V
I_{SD}	Shutdown Pin Input Current (LMV118)	See (4)		−20		µA

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) Short circuit test is a momentary test. See Absolute Maximum Ratings, Note 6.
(6) Slew rate is the average of the rising and falling slew rates.

Connection Diagram

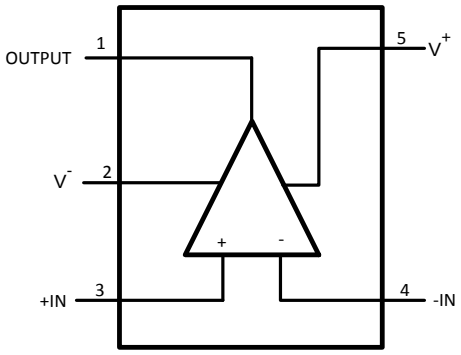


Figure 2. SOT-23-5 (LMV116)
Top View

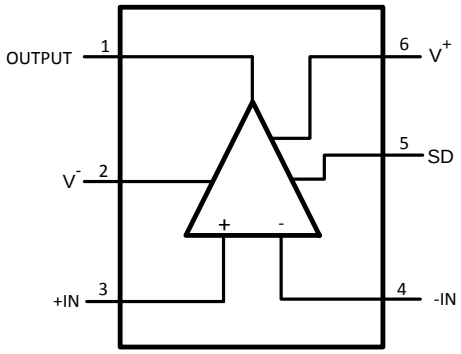


Figure 3. SOT-23-6 (LMV118)
Top View

Typical Performance Characteristics

At T_J = 25°C. Unless otherwise specified.

Supply Current vs. Supply Voltage

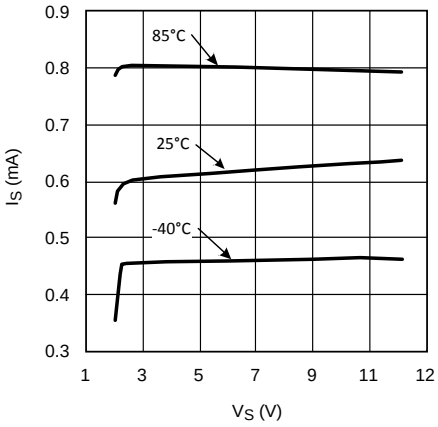


Figure 4.

Supply Current vs. V_{CM}

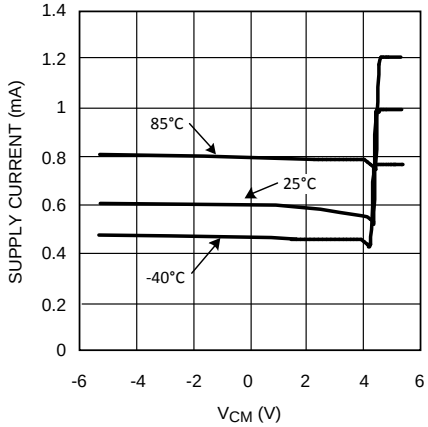


Figure 5.

Gain and Phase vs. Frequency

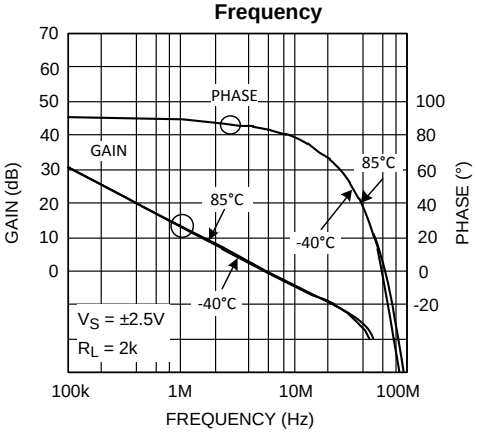


Figure 6.

CMRR vs. Frequency

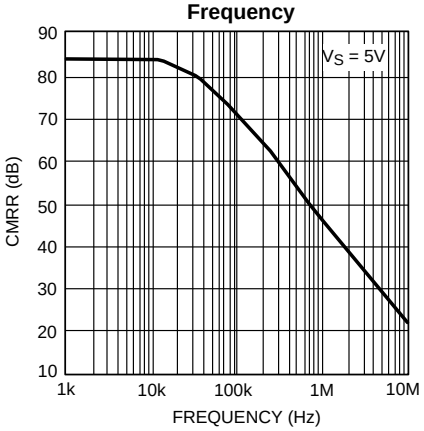


Figure 7.

PSRR vs. Frequency

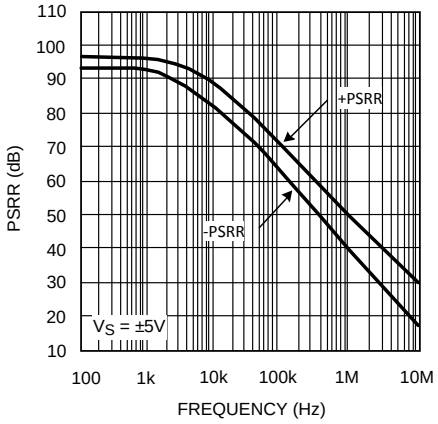


Figure 8.

Input Voltage Noise vs. Frequency

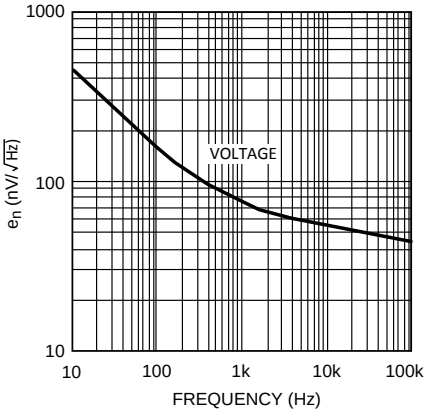


Figure 9.

Typical Performance Characteristics (continued)

At T_J = 25°C. Unless otherwise specified.

Input Current Noise vs. Frequency

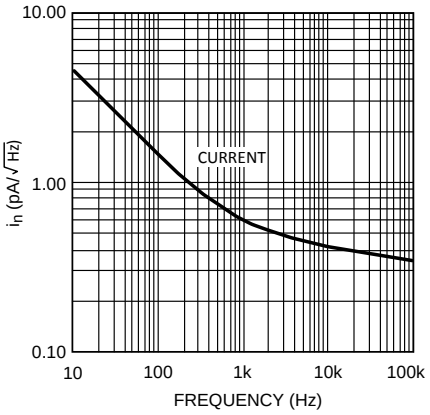


Figure 10.

Closed Loop Frequency Response for Various Temperature

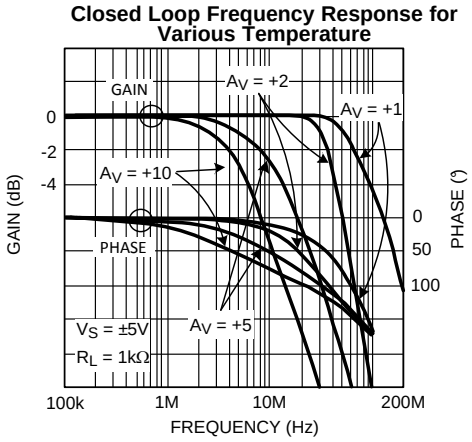


Figure 11.

Frequency Response for Various (A_V)

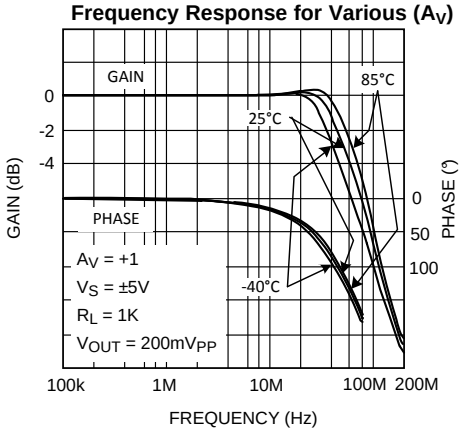


Figure 12.

Large Signal Step Response

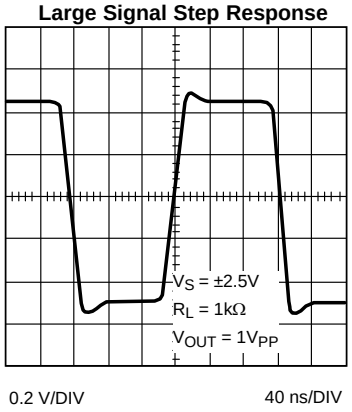


Figure 13.

Offset Voltage vs. Common Mode Voltage (A Typical Unit)

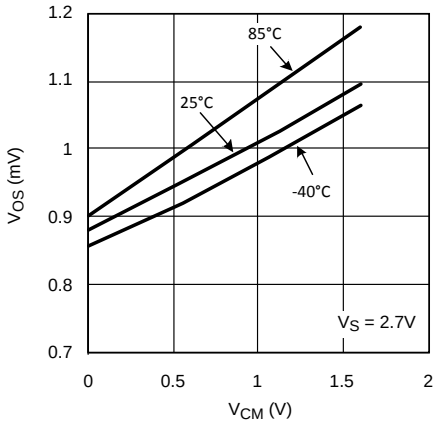


Figure 14.

Offset Voltage vs. Common Mode Voltage (A Typical Unit)

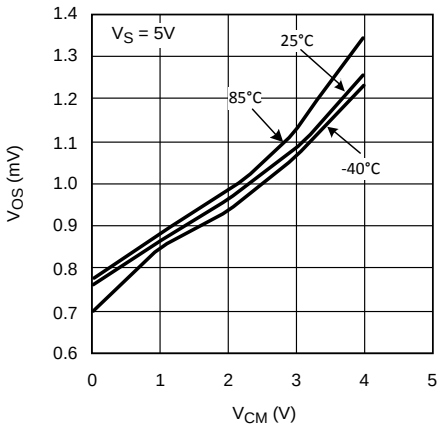


Figure 15.

Typical Performance Characteristics (continued)

At T_J = 25°C. Unless otherwise specified.

Offset Voltage vs. Common Mode Range (A Typical Unit)

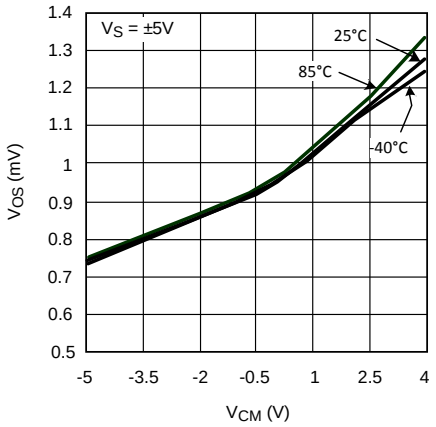


Figure 16.

Input Bias Current vs. Supply Voltage

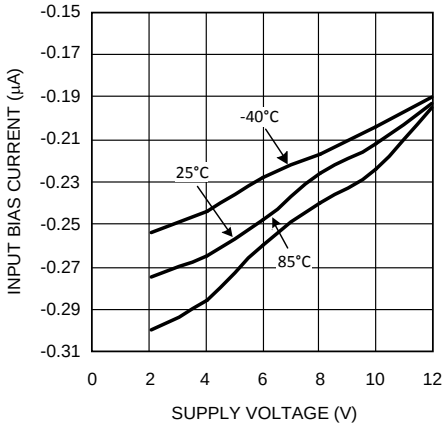


Figure 17.

Input Bias Current vs. V_{CM}

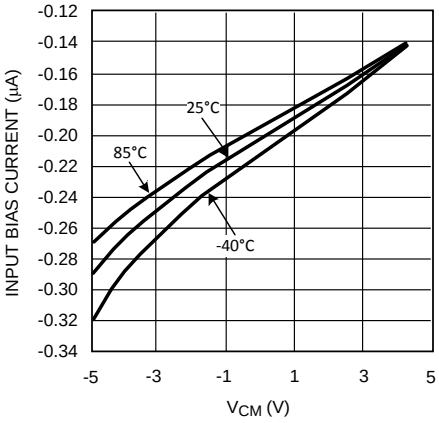


Figure 18.

Sink Current vs. V_{OUT}

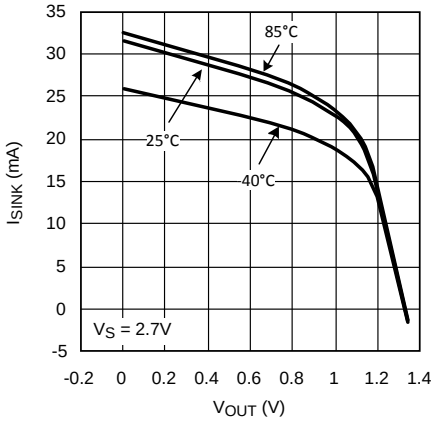


Figure 19.

Sink Current vs. V_{OUT}

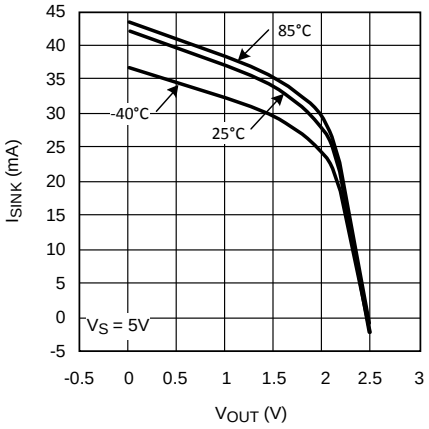


Figure 20.

Typical Performance Characteristics (continued)

At T_J = 25°C. Unless otherwise specified.

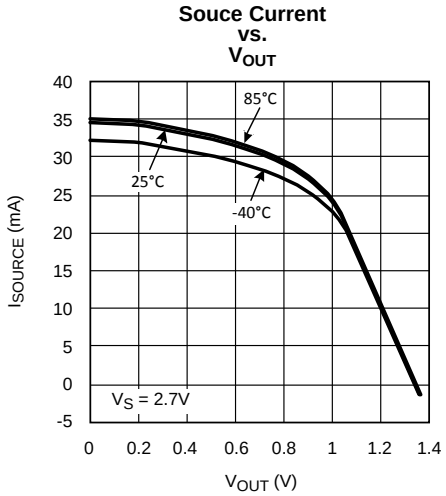


Figure 21.

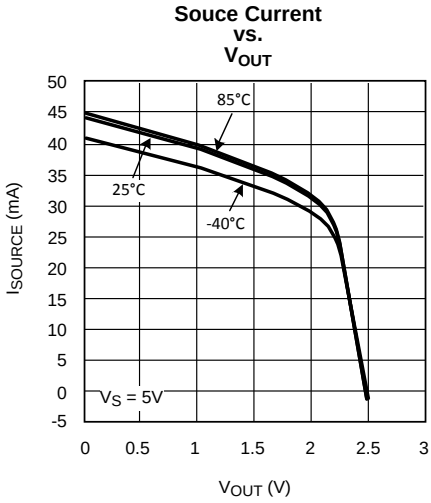


Figure 22.

APPLICATION NOTES

CIRCUIT DESCRIPTION

The LMV116 and LMV118 are based on TI's proprietary VIP10 dielectrically isolated bipolar process.

The LMV116 and LMV118 architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8GHz) even under low supply voltage (2.7V) and low Collector bias current.
- Common Emitter push-pull output stage capable of 20mA output current (at 0.5V from the supply rails) while consuming only 600µA of total supply current. This architecture allows output to reach within milli-volts of either supply rail at light loads.
- Consistent performance from any supply voltage (2.7V-10V) with little variation with supply voltage for the most important specifications (e.g. BW, SR, I_{OUT}, etc.)

APPLICATION HINTS

When the output swing approaches either supply rail, the output transistor will enter a Quasi-saturated state. A subtle effect of this operational region is that there is an increase in supply current in this state (up to 1 mA). The onset of Quasi-saturation region is a function of output loading (current) and varies from 100 mV at no load to about 1V when output is delivering 20 mA, as measured from supplies. Both input common mode voltage and output voltage level effect the supply current (see typical performance characteristics for plot).

MICRO-POWER SHUTDOWN

The LMV118 can be shutdown to save power and reduce its supply current to less than 50µA specified, by applying a voltage to the SD pin. The SD pin is "active high" and needs to be tied to V^- for normal operation. This input is low current (<20µA, 4pF equivalent capacitance) and a resistor to V^- (≤20kΩ) will result in normal operation. Shutdown is specified when SD pin is 0.4V or less from V^+ at any operating supply voltage and temperature.

In the shutdown mode, essentially all internal device biasing is turned off in order to minimize supply current flow and the output goes into Hi-Z (high impedance) mode. Complete device Turn-on and Turn-off times vary considerably relative to the output loading conditions, output voltage, and input impedance, but is generally limited to less than 1µs (see tables for actual data).

During shutdown, the input stage has an equivalent circuit as shown below in Figure 23.

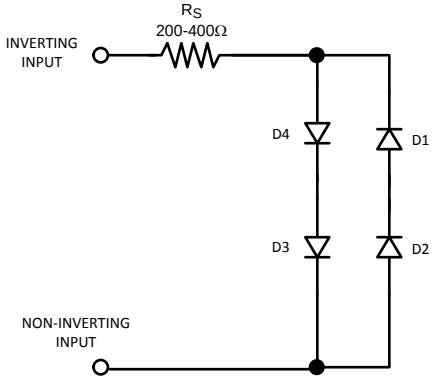


Figure 23.

As can be seen above, in shutdown, there may be current flow through the internal diodes shown, caused by input potential, if present. This current may flow through the external feedback resistor and result in an apparent output signal. In most shutdown applications the presence of this output is inconsequential. However, if the output is "forced" by another device such as in a multiplexer, the other device will need to conduct the current described in order to maintain the output potential.

To keep the output at or near ground during shutdown when there is no other device to hold the output low, a switch (transistor) could be used to shunt the output to ground. Figure 24 shows a circuit where a NPN bipolar is used to keep the output near ground (~80mV):

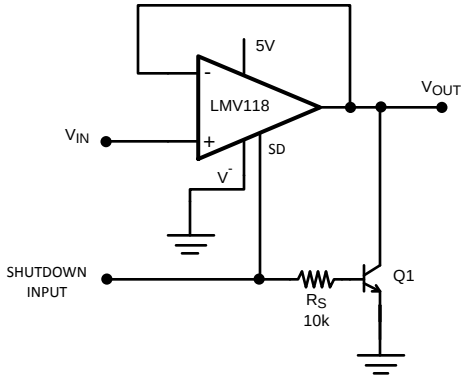


Figure 24. Active Pull-Down Schematic

Figure 25 shows the output waveform.

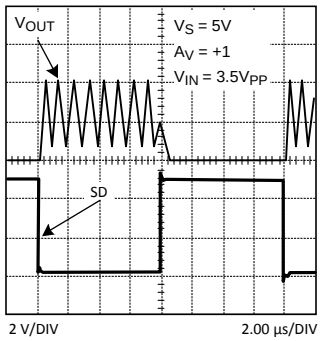


Figure 25. Output Held Low by Active Pull-Down Circuit

If bipolar transistor power dissipation is not tolerable, the switch could be by a N-channel enhancement mode MOSFET.

2.7V SINGLE SUPPLY 2:1 MUX

The schematic show in Figure 26 will function as a 2:1 MUX operating on a single 2.7V power supply, by utilizing the shutdown feature of the LMV118.

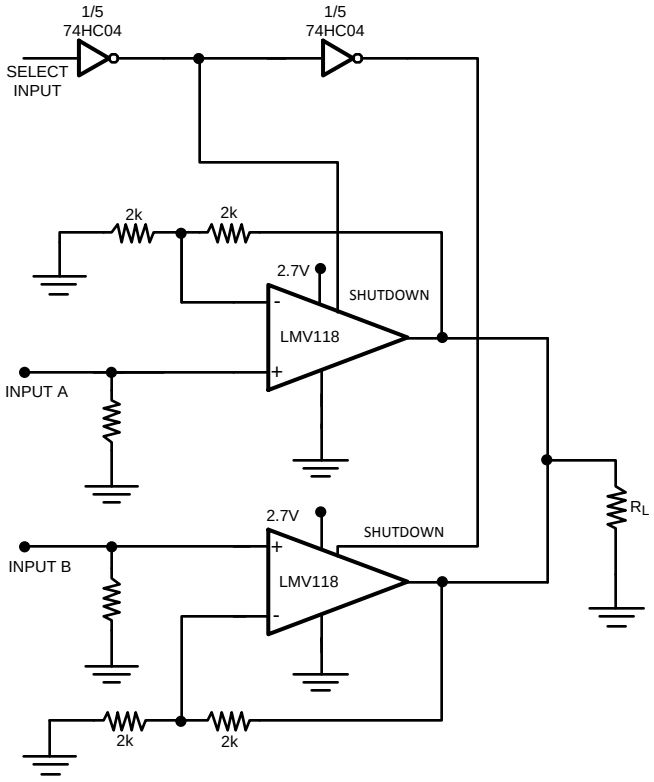


Figure 26. 2:1 MUX Operating off a 2.7V Single Supply

Figure 27 shows the MUX output when selecting between a 1MHz sine and a 250kHz triangular waveform.

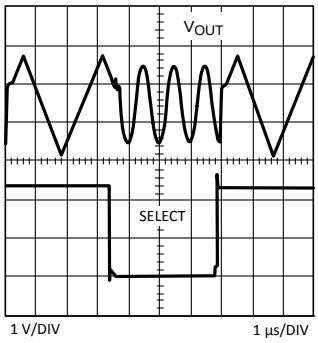


Figure 27. 2:1 MUX Output

As can be seen in Figure 27, the output is well behaved and there are no spikes or glitches due to the switching. Switching times are approximately around 500ns based on the time when the output is considered “valid”.

PRINTED CIRCUIT BOARD LAYOUT, COMPONENT VALUES SELECTION, AND EVALUATION BOARDS

Generally, a good high-frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 (SNOA367) for more information).

Another important parameter, is the component values selection. Choosing large valued external resistors, will effect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These capacitors could be inherent to the device or a by-product of the board layout and component placement. Either way, keeping the resistor values lower, will diminish this interaction. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation.

TI suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board PN
LMV116	SOT-23-5	CLC730068
LMV118	SOT-23-6	CLC730116

These free evaluation boards are shipped when a device sample request is placed with TI.

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV116MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	AC1A	Samples
LMV116MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	AC1A	Samples
LMV118MF	NRND	SOT-23	DBV	6	1000	TBD	Call TI	Call TI	-40 to 85	AD1A	
LMV118MF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	AD1A	Samples
LMV118MFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	AD1A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

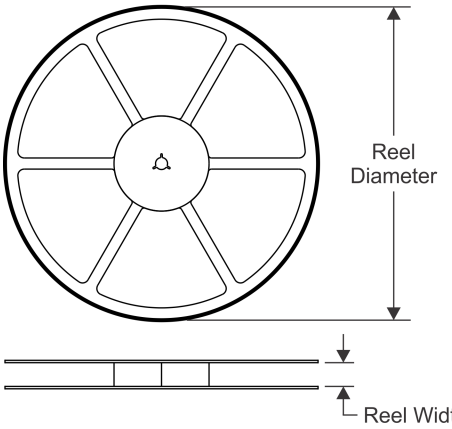
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

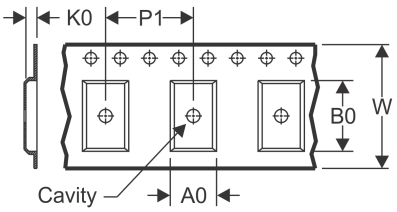
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

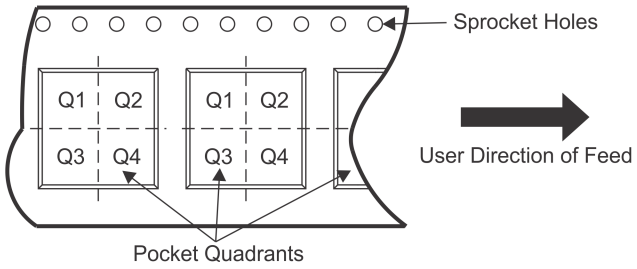


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

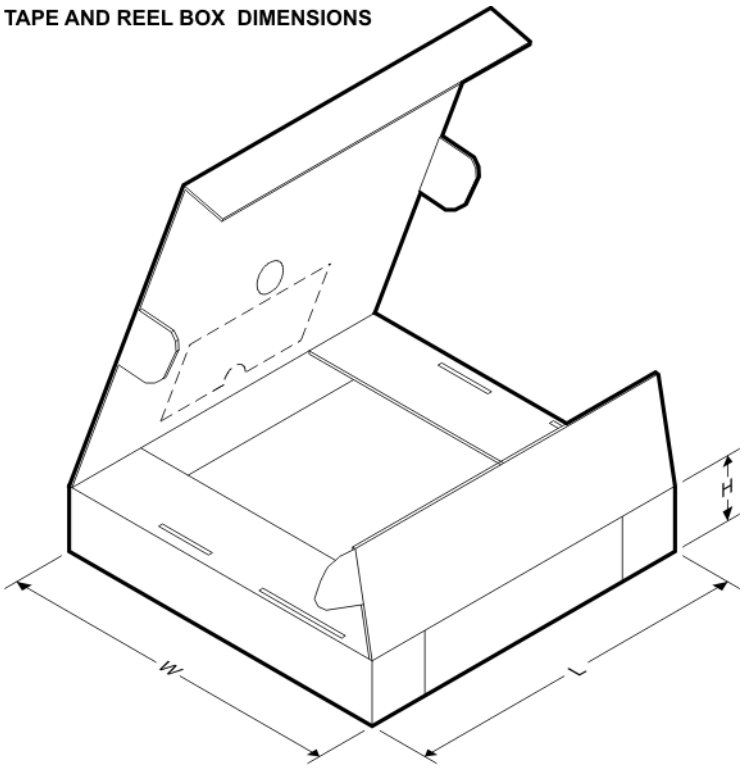
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV116MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV116MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV118MF	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV118MF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV118MFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

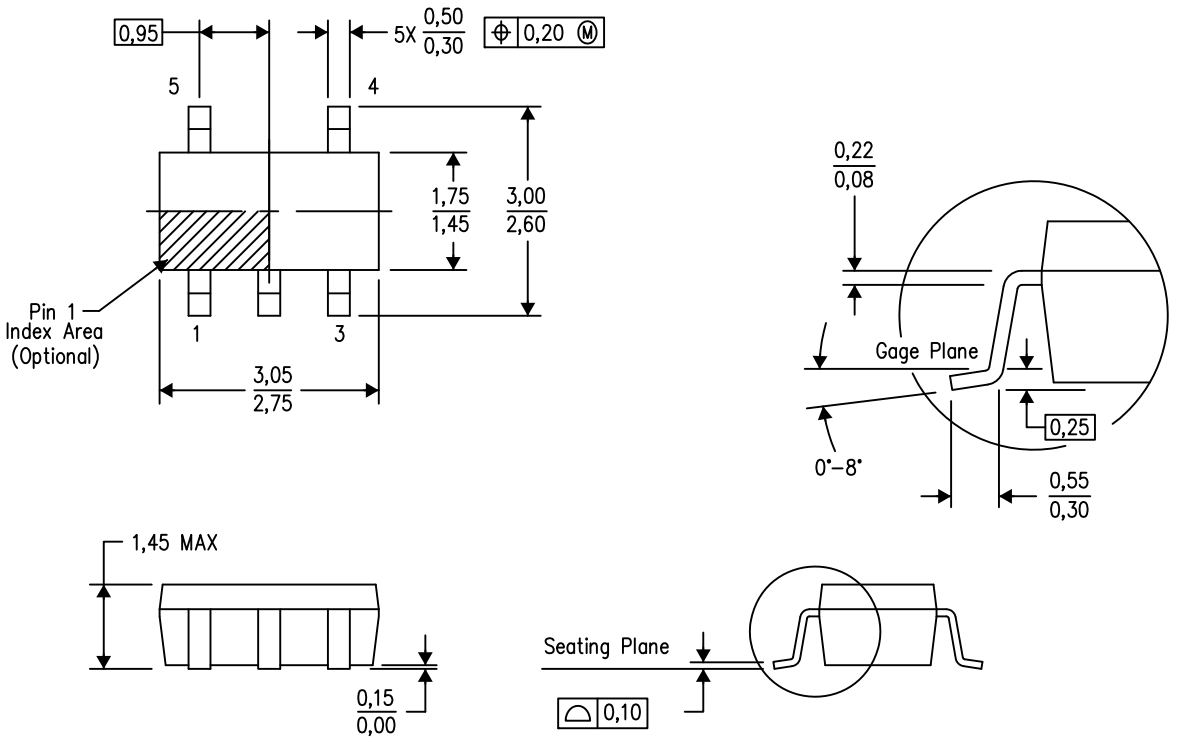
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV116MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV116MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV118MF	SOT-23	DBV	6	1000	210.0	185.0	35.0
LMV118MF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LMV118MFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0

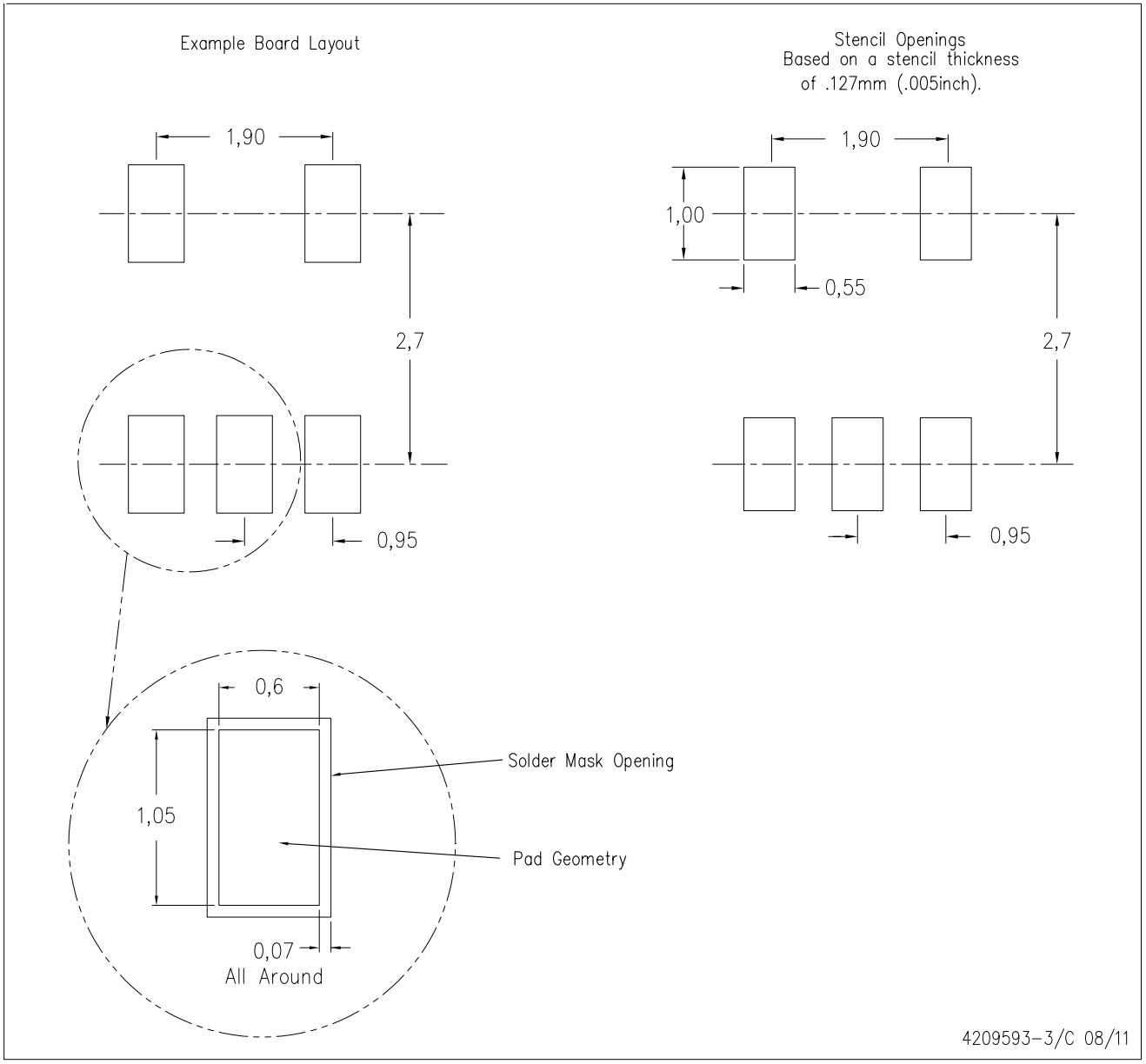
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

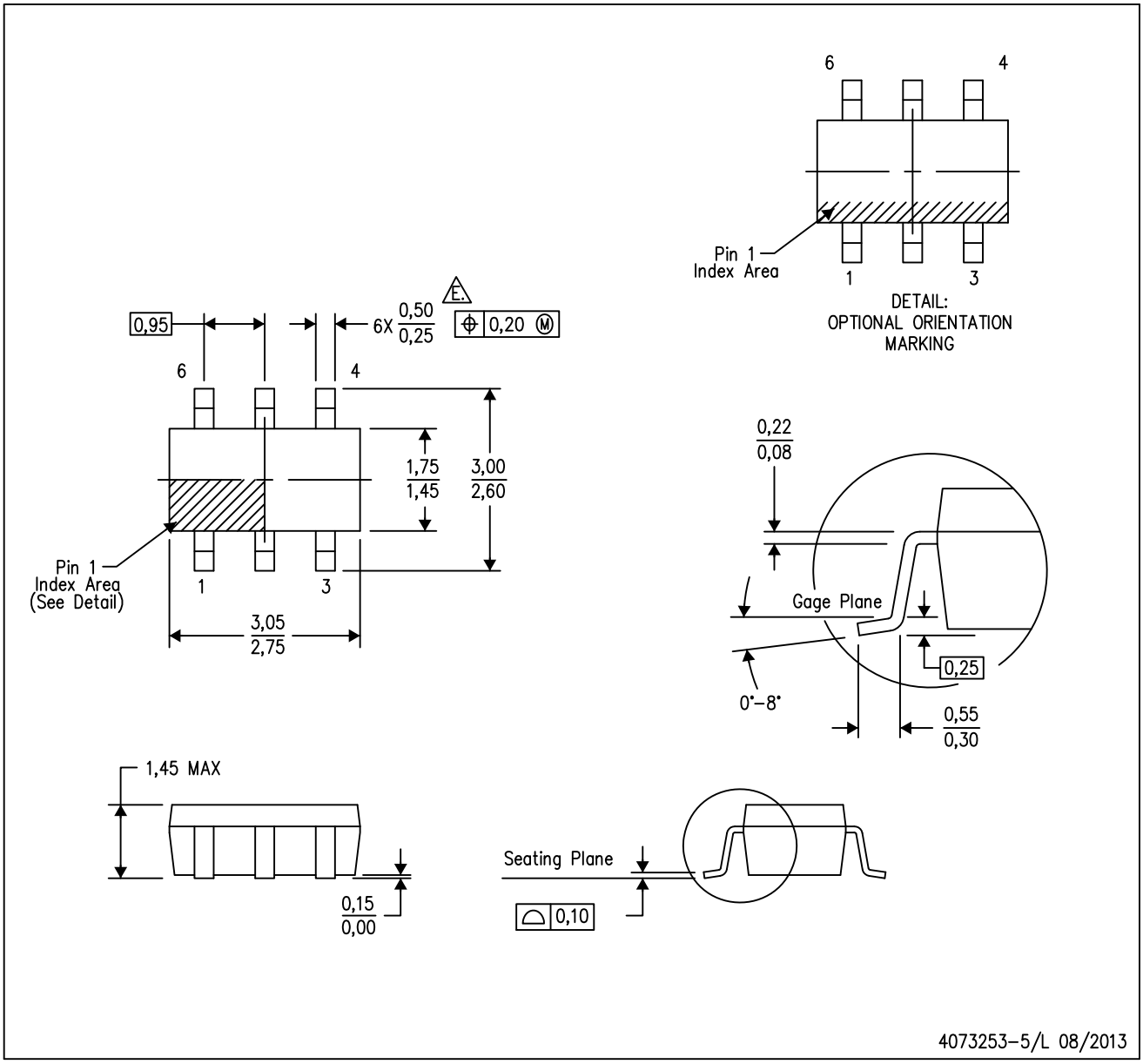
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

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