



FDMA410NZ

Single N-Channel 1.5 V Specified PowerTrench[®] MOSFET 20 V, 9.5 A, 23 mΩ

Features

- Max $r_{DS(on)}$ = 23 mΩ at $V_{GS} = 4.5$ V, $I_D = 9.5$ A
- Max $r_{DS(on)}$ = 29 mΩ at $V_{GS} = 2.5$ V, $I_D = 8.0$ A
- Max $r_{DS(on)}$ = 36 mΩ at $V_{GS} = 1.8$ V, $I_D = 4.0$ A
- Max $r_{DS(on)}$ = 50 mΩ at $V_{GS} = 1.5$ V, $I_D = 2.0$ A
- HBM ESD protection level > 2.5 kV (Note 3)
- Low Profile-0.8 mm maximum in the new package MicroFET 2x2 mm
- Free from halogenated compounds and antimony oxides
- RoHS Compliant

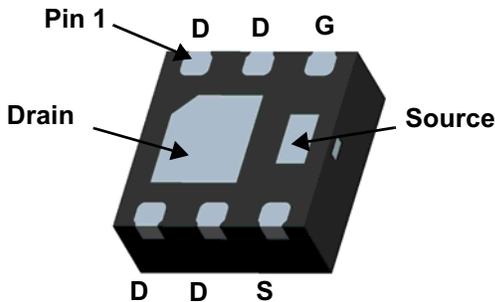


General Description

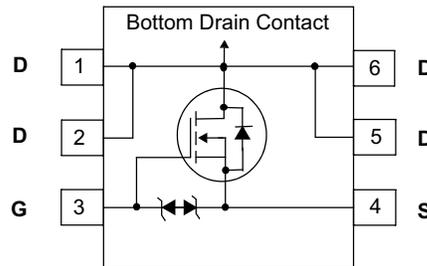
This Single N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the $r_{DS(on)}$ @ $V_{GS} = 1.5$ V on special MicroFET leadframe.

Applications

- Li-Ion Battery Pack
- Baseband Switch
- Load Switch
- DC-DC Conversion



MicroFET 2X2 (Bottom View)



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	-Continuous $T_A = 25$ °C (Note 1a)	9.5	A
	-Pulsed	24	
P_D	Power Dissipation $T_A = 25$ °C (Note 1a)	2.4	W
	Power Dissipation $T_A = 25$ °C (Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
410	FDMA410NZ	MicroFET 2X2	7"	8 mm	3000 units

FDMA410NZ Single N-Channel 1.5 V Specified PowerTrench[®] MOSFET

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		17		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	0.4	0.7	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 4.5\text{ V}$, $I_D = 9.5\text{ A}$		17	23	m Ω
		$V_{GS} = 2.5\text{ V}$, $I_D = 8.0\text{ A}$		20	29	
		$V_{GS} = 1.8\text{ V}$, $I_D = 4.0\text{ A}$		24	36	
		$V_{GS} = 1.5\text{ V}$, $I_D = 2.0\text{ A}$		29	50	
		$V_{GS} = 4.5\text{ V}$, $I_D = 9.5\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		23	32	
g_{FS}	Forward Transconductance	$V_{DD} = 5\text{ V}$, $I_D = 9.5\text{ A}$		35		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		815	1080	pF
C_{oss}	Output Capacitance			130	175	pF
C_{rss}	Reverse Transfer Capacitance			85	130	pF
R_g	Gate Resistance	$f = 1\text{ MHz}$		2.1		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{ V}$, $I_D = 9.5\text{ A}$, $V_{GS} = 4.5\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		7.5	15	ns
t_r	Rise Time			3.9	10	ns
$t_{d(off)}$	Turn-Off Delay Time			27	44	ns
t_f	Fall Time			3.7	10	ns
Q_g	Total Gate Charge			10	14	nC
Q_{gs}	Gate to Source Charge	$V_{GS} = 4.5\text{ V}$, $V_{DD} = 10\text{ V}$, $I_D = 9.5\text{ A}$		1.2		nC
Q_{gd}	Gate to Drain "Miller" Charge			2.0		nC

Drain-Source Diode Characteristics

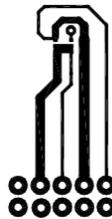
I_S	Maximum Continuous Drain-Source Diode Forward Current			2.0	A	
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2.0\text{ A}$ (Note 2)		0.7	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 9.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		12	22	ns
Q_{rr}	Reverse Recovery Charge			2.6	10	nC

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. $52\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper.



b. $145\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

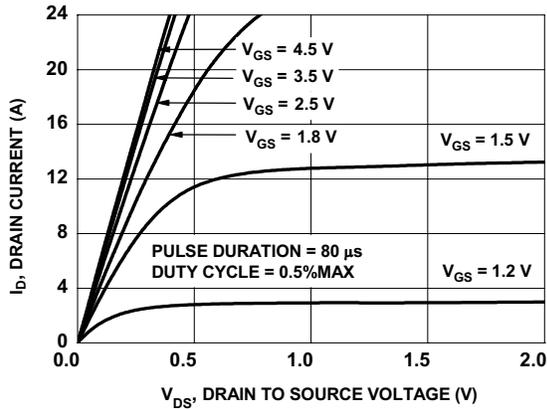


Figure 1. On-Region Characteristics

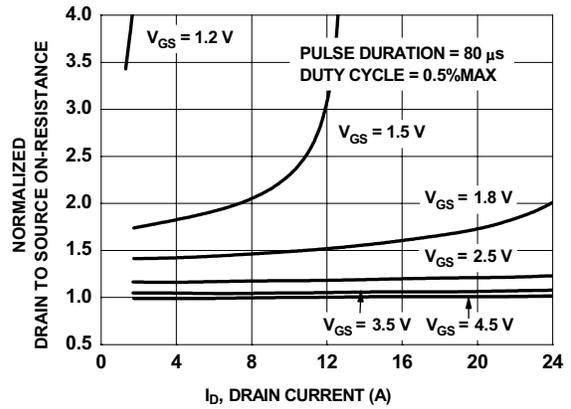


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

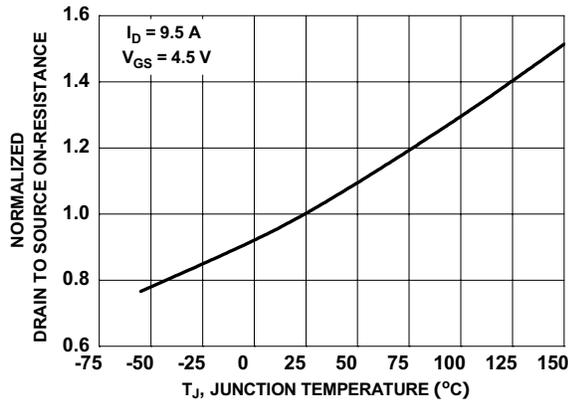


Figure 3. Normalized On-Resistance vs Junction Temperature

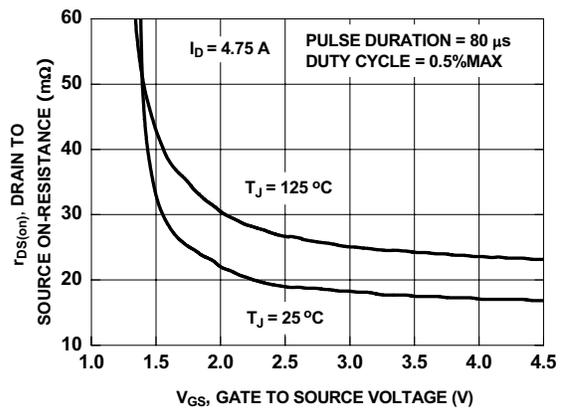


Figure 4. On-Resistance vs Gate to Source Voltage

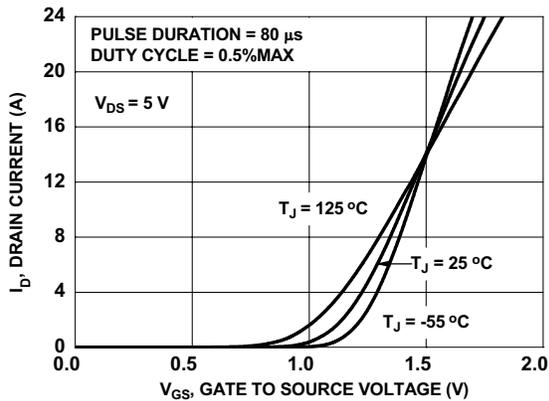


Figure 5. Transfer Characteristics

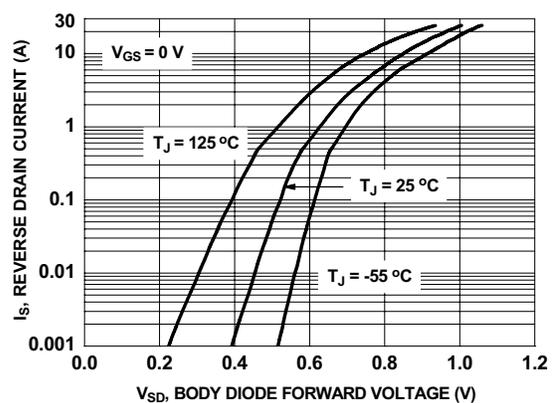


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

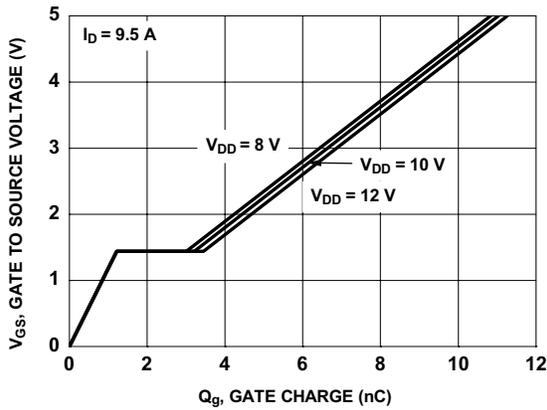


Figure 7. Gate Charge Characteristics

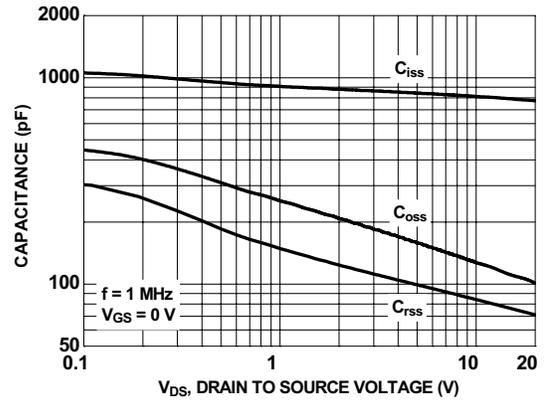


Figure 8. Capacitance vs Drain to Source Voltage

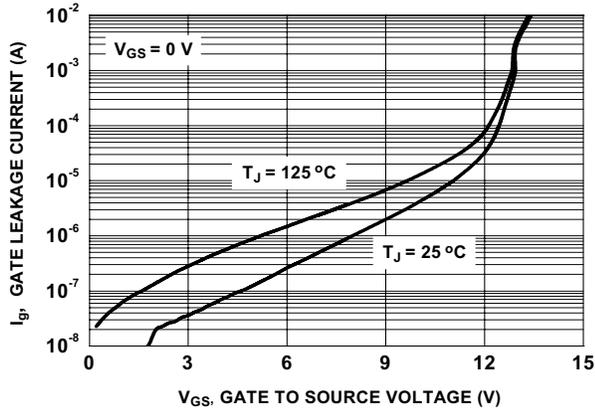


Figure 9. Gate Leakage Current vs Gate to Source Voltage

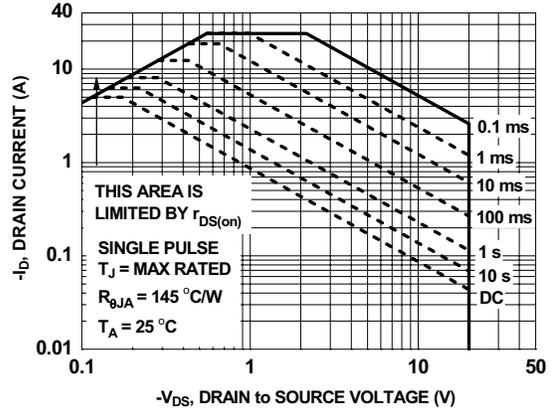


Figure 10. Forward Bias Safe Operation Area

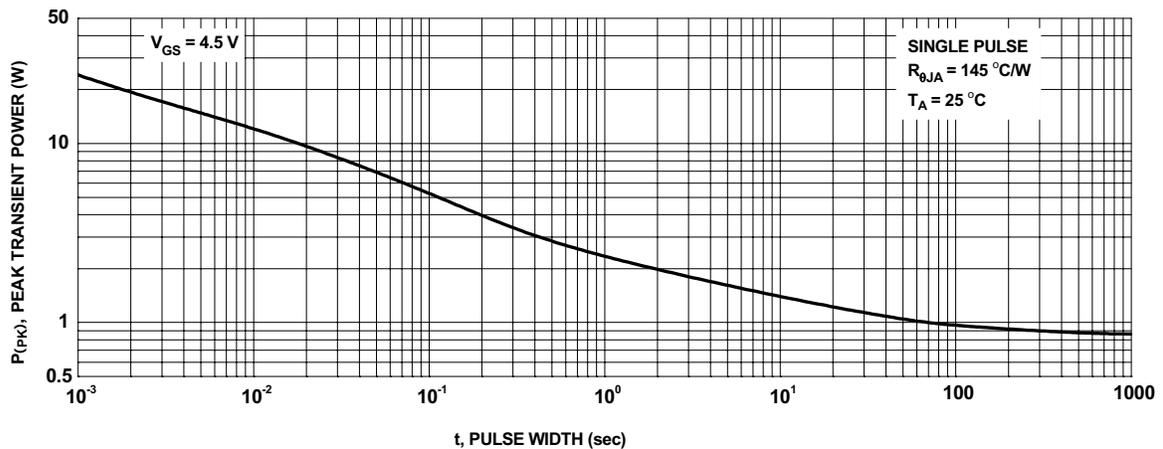


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

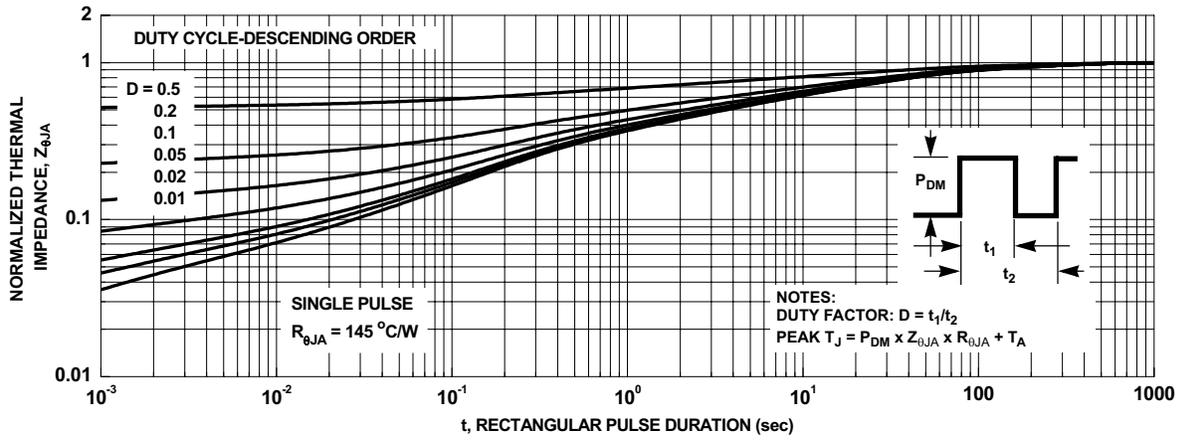
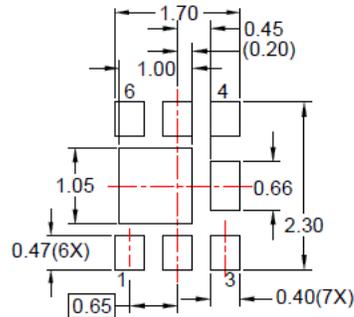
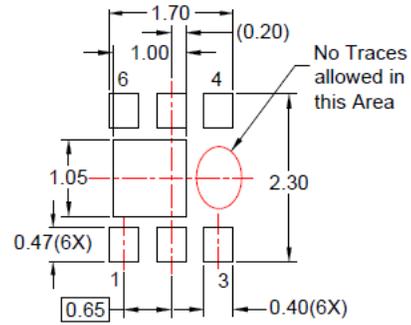
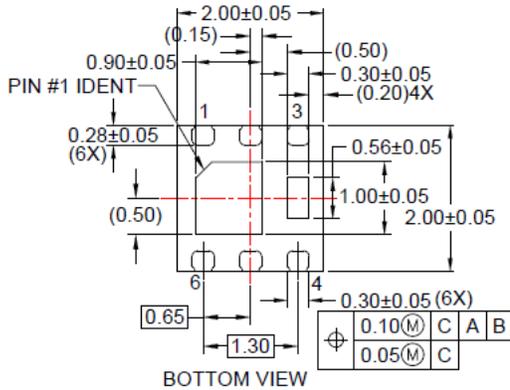
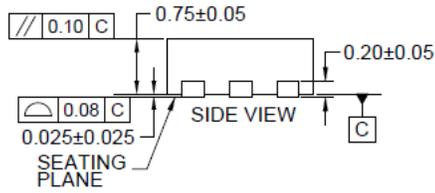
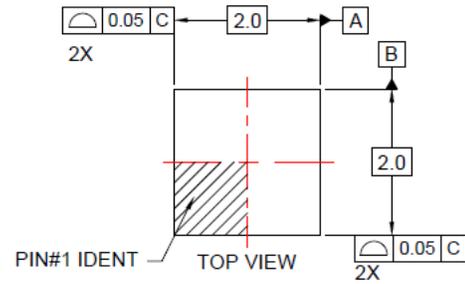


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP06Lrev4.



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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