

# FDN361BN

## 30V N-Channel, Logic Level, PowerTrench® MOSFET

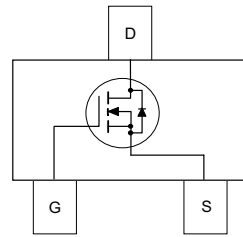
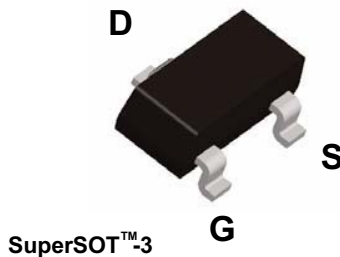
### General Description

These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

### Features

- 1.4 A, 30 V.  $R_{DS(ON)} = 110 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 160 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- Low gate charge
- Industry standard outline SOT-23 surface mount package using proprietary SuperSOT™-3 design for superior thermal and electrical capabilities
- High performance trench technology for extremely low  $R_{DS(ON)}$



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	30	V
V <sub>GSS</sub>	Gate-Source Voltage	± 20	V
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	1.4	A
	– Pulsed	10	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a) (Note 1b)	0.5	W
		0.46	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	–55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	75	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
361B	FDN361BN	7"	8mm	3000 units

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		26		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			10	$\mu\text{A}$
$I_{GSS}$	Gate–Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	2.1	3	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 1.4\text{ A}$		92	110	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 1.2\text{ A}$		120	160	
		$V_{GS} = 10\text{ V}, I_D = 1.4\text{ A}, T_J = 125^\circ\text{C}$		114	150	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	3.5			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 1.4\text{ A}$		4		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		145	193	pF
$C_{oss}$	Output Capacitance			35	47	pF
$C_{rss}$	Reverse Transfer Capacitance			15	23	pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		1.6		$\Omega$

### Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		3	6	ns
$t_r$	Turn–On Rise Time			8	16	ns
$t_{d(off)}$	Turn–Off Delay Time			16	29	ns
$t_f$	Turn–Off Fall Time			2	4	ns
$Q_g$	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 1.4\text{ A},$ $V_{GS} = 4.5\text{ V}$		1.3	1.8	nC
$Q_{gs}$	Gate–Source Charge			0.5		nC
$Q_{gd}$	Gate–Drain Charge			0.5		nC

### Drain–Source Diode Characteristics

$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.42\text{ A}$ (Note 2)		0.8	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 1.4\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$		11	22	nS
$Q_{rr}$	Diode Reverse Recovery Charge			4		nC

#### Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $250^\circ\text{C}/\text{W}$  when mounted on a  $0.02\text{ in}^2$  pad of 2 oz. copper.



b)  $270^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

### Typical Characteristics

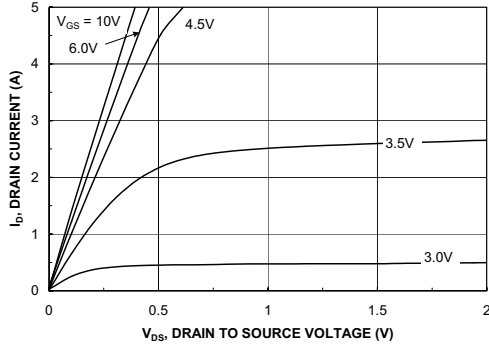


Figure 1. On-Region Characteristics.

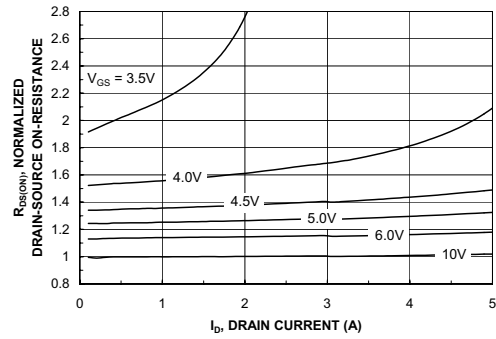


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

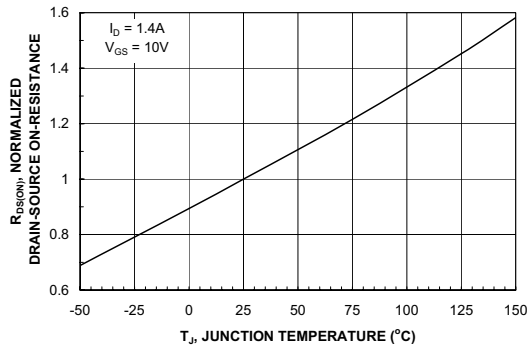


Figure 3. On-Resistance Variation with Temperature.

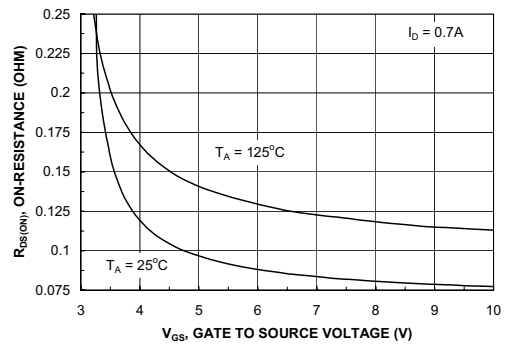


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

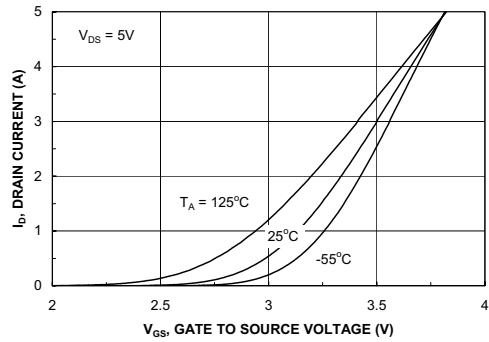


Figure 5. Transfer Characteristics.

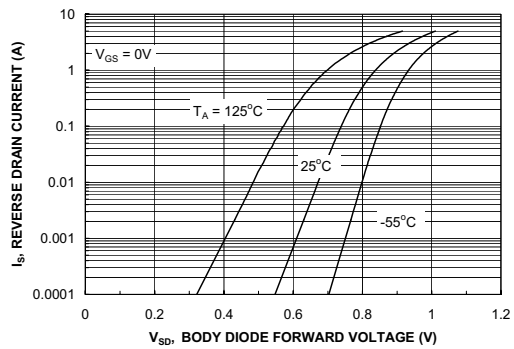


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics

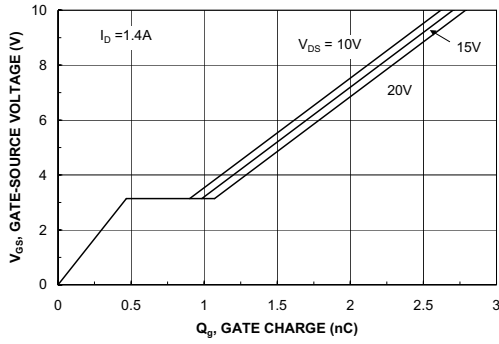


Figure 7. Gate Charge Characteristics.

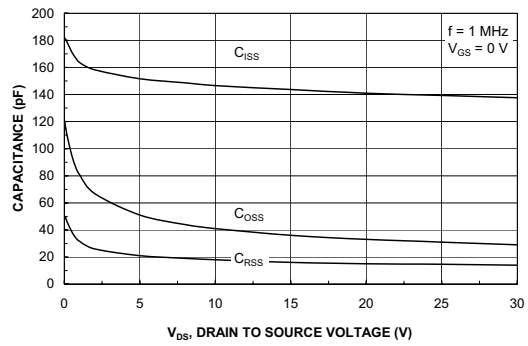


Figure 8. Capacitance Characteristics.

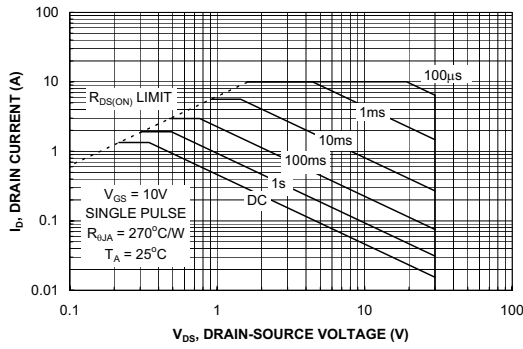


Figure 9. Maximum Safe Operating Area.

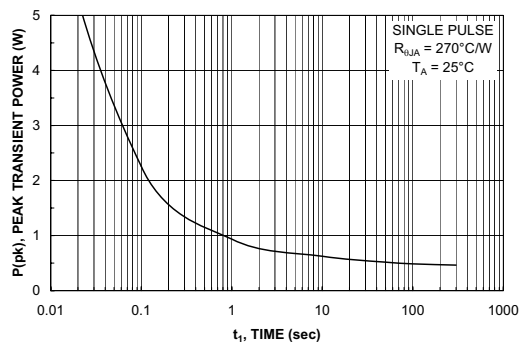


Figure 10. Single Pulse Maximum Power Dissipation.

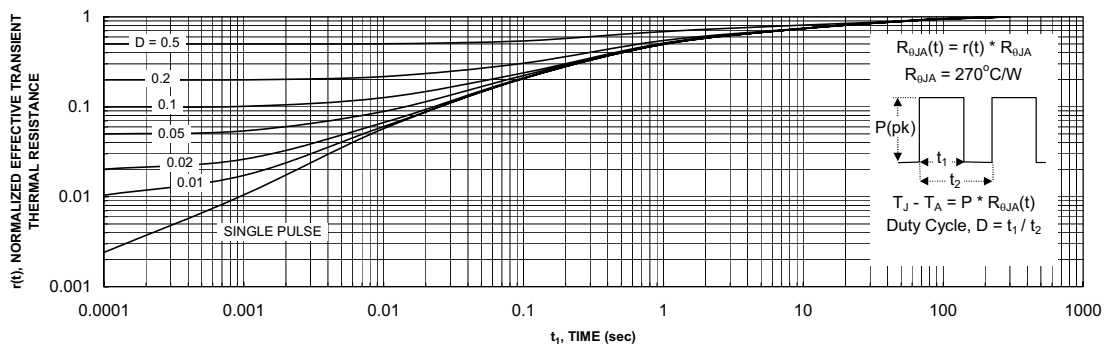


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.


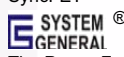



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