EN23F0QI
15A Voltage Mode Synchronous Buck PWM DC-DC Converter with Integrated Inductor

Description

The EN23F0QI is a Power System on a Chip (PowerSoC) DC-DC converter. It integrates MOSFET switches, small-signal control circuits, compensation and an integrated inductor in an advanced 12x13x3mm QFN module. It offers high efficiency, excellent line and load regulation. The EN23F0QI operates over a wide input voltage range and is specifically designed to meet the precise voltage and fast transient requirements of high-performance products. The EN23F0QI features frequency synchronization to an external clock, power OK output voltage monitor, programmable soft-start along with thermal and over current protection. The device's advanced circuit design, ultra high switching frequency and proprietary integrated inductor technology delivers high-quality, ultra compact, non-isolated DC-DC conversion.

The Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, overall system level reliability is improved given the small number of components required with the Enpirion solution.

All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

Features

- Integrated Inductor, MOSFETs, Controller
- Total Solution Size Estimate 308mm^2
- Wide Input Voltage Range: 4.5V – 14V
- 2% V_{OUT} Accuracy (Over Line/Load/Temperature)
- Master/Slave Configuration for Parallel Operation
  - Up to 4 Devices with 48A capability
- Frequency Synchronization (External Clock)
- Output Enable Pin and Power OK Signal
- Programmable Soft-Start Time
- Under Voltage Lockout Protection (UVLO)
- Programmable Over Current Protection
- Thermal Shutdown and Short Circuit Protection
- RoHS compliant, MSL level 3, 260°C reflow

Applications

- Space Constrained Applications
- Distributed Power Architectures
- Output Voltage Ripple Sensitive Applications
- Beat Frequency Sensitive Applications
- Servers, Embedded Computing Systems, LAN/SAN Adapter Cards, RAID Storage Systems, Industrial Automation, Test and Measurement, and Telecommunications

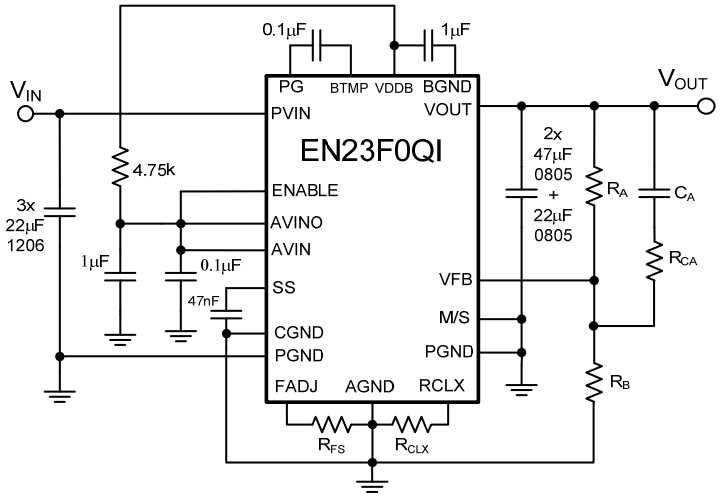

Figure 1. Simplified Applications Circuit (Footprint Optimized)

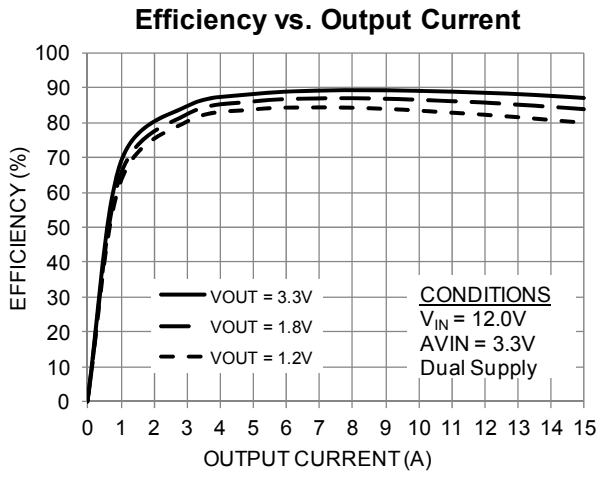

Figure 2. Highest Efficiency in Smallest Solution Size

Ordering Information

Part Number	Package Markings	Temp Rating (°C)	Package Description
EN23F0QI	EN23F0QI	-40 to +85	92-pin (12mm x 13mm x 3mm) QFN T&R
EN23F0QI-E	EN23F0QI	QFN Evaluation Board	

Packing and Marking Information: http://www.enpirion.com/resource-center-packing-and-marking-information.htm

Pin Assignments (Top View)

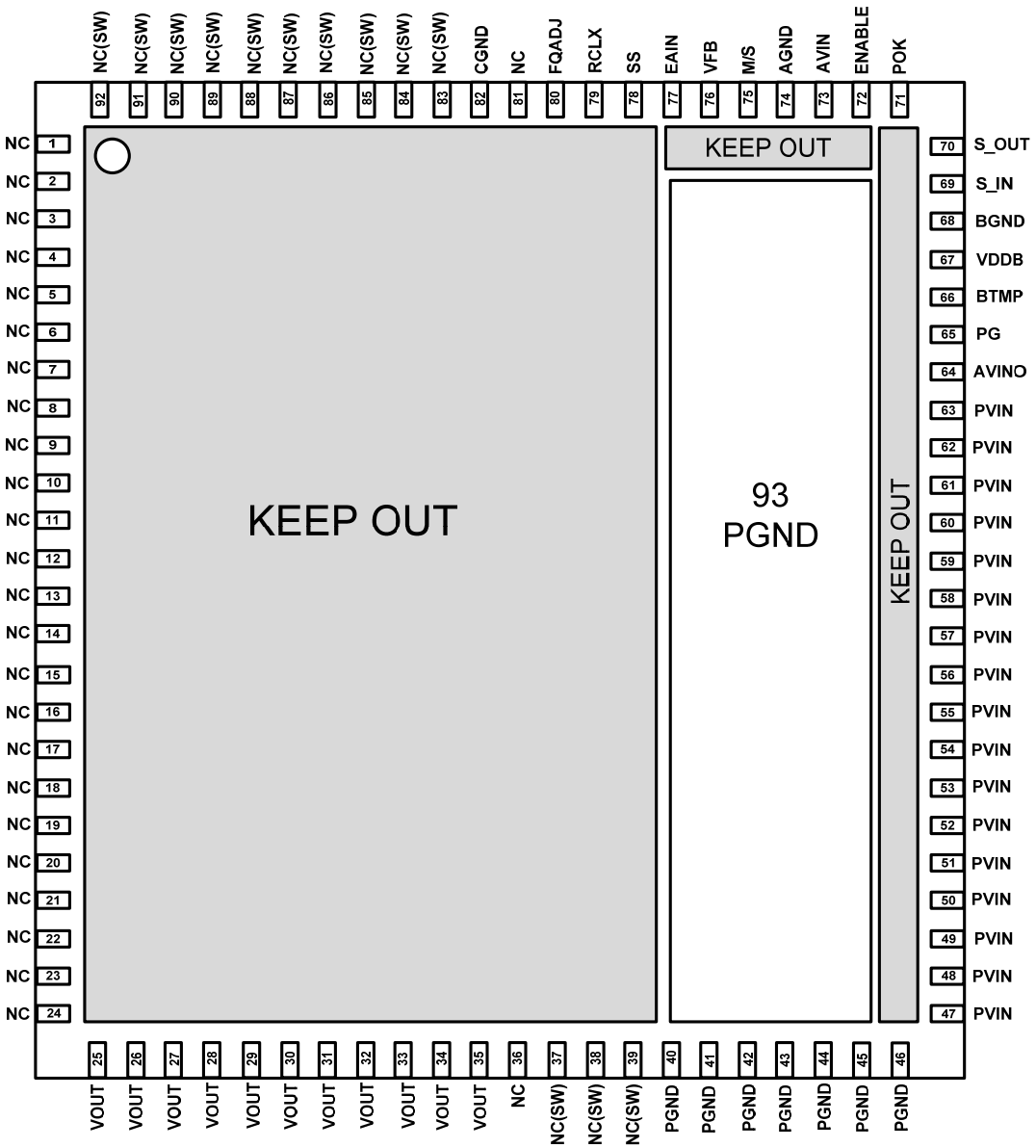

Figure 3: Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: Shaded area highlights exposed metal below the package that is not to be mechanically or electrically connected to the PCB. Refer to Figure 14 for details.

NOTE C: White 'dot' on top left is pin 1 indicator on top of the device package.

Pin Description

I/O Legend: P=Power G=Ground NC=No Connect I=Input O=Output I/O=Input/Output

PIN	NAME	I/O	FUNCTION
1-24, 36, 81	NC	NC	NO CONNECT – These pins may be internally connected. Do not connect them to each other or to any other electrical signal. Failure to follow this guideline may result in device damage.
25-35	VOUT	O	Regulated converter output. Connect these pins to the load and place output capacitor between these pins and PGND pins 40-42.
37-39, 83-92	NC(SW)	NC	NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. They are not to be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in damage to the device.
40-46	PGND	G	Input/Output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.
47-63	PVIN	P	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pins 43-46.
64	AVINO	O	Internal 3.3V linear regulator output. Connect this pin to AVIN (Pin 73) for applications where operation from a single input voltage (PVIN) is required. If AVINO is being used, place a 1µF, X5R/X7R, capacitor between AVINO and AGND as close as possible to AVINO.
65	PG	I/O	Place a 0.1µF, X7R, capacitor between this pin and BTMP.
66	BTMP	I/O	See pin 65 description.
67	VDDB	O	Internal regulated voltage used for the internal control circuitry. Place a 1µF, X7R, capacitor between this pin and BGND.
68	BGND	G	See pin 67 description.
69	S_IN	I	Digital Input. This pin accepts either an input clock to phase lock the internal switching frequency or a S_OUT signal from another EN23F0QI. Leave this pin floating if not used.
70	S_OUT	O	Digital Output. PWM signal is output on this pin. Leave this pin floating if not used.
71	POK	O	Power OK is an open drain transistor (pulled up to AVIN or similar voltage) used for power system state indication. POK is logic high when VOUT is -10% of VOUT nominal. Leave this pin floating if not used.
72	ENABLE	I	Input Enable. Applying a logic high to this pin enables the output and initiates a soft-start. Applying a logic Low disables the output. Do not leave this pin floating.
73	AVIN	P	3.3V Input power supply for the controller. Place a 0.1µF, X7R, capacitor between AVIN and AGND.
74	AGND	G	Analog Ground. This is the ground return for the controller. Needs to be connected to a quiet ground.
75	M/S	I	A logic level low configures the device as Master and a logic level high configures the device as a Slave. Connect to ground in standalone mode.
76	VFB	I/O	External Feedback Input. The feedback loop is closed through this pin. A voltage divider at VOUT is used to set the output voltage. The mid-point of the divider is connected to VFB. A phase lead capacitor from this pin to VOUT is also required to stabilize the loop.
77	EAIN	O	Optional Error Amplifier Input. Allows for customization of the control loop for performance optimization. Leave this pin floating if unused.
78	SS	I/O	Soft-Start node. The soft-start capacitor is connected between this pin and AGND. The value of this capacitor determines the startup time. See Soft-Start Operation in the Functional Description section for details.
79	RCLX	I/O	Programmable over-current protection. Placement of a resistor on this pin will adjust the over-current protection threshold. See Table 2 for the recommended RCLX Value to set OCP at the nominal value specified in the Electrical Characteristics table. No current limit protection when this pin is left floating.
80	FADJ	I/O	Adding a resistor (R_{FS}) to this pin will adjust the switching frequency of the EN23F0QI. See Table 1 for suggested resistor values on R_{FS} for various PVIN/VOUT combinations to maximize efficiency. Do not leave this pin floating.
82	CGND	G	Connect to GND plane at all times.
93	PGND	G	Not a perimeter pin. Device thermal pad to be connected to the system GND plane for heat-sinking purposes.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Voltages on : PVIN, VOUT		-0.5	15	V
Pin Voltages – AVINO, AVIN, ENABLE, POK, S_IN, S_OUT, M/S		2.5	6.0	V
Pin Voltages – VFB, SS, EAIN, RCLX, FADJ		-0.5	2.75	V
PVIN Slew Rate		0.3	3	V/ms
Storage Temperature Range	T_{STG}	-65	150	°C
Maximum Operating Junction Temperature	$T_{J\text{-}ABS\ Max}$		150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model)			2000	V
ESD Rating (based on CDM)			500	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	PVIN	4.5	14.0	V
AVIN: Controller Supply Voltage	AVIN	2.5	5.5	V
Output Voltage Range (Note 1)	V_{OUT}	0.75	3.3	V
Output Current	I_{OUT}		15	A
Operating Ambient Temperature	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Shutdown	T_{SD}	160	°C
Thermal Shutdown Hysteresis	T_{SDH}	35	°C
Thermal Resistance: Junction to Ambient (0 LFM) (Note 2)	θ_{JA}	13	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	1	°C/W

Note 1: RCLX resistor value may need to be raised for $V_{OUT} > V_{IN} – 2.5V$ to increase current limit threshold. Contact techsupport@enpirion.com for details.

Note 2: Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

Electrical Characteristics

NOTE: V_{IN}=12V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	PVIN		4.5		14.0	V
Controller Input Voltage	AVIN		2.5		5.5	V
PVIN Under Voltage Lock-out	$UVLO_{PVIN}$	Voltage above which UVLO is not asserted		2		V
AVIN Under Voltage Lock-out rising	$AVIN_{UVLOR}$	Voltage above which UVLO is not asserted		2.3		V
AVIN Under Voltage Lock-out falling	$AVIN_{OVLOF}$	Voltage below which UVLO is asserted		2.1		V
AVIN Pin Input Current	I_{AVIN}			14		mA
Internal Linear Regulator Output Voltage	AVINO			3.3		V
Shut-Down Supply Current	$IPVIN_S$	PVIN=12V, AVIN=3.3, ENABLE=0V		300		µA
	$IAVIN_S$	PVIN=12V, AVIN=3.3, ENABLE=0V		50		µA
Feedback Pin Voltage	V_{FB}	Feedback Node Voltage at: V_{IN} = 12V, ILOAD = 0, T_A = 25°C	0.594	0.60	0.606	V
Feedback Pin Voltage	V_{FB}	Feedback Node Voltage at: 4.5V ≤ V_{IN} ≤ 14V 0A ≤ I_{LOAD} ≤ 15A, T_A = -40 to 85°C	0.588	0.60	0.612	V
Feedback pin Input Leakage Current	I_{FB}	VFB pin input leakage current (Note 3)	-5		5	nA
V_{OUT} Rise Time	t_{RISE}	C_{SS} = 47nF (Note 3, Note 4 and Note 5)	1.96	2.8	3.64	ms
Soft Start Capacitor Range	C_{SS_RANGE}			47		nF
Continuous Output Current	I_{OUT_CONT}		0		15	A
Over Current Trip Level	I_{OCP}	Reference Table 3		22.5		A
ENABLE Logic High	V_{ENABLE_HIGH}	4.5V ≤ V_{IN} ≤ 14V;	1.8		AV_{IN}	V
ENABLE Logic Low	V_{ENABLE_LOW}	4.5V ≤ V_{IN} ≤ 14V;	0		0.6	V
ENABLE Lockout Time	$T_{ENLOCKOUT}$			8		ms
ENABLE pin Input Current	I_{ENABLE}	180kΩ Pull Down (Note 3)		4		µA
Switching Frequency	F_{SW}	RFADJ =3kΩ		1.0		MHz
External SYNC Clock Frequency Lock Range	F_{PLL_LOCK}	Range of SYNC clock frequency	0.8		1.6	MHz
S_IN Threshold – Low	$V_{S_IN_LO}$	S_IN Clock Logic Low Level			0.8	V
S_IN Threshold – High	$V_{S_IN_HI}$	S_IN Clock Logic High Level	1.8		2.5	V
S_OUT Threshold – Low	$V_{S_OUT_LO}$	S_OUT Clock Logic Low Level			0.8	V
S_OUT Threshold – High	$V_{S_OUT_HI}$	S_OUT Clock Logic High Level	1.8		2.5	V
POK Lower Threshold	POK_{LT}	Percentage of Nominal Output Voltage for POK to be Low		90		%

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POK Output low Voltage	V_{POKL}	With 4mA Current Sink into POK			0.4	V
POK Output Hi Voltage	V_{POKH}	PVIN range: 4.5V ≤ V_{IN} ≤ 15V			AVIN	V
POK pin V_{OH} leakage current	I_{POKL}	POK High (Note 3)			1	µA
M/S Pin Logic Low	V_{T-LOW}	Tie Pin to GND			0.8V	V
M/S Pin Logic High	V_{T-HIGH}	Pull up to AVIN Through an External Resistor REXT	1.8V			V
M/S Pin Input Current	$I_{M/S}$	VIN = 5.0V, REXT = 24.9kΩ		100		µA

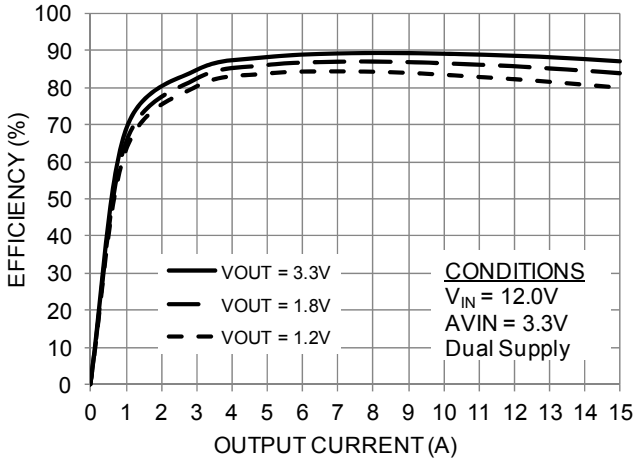
Note 3: Parameter not production tested but is guaranteed by design.

Note 4: Rise time calculation begins when AVIN > V_{UVLO} and ENABLE = HIGH.

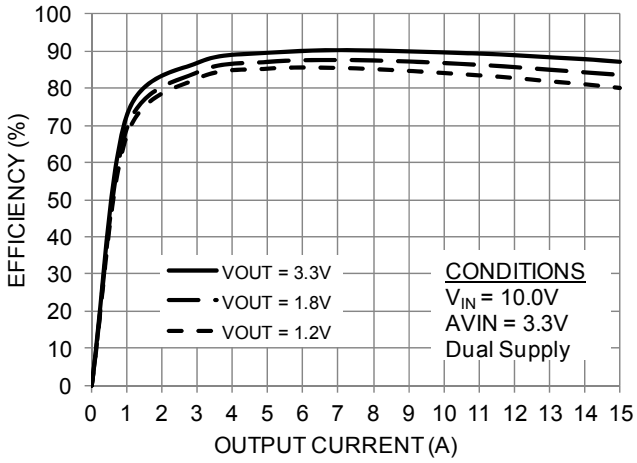
Note 5: V_{OUT} Rise Time Accuracy does not include soft-start capacitor tolerance.

Typical Performance Curves

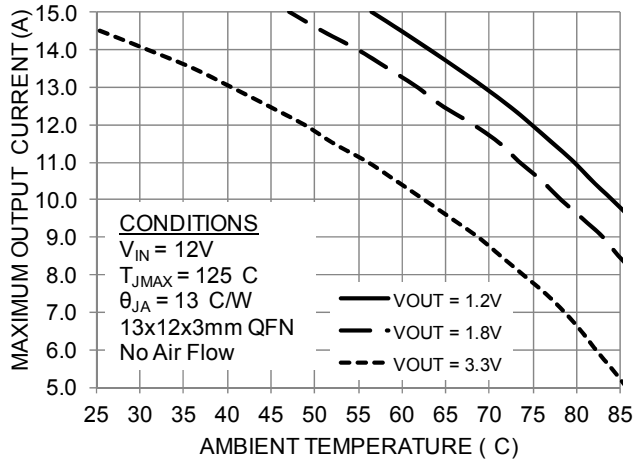
Efficiency vs. Output Current



Efficiency vs. Output Current



Output Current De-rating



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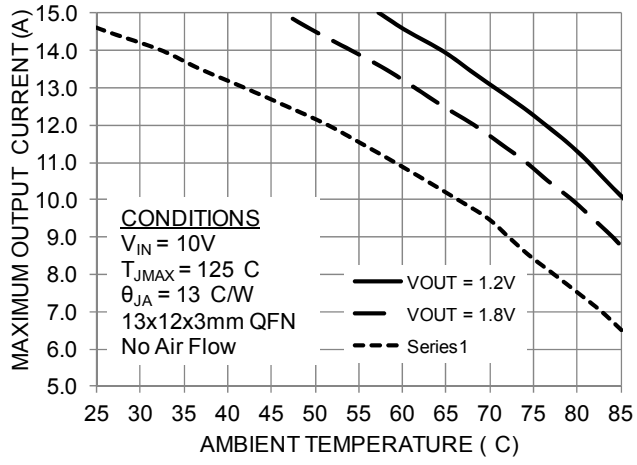
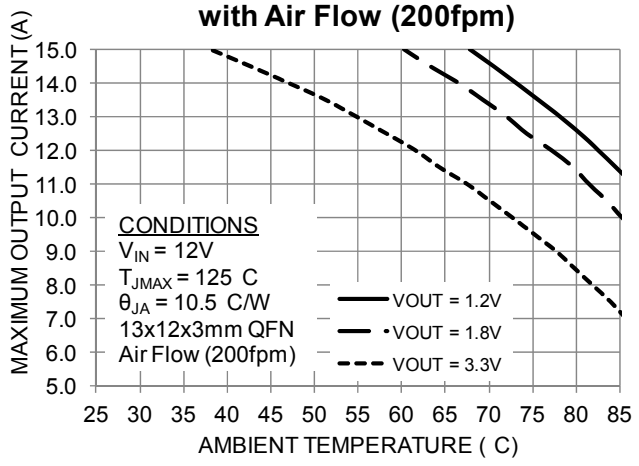
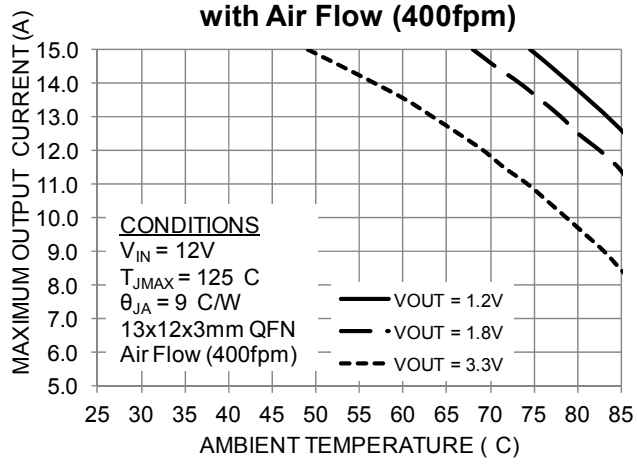


Output Current De-rating with Air Flow (200fpm)



Output Current De-rating with Air Flow (400fpm)



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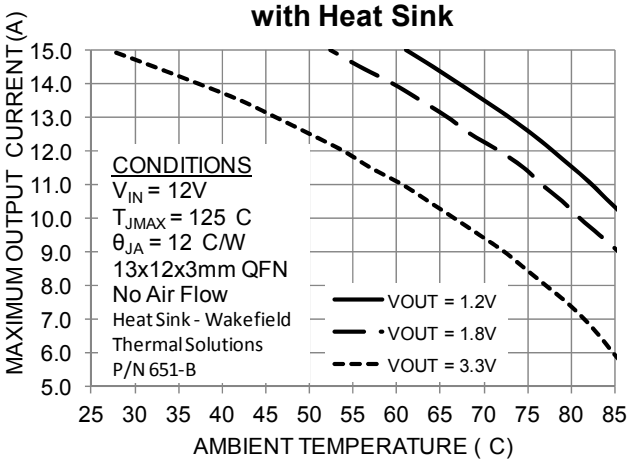
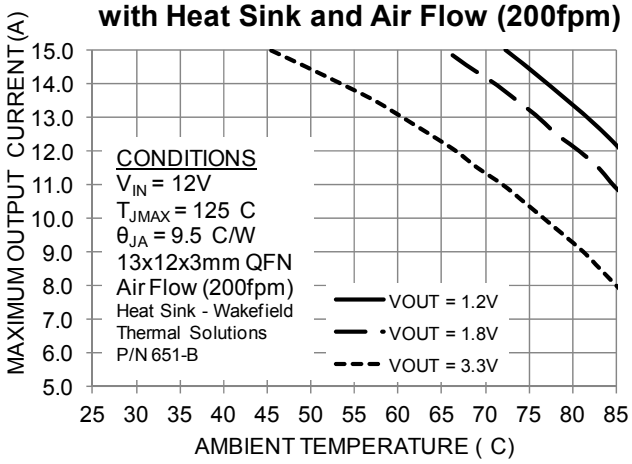
Typical Performance Curves

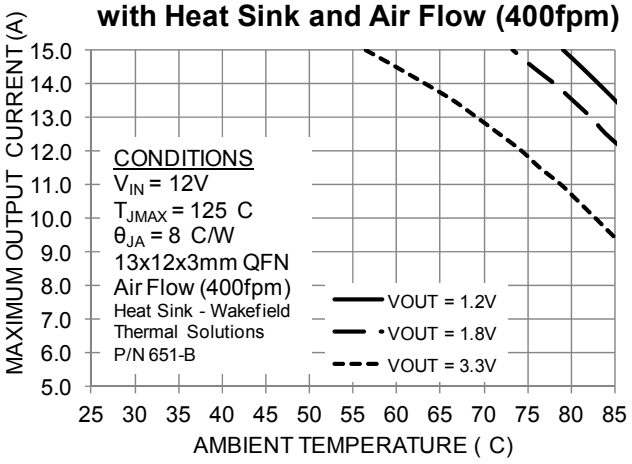
Output Current De-rating with Heat Sink



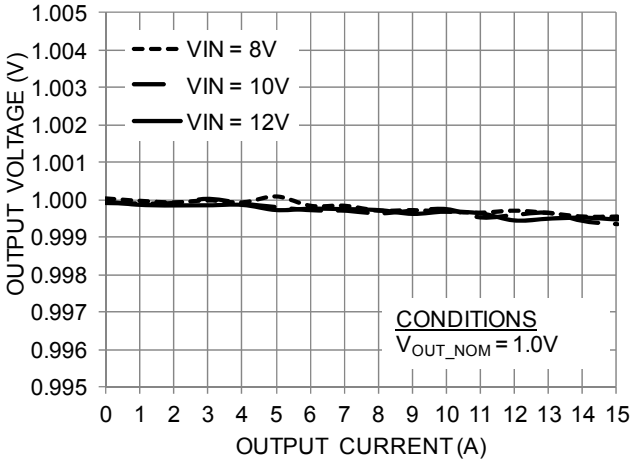
Output Current De-rating with Heat Sink and Air Flow (200fpm)



Output Current De-rating with Heat Sink and Air Flow (400fpm)



Output Voltage vs. Output Current



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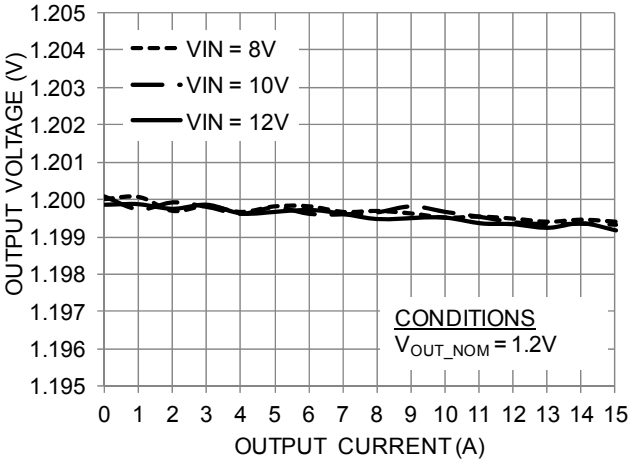
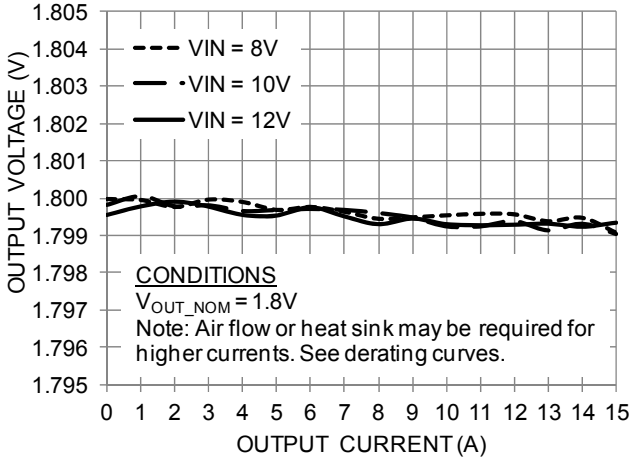
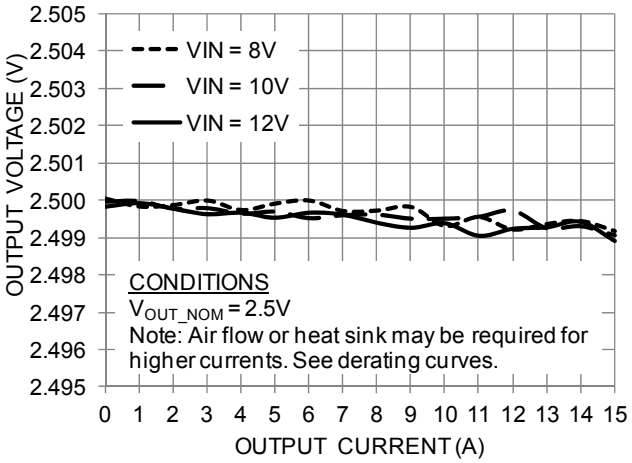


Output Voltage vs. Output Current

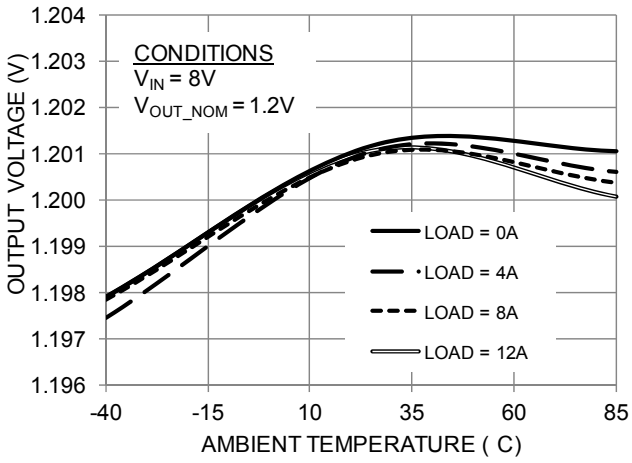


Typical Performance Curves

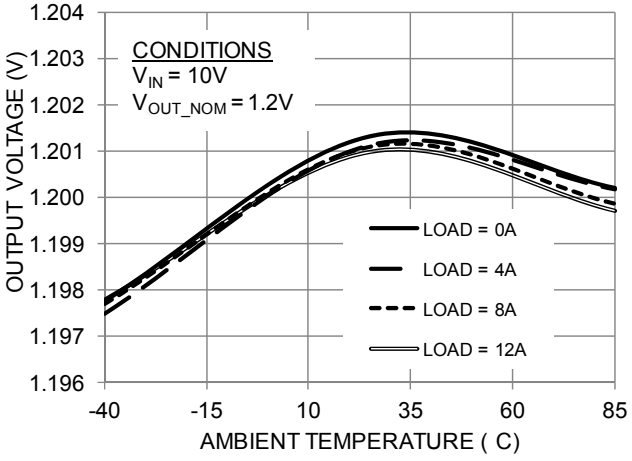
Output Voltage vs. Output Current



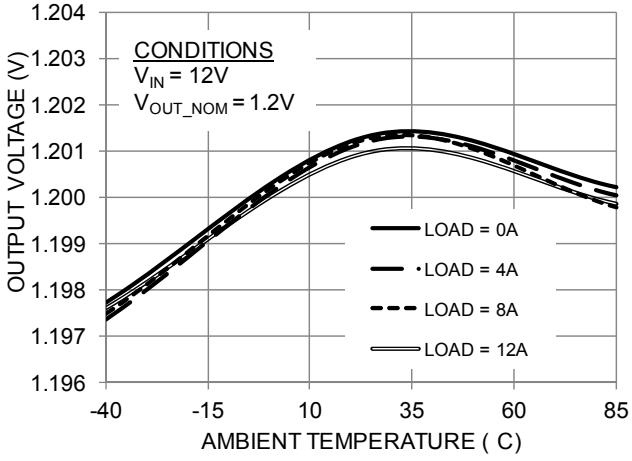
Output Voltage vs. Temperature



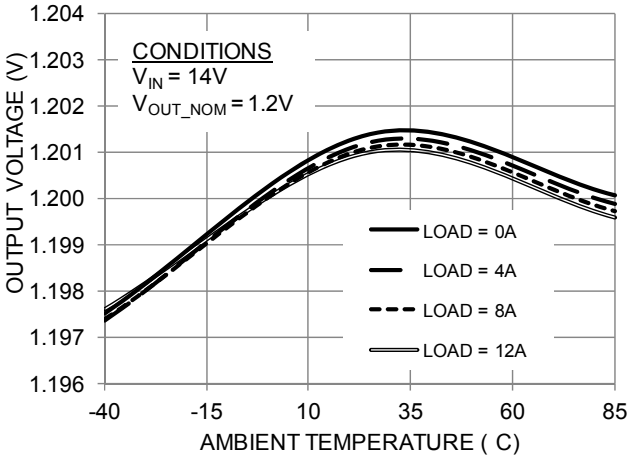
Output Voltage vs. Temperature



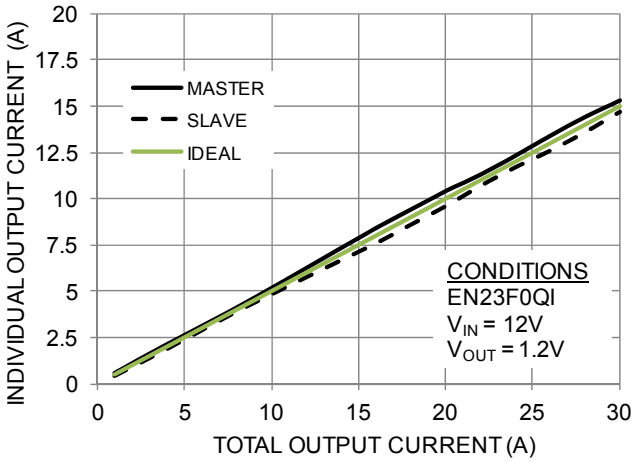
Output Voltage vs. Temperature



Output Voltage vs. Temperature

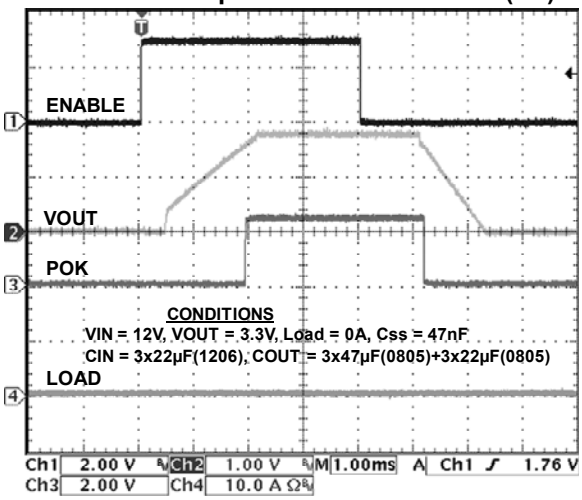


Parallel Current Share Breakdown

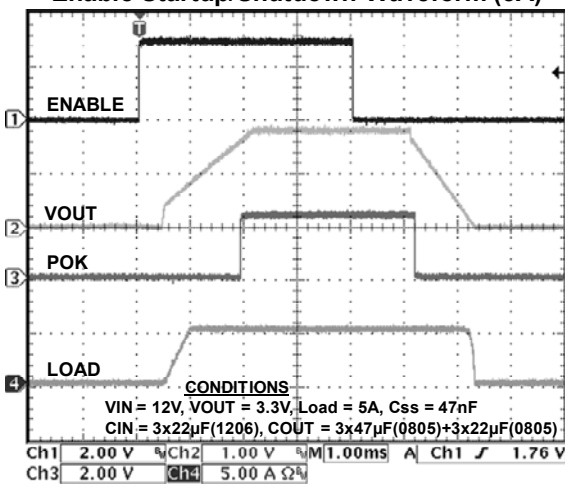


Typical Performance Characteristics

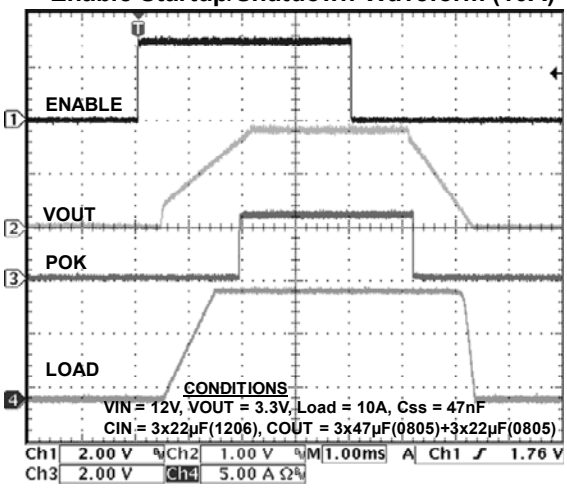
Enable Startup/Shutdown Waveform (0A)



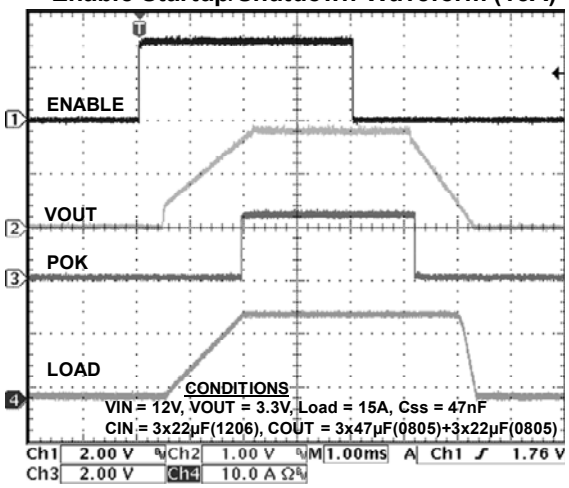
Enable Startup/Shutdown Waveform (5A)



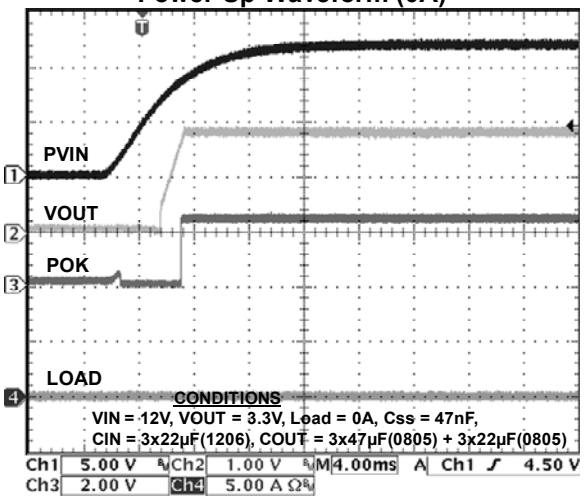
Enable Startup/Shutdown Waveform (10A)



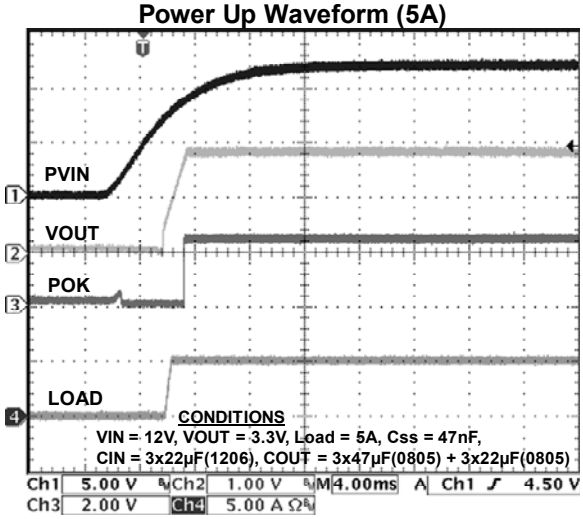
Enable Startup/Shutdown Waveform (15A)



Power Up Waveform (0A)



Power Up Waveform (5A)



Typical Performance Characteristics

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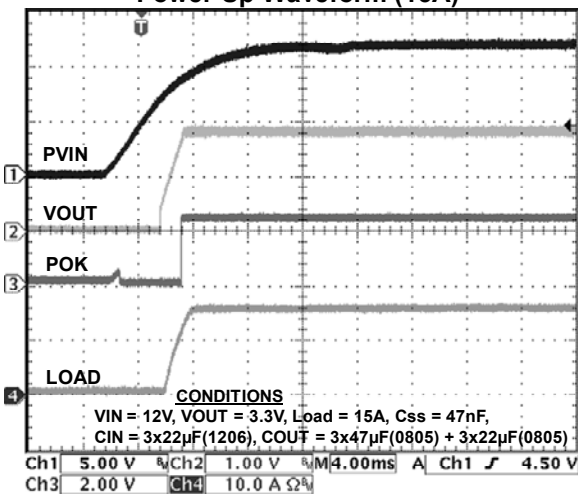
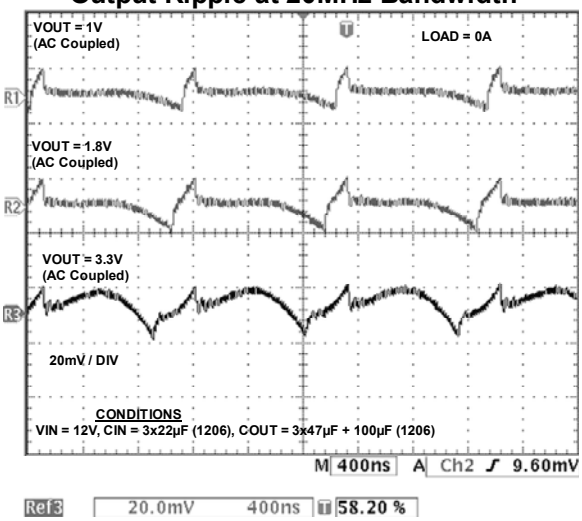
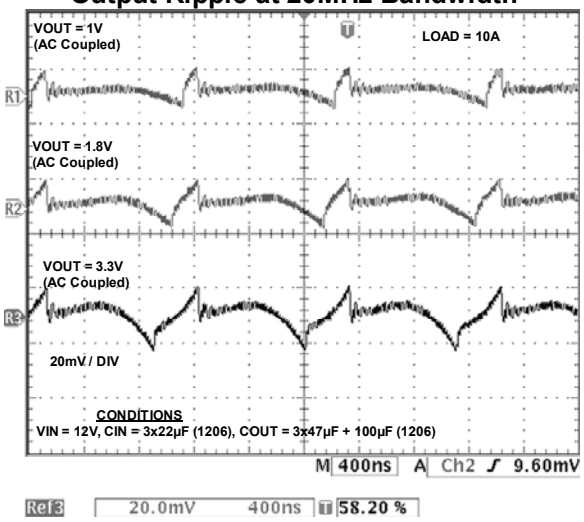


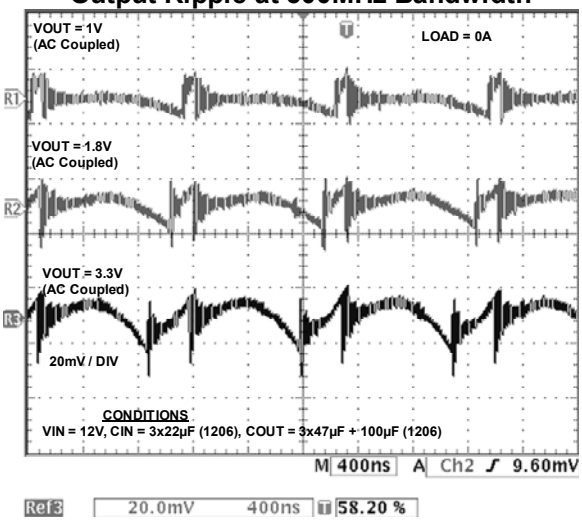
Output Ripple at 20MHz Bandwidth



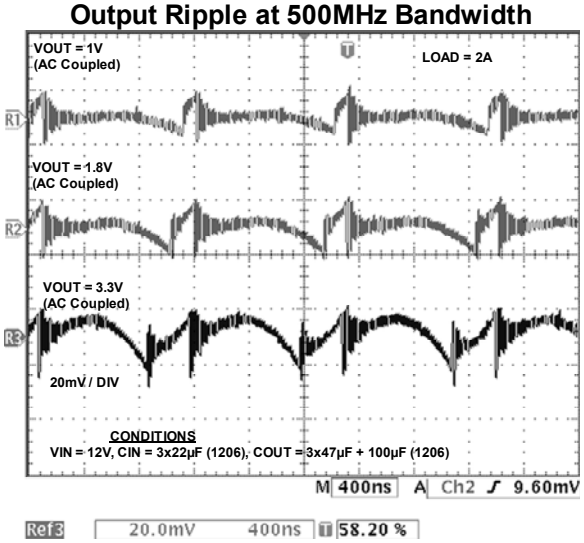
Output Ripple at 20MHz Bandwidth



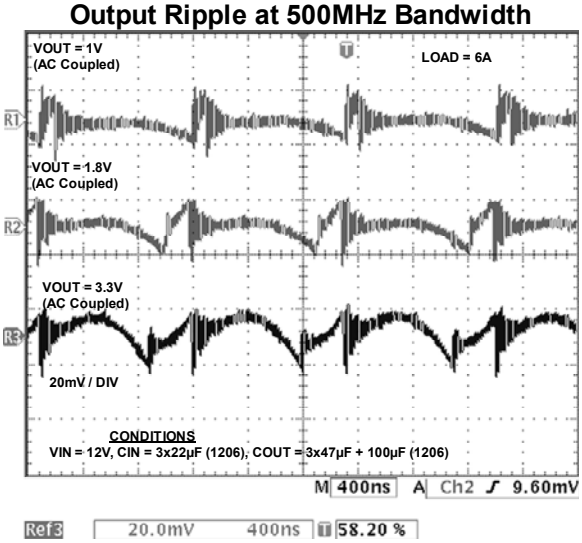
Output Ripple at 500MHz Bandwidth



Output Ripple at 500MHz Bandwidth

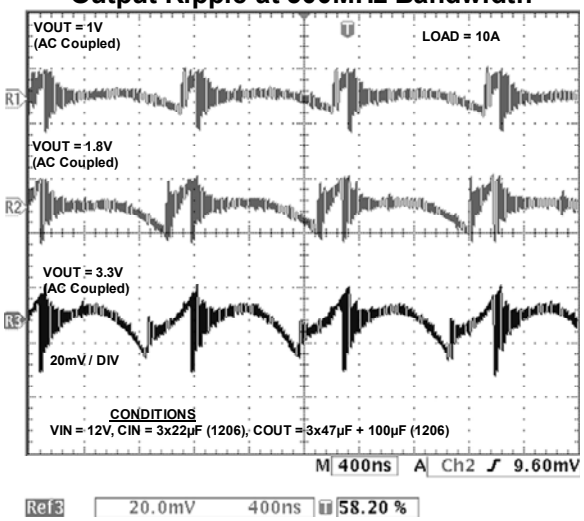


Output Ripple at 500MHz Bandwidth

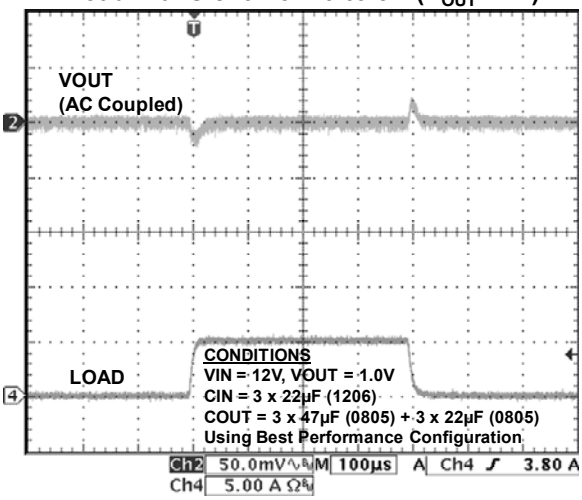


Typical Performance Characteristics

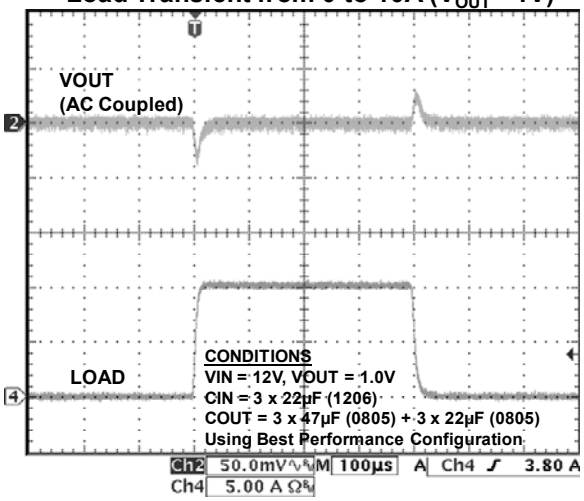
Output Ripple at 500MHz Bandwidth



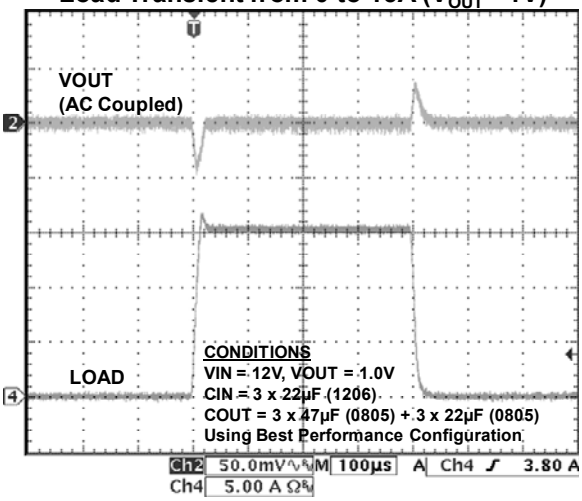
Load Transient from 0 to 5A (V_{OUT} =1V)



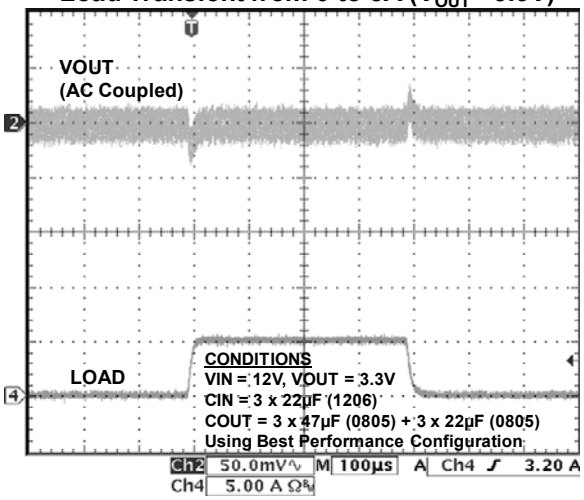
Load Transient from 0 to 10A (V_{OUT} =1V)



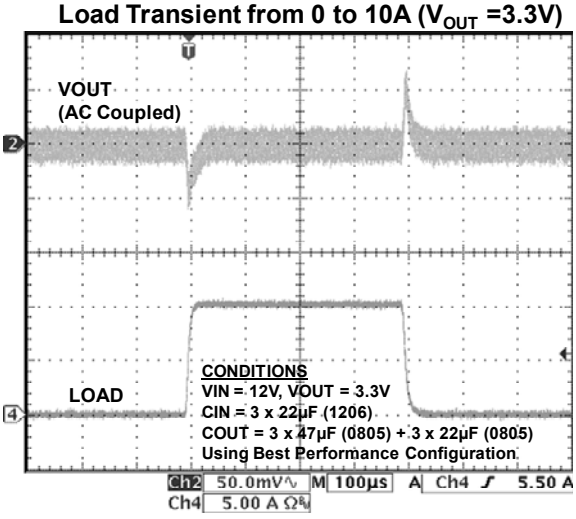
Load Transient from 0 to 15A (V_{OUT} =1V)



Load Transient from 0 to 5A (V_{OUT} =3.3V)

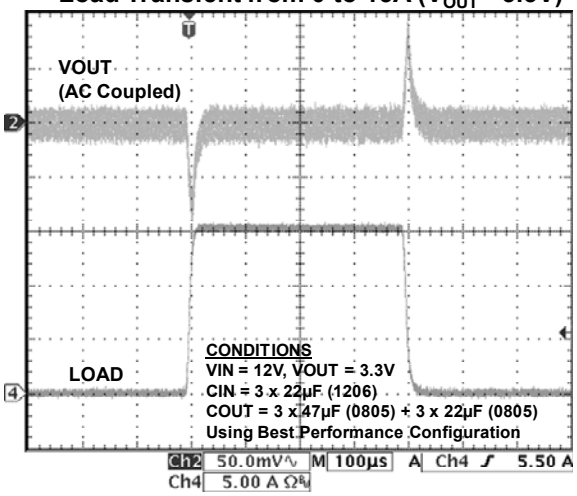


Load Transient from 0 to 10A (V_{OUT} =3.3V)

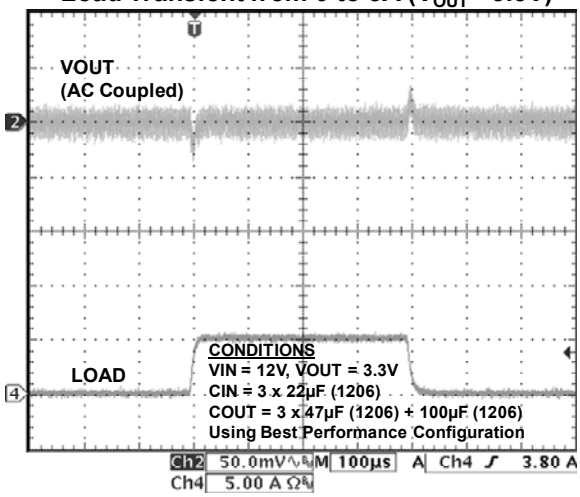


Typical Performance Characteristics

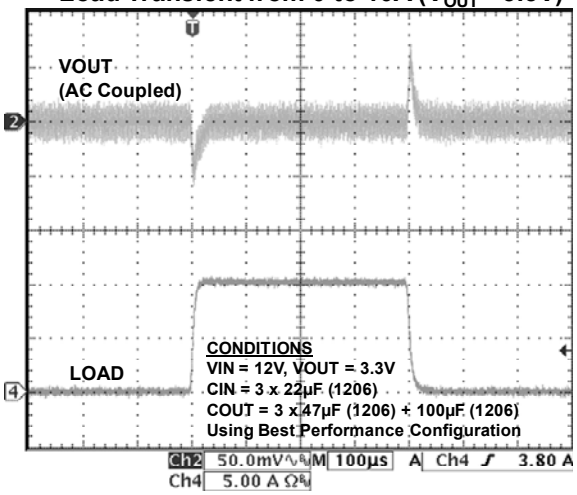
Load Transient from 0 to 15A (V_{OUT} =3.3V)



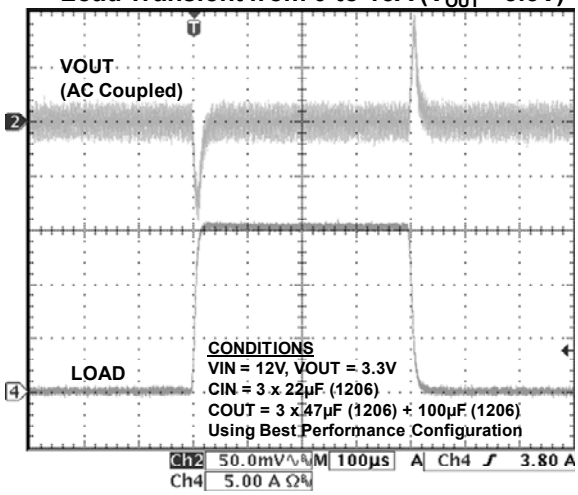
Load Transient from 0 to 5A (V_{OUT} =3.3V)



Load Transient from 0 to 10A (V_{OUT} =3.3V)



Load Transient from 0 to 15A (V_{OUT} =3.3V)



Functional Block Diagram

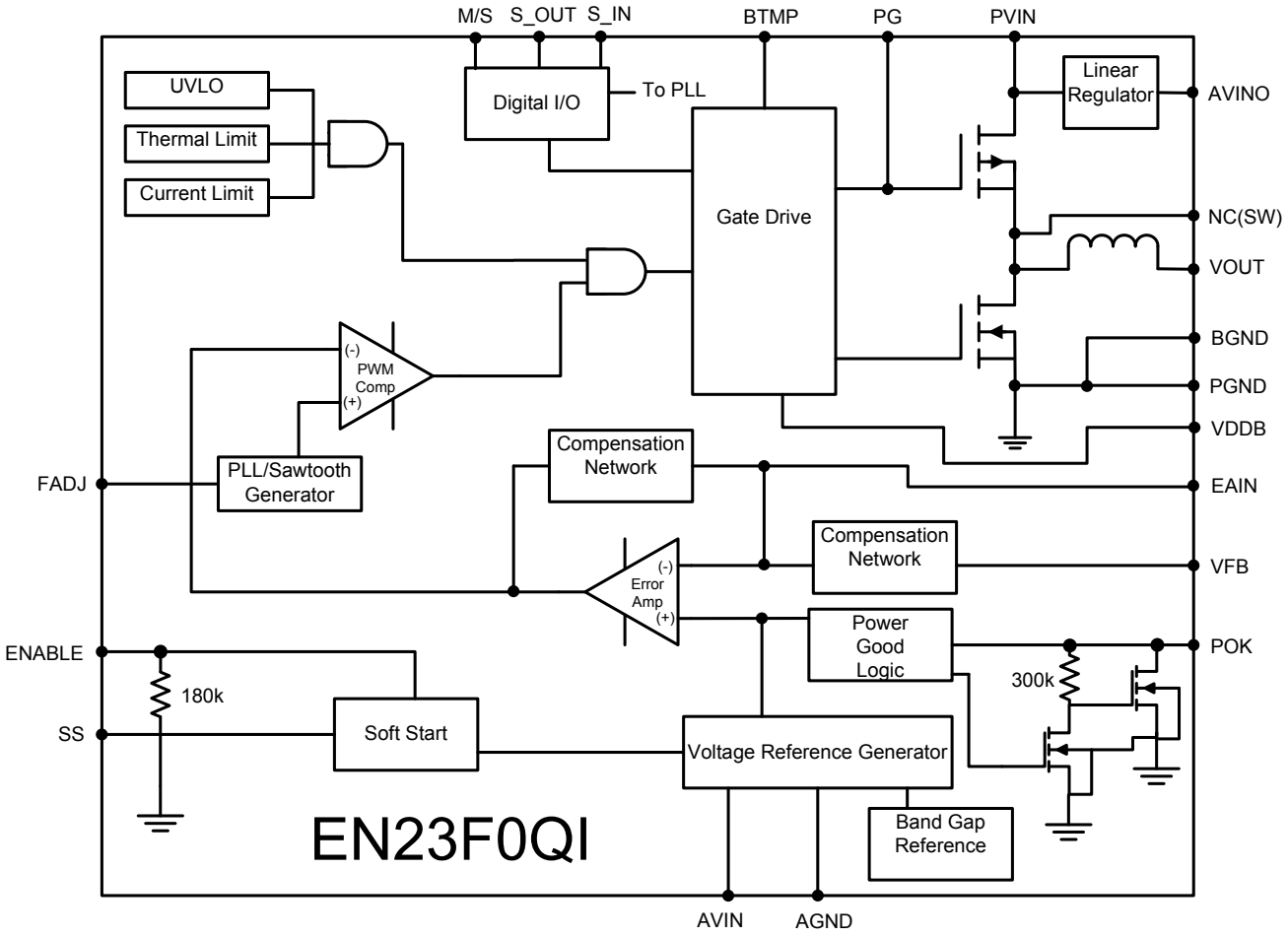


Figure 4: Functional Block Diagram

Functional Description

Synchronous Buck Converter

The EN23F0QI is a highly integrated synchronous, buck converter with integrated controller, power MOSFET switches and integrated inductor. The nominal input voltage (PVIN) range is 4.5V to 14V and can support up to 15A of continuous output current. The output voltage is programmed using an external resistor divider network. The control loop utilizes a Type IV Voltage-Mode compensation network and maximizes on a low-noise PWM topology. Much of the compensation circuitry is internal to the device. However, a phase lead capacitor is required along with the output voltage feedback resistor divider to complete the Type IV compensation network.. The high switching frequency of the EN23F0QI enables the use of small size input and output capacitors, as well as a wide loop bandwidth within a small foot print.

Protection Features:

The power supply has the following protection features:

- Programmable Over-Current Protection
- Thermal Shutdown with Hysteresis
- Under-Voltage Lockout Protection

Additional Features:

- Switching Frequency Synchronization
- Programmable Soft-Start
- Power OK Output Monitoring

Power Up Sequence

The EN23F0QI is designed to be powered by either a single input supply (PVIN) or two separate

supplies: one for PVIN and the other for AVIN.

Single Input Supply Application (PVIN):

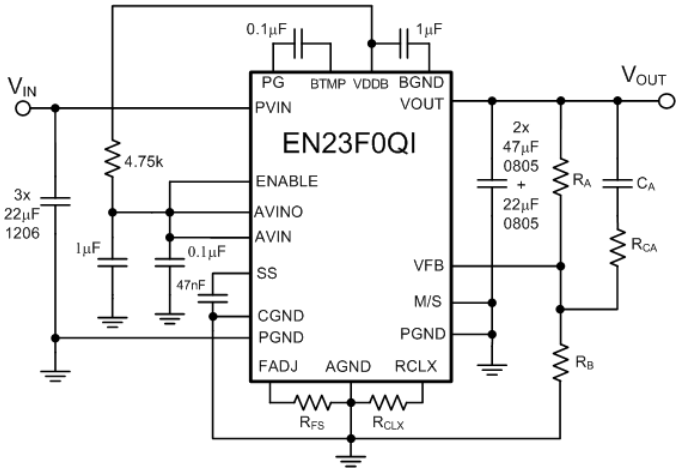


Figure 5. Single Supply Applications Circuit

The EN23F0QI has an internal linear regulator that converts PVIN to 3.3V. The output of the linear regulator is provided on the AVINO pin once the device is enabled. AVINO should be connected to AVIN on the EN23F0QI. In this application, the following external components are required: Place a 1µF, X5R/X7R, capacitor between AVINO and AGND as close as possible to AVINO. Place a 0.1µF, X5R/X7R, capacitor between AVIN and AGND as close as possible to AVIN. In addition, place a resistor (R_{VB}) between VDDB and AVIN, as shown in Figure 5. Enpirion recommends R_{VB}=4.75kΩ. In this application, ENABLE cannot be asserted before PVIN. If no external enable signal is used, tying ENABLE to AVIN meets this requirement.

Dual Input Supply Application (PVIN and AVIN):

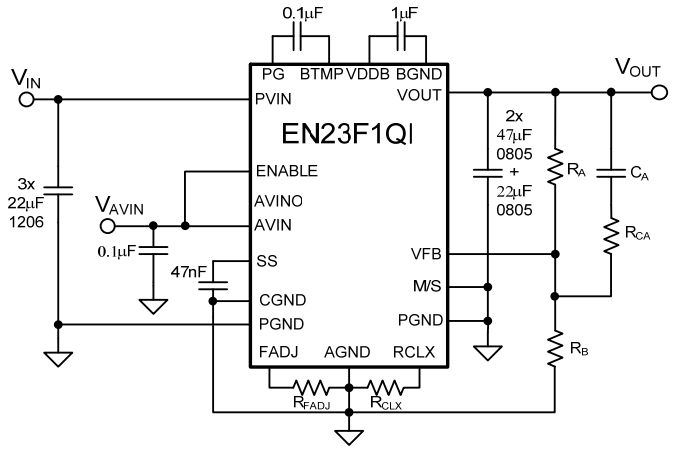


Figure 6: Dual Input Supply Application Circuit

In this application, place a 0.1µF, X7R, capacitor between AVIN and AGND as close as possible to AVIN. Refer to Figure 6 for a recommended schematic for a dual input supply application.

For dual input supply applications, the sequencing of the two input supplies, PVIN and AVIN, is very important. During power up, neither ENABLE nor PVIN should be asserted before AVIN. There are two common acceptable turn-on/off sequences for the device. ENABLE can be tied to AVIN and come up with it, and PVIN can be ramped up and down as needed. Alternatively, PVIN can be brought high after AVIN is asserted, and the device can be turned on and off by toggling the ENABLE pin. PVIN may be applied before AVIN if ENABLE is toggled after both PVIN and AVIN is applied.

Enable Operation

The ENABLE pin provides a means to enable normal operation or to shut down the device. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted (high) the device will undergo a normal soft-start, allowing the output voltage to rise monotonically into regulation. A logic low will disable the converter and the device will power down in a controlled manner. The ENABLE signal has to be low for at least the ENABLE Lockout Time (8ms) in order for the device to be re-enabled.

Pre-Bias Precaution

The EN23F0QI is not designed to be turned on into a pre-biased output voltage. Be sure the output capacitors are not charged or the output of the EN23F0QI is not pre-biased when the EN23F0QI is first enabled.

Frequency Synchronization

The switching frequency of the EN23F0QI can be phase-locked to an external clock source to move unwanted beat frequencies out of band. The internal switching clock of the EN23F0QI can be phase locked to a clock signal applied to the S_IN pin. An activity detector recognizes the presence of an external clock signal and automatically phase-locks the internal oscillator to this external clock. Phase-lock will occur as long as the input clock frequency is in the range of 0.8MHz to 1.6MHz. When no clock is present, the device reverts to the free running frequency of the internal oscillator. Adding a resistor (R_{FS}) to the FADJ pin will adjust the switching frequency. If a 3KΩ resistor is placed on FADJ the nominal switching frequency of the EN23F0QI is 1MHz. Figure 7 shows the typical R_{FS} resistor value versus switching frequency.

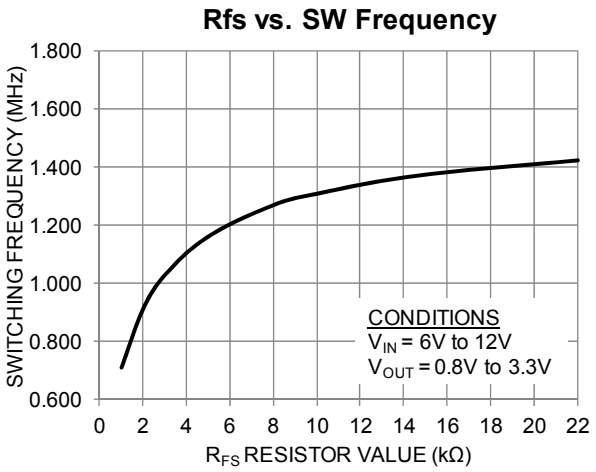


Figure 7. R_{FS} versus Switching Frequency

The efficiency performance of the EN23F0QI for various VOUTs can be optimized by adjusting the switching frequency. Table 1 shows recommended R_{FS} values for various VOUTs in order to optimize performance of the EN23F0QI.

PVIN	VOUT	R_{FS}
12V	1.0V	3k
	1.2V	3.3k
	1.8V	4.87k
	2.5V	10k
	3.3V	15k

Table 1: Recommended R_{FS} Values

Spread Spectrum Mode

The external clock frequency may be swept between 0.8MHz and 1.6MHz at repetition rates of up to 10 kHz in order to reduce EMI frequency components.

Soft-Start Operation

Soft start is a means to ramp the output voltage gradually upon start-up. The output voltage rise time is controlled by the choice of soft-start capacitor, which is placed between the SS pin (pin 78) and the AGND pin (pin 74).

Rise Time (ms): $T_R \approx C_{ss}$ [nF] x 0.06

During start-up of the converter, the reference voltage to the error amplifier is linearly increased to its final level by an internal current source of approximately 10µA. Typical soft-start rise time is ~2.8ms with SS capacitor value of 47nF. The rise time is measured from when $V_{IN} > V_{UVLOR}$ and ENABLE pin voltage crosses its logic high threshold to when V_{OUT} reaches its programmed value.

POK Operation

The POK signal is an open drain signal (requires a pull up resistor to AVIN or similar voltage) from the converter indicating the output voltage is within the specified range. Typically, a 100kΩ or lower resistance is used as the pull-up resistor. The POK signal will be logic high (AVIN) when the output voltage is above 90% of the programmed voltage level. If the output voltage is below this point, the POK signal will be a logic low. The POK signal can be used to sequence down-stream converters by tying to their enable pins.

Over-Current Protection (OCP)

The current limit function is achieved by sensing the current flowing through a sense PFET. When the sensed current exceeds the current limit, both power FETs are turned off for the rest of the switching cycle. If the over-current condition is removed, the over-current protection circuit will re-enable PWM operation. If the over-current condition persists, the circuit will continue to protect the load.
The OCP trip point is nominally set as specified in the Electrical Characteristics table. In the event the OCP circuit trips consistently in normal operation, the device enters a hiccup mode. While in hiccup mode, the device is disabled for a short while and restarted with a normal soft-start. The hiccup time is approximately 32ms. This cycle can continue indefinitely as long as the over current condition persists.
The OCP trip point can be programmed to trip at a lower level via the RCLX pin. The value of the resistor connected between RCLX and ground will determine the OCP trip point. Generally, the higher the RCLX value, the higher the current limit threshold. Note that if RCLX pin is left open the output current will be unlimited and the device will not have current limit protection. Reference Table 2 for a list of recommended resistor values on RCLX that will set the OCP trip point at the typical value of 22.5A, also specified in the Electrical Characteristics table.

V_{OUT} Range	R_{CLX} Value
$0.6V < V_{OUT} \leq 0.9V$	36.5k
$0.9V < V_{OUT} \leq 1.2V$	38.4k
$1.2V < V_{OUT} \leq 2.0V$	40.2k
$2.0V < V_{OUT} \leq 5.0V$	45.3k

Table 2: Recommended R_{CLX} Values vs. V_{OUT}

Thermal Overload Protection

Thermal shutdown circuit will disable device operation when the junction temperature exceeds approximately 150ºC. After a thermal shutdown event, when the junction temperature drops by approx 20ºC, the converter will re-start with a normal soft-start.

Input Under-Voltage Lock-Out (UVLO)

Internal circuits ensure that the converter will not start switching until the input voltage is above the specified minimum voltage. Hysteresis, input de-glitch and output leading edge blanking ensures high noise immunity and prevents false UVLO triggers.

Master / Slave (Parallel) Operation:

Up to four EN23F0QI devices may be connected in a Master/Slave configuration to handle larger load currents. The maximum output current for each parallel device will need to be de-rated by 20 percent so that no devices will over current due to current mis-match. The Master device's switching clock may be phase-locked to an external clock source via the S_IN pin or left open and use its default switching frequency. The device is placed in Master mode by pulling the M/S pin low or in Slave mode by pulling M/S pin high. Note that the M/S pin is also pulled low for standalone mode. In Master mode, the internal PWM signal is output on the S_OUT pin. This PWM signal from the Master is fed to the Slave device at its S_IN input. The Slave device acts like an extension of the power FETs in the Master. The inductor in the Slave prevents crow-bar currents from Master to Slave due to timing delays. Parallel operation in dual supply mode is shown in Figure 9. Single supply mode operation may also be implemented similarly. Note that only critical components are shown. The red text and red lines indicate the important parallel operation connections and care should be taken in layout to ensure low impedance between those paths. The parallel current matching is illustrated in Figure 8.

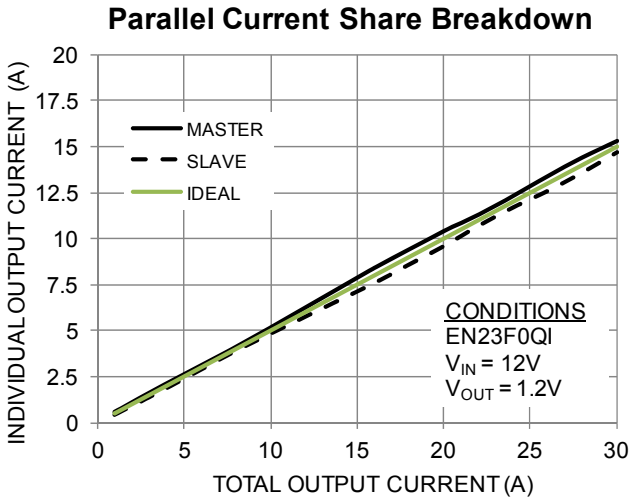


Figure 8. Parallel Current Matching

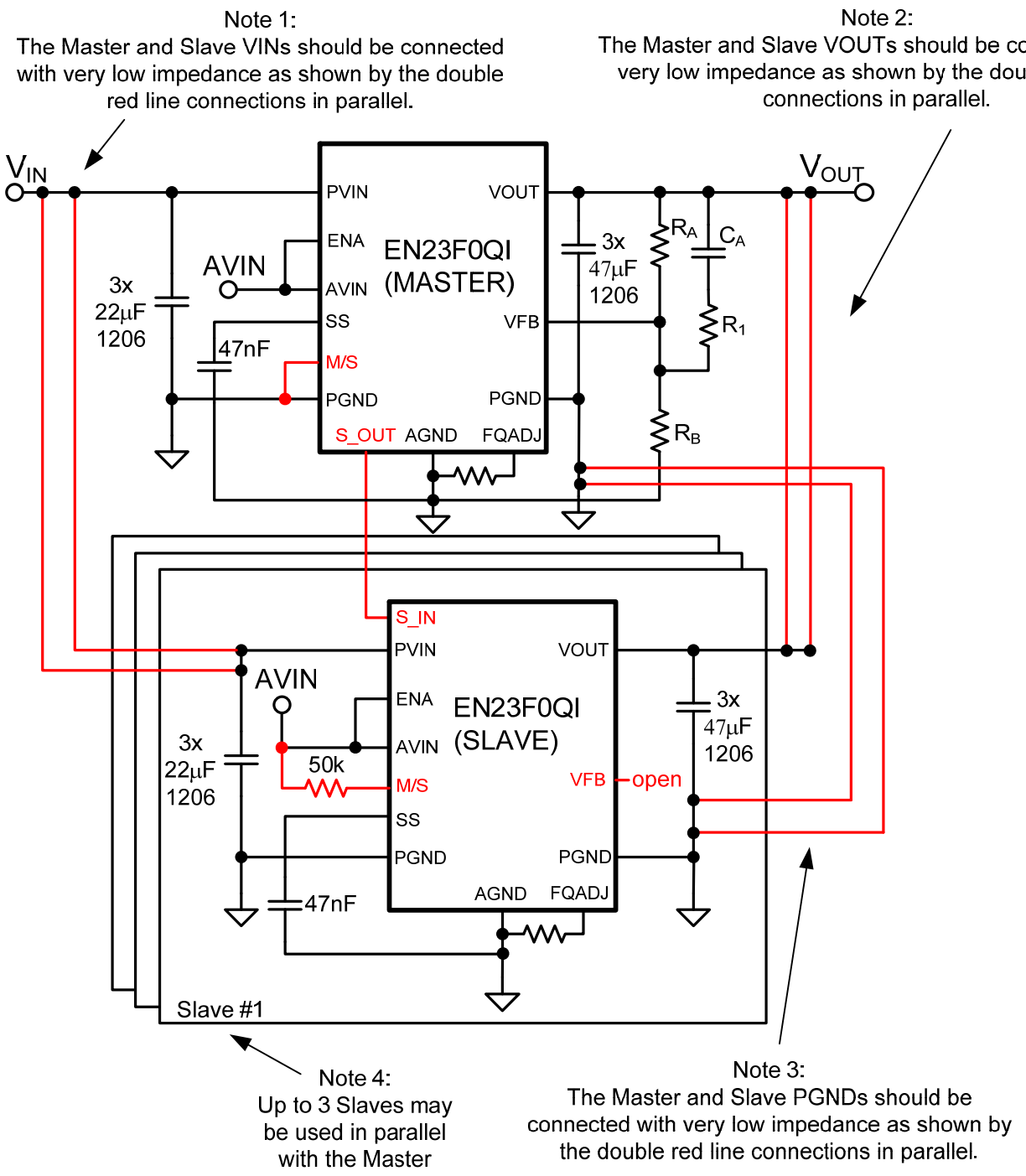


Figure 9. Parallel Operation Illustration

Application Information

Output Voltage Programming and Loop Compensation

The EN23F0QI uses a Type IV Voltage Mode compensation network. Type IV Voltage Mode control is a proprietary Enpirion control scheme that maximizes control loop bandwidth to deliver excellent load transient responses and maintain output regulation with pin point accuracy. For ease of use, most of this network has been customized and is integrated within the device package. The EN23F0QI output voltage is programmed using a simple resistor divider network (R_A and R_B). The feedback voltage at VFB is nominally 0.6V. R_A is predetermined based on Table 5 and R_B can be calculated based on Figure 10. The values recommended for C_{OUT}, C_A, R_{CA} and R_{EA} make up the external compensation of the EN23F0QI. It will vary with each PVIN and VOUT combination to optimize on performance. The EN23F0QI solution can be optimized for either smallest size or highest performance. Please see Table 5 for a list of recommended R_A, C_A, R_{CA}, R_{EA} and C_{OUT} values for each solution.

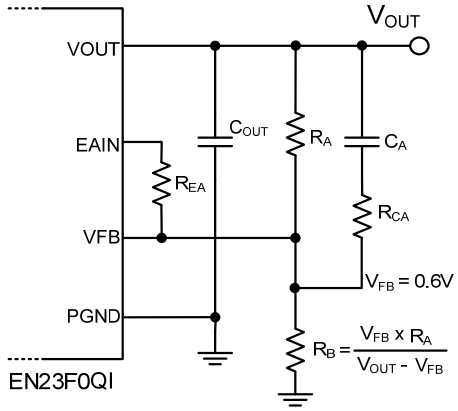


Figure 10: V_{OUT} Resistor Divider & Compensation Components. See Table 5 for details.

Input Capacitor Selection

The EN23F0QI requires three 22µF/1206 input capacitor. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this converter. The dielectric must be X5R or X7R rated. **Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.** In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling. Table 3 contains a list of recommended input capacitors.

Recommended Input Capacitors

Description	MFG	P/N
22µF, 16V, X5R, 10%, 1206	Murata	GRM31CR61C226ME15
22µF, 16V, X5R, 20%, 1206	Taiyo Yuden	EMK316ABJ226ML-T
22µF, 25V, X5R, 10%, 1210	Murata	GRM32ER61E226KE15L
22µF, 25V, X5R, 20%, 1210	Taiyo Yuden	TMK325BJ226MM-T

Table 3: Recommended Input Capacitors

Output Capacitor Selection

As seen from Table 5, the EN23F0QI has been optimized for use with three 47µF/1206 plus one 100µF/1206 for best performance. For smallest solution size, various combinations of output capacitance may be used. See Table 5 for details. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. **Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.** Table 4 contains a list of recommended output capacitors.

Output ripple voltage is determined by the aggregate output capacitor impedance. Capacitor impedance, denoted as Z, is comprised of capacitive reactance, effective series resistance, ESR, and effective series inductance, ESL reactance.

Placing output capacitors in parallel reduces the impedance and will hence result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

Recommended Output Capacitors

Description	MFG	P/N
47µF, 6.3V, X5R, 20%, 1206	Murata	GRM31CR60J476ME19L
47µF, 10V, X5R, 20%, 1206	Taiyo Yuden	LMK316BJ476ML-T
22µF, 10V, X5R, 20%, 0805	Panasonic	ECJ-2FB1A226M
22µF, 10V, X5R, 20%, 0805	Taiyo Yuden	LMK212BJ226MG-T
100µF, 6.3V, X5R, 20%, 1206	Murata	GRM31CR60J107ME39L
	Taiyo Yuden	JMK316BJ107ML-T

Table 4: Recommended Output Capacitors

Best Performance						
C_{IN} = 3 x 22µF/1206						
C_{OUT} = 3x47µF (1206) + 100µF(1206)						
R_A = 200 kΩ						
PVIN (V)	VOUT (V)	C_A (pF)	R_{CA} (kΩ)	R_{EA} (kΩ)	Ripple (mV)	Deviation (mV)
14V	1.0V	15	19	0	25.6	23
	1.2V	12	22	0	24	35
	1.5V	12	22	0	26.4	42
	1.8V	10	24	0	28.4	45
	2.5V	18	14	56	31.6	78
	3.3V	12	14	56	37.3	114
12V	1.0V	18	16	0	21.6	31
	1.2V	15	19	0	22.7	38
	1.5V	15	19	0	25.2	39
	1.8V	12	22	0	25.8	41
	2.5V	22	12	56	30	84
	3.3V	15	12	56	30.8	116
10V	1.0V	18	14	0	18.8	37
	1.2V	18	14	0	20.4	41
	1.5V	18	16	0	22	42
	1.8V	15	19	0	23.6	46
	2.5V	27	10	56	26.5	90
	3.3V	22	10	56	28.9	122
8V	1.0V	22	10	0	17.2	17.2
	1.2V	22	13	0	18.7	18.7
	1.5V	18	15	0	20.1	20.1
	1.8V	18	15	0	20.9	20.9
	2.5V	39	6	56	23.6	23.6
	3.3V	27	6	56	22.8	22.8
6.6V	1.0V	27	10	0	13.8	13.8
	1.2V	27	10	0	15.2	15.2
	1.5V	22	13	0	16.4	16.4
	1.8V	22	13	0	19.6	19.6
	2.5V	47	4	56	20.4	20.4
	3.3V	39	4	56	21.1	21.1
5V	1.0V	33	10	0	12.4	12.4
	1.2V	33	10	0	13.4	13.4
	1.5V	27	13	0	14.3	14.3
	1.8V	27	13	0	15.4	15.4
	2.5V	68	1	56	15.5	15.5
	3.3V	47	1	56	12.9	12.9

Smallest Solution Size						
C_{IN} = 3 x 22µF/1206						
$V_{OUT} \leq 1.8V$, C_{OUT} = 22µF/0805 + 2x47µF/0805 $3.3V > V_{OUT} > 1.8V$, C_{OUT} = 3x47µF/1206						
R_A = 100 kΩ						
PVIN (V)	VOUT (V)	C_A (pF)	R_{CA} (kΩ)	R_{EA} (kΩ)	Ripple (mV)	Deviation (mV)
14V	1.0V	12	36	Open	15	78
	1.2V	12	36	Open	18	93
	1.5V	12	36	Open	22	104
	1.8V	12	36	Open	25	130
	2.5V	15	27	Open	32	162
	3.3V	10	27	Open	46	200
12V	1.0V	22	27	Open	15	84
	1.2V	22	27	Open	18	97
	1.5V	18	27	Open	21	118
	1.8V	18	27	Open	24	130
	2.5V	22	27	Open	30	172
	3.3V	15	27	Open	43	213
10V	1.0V	56	20	Open	15	85
	1.2V	47	20	Open	17	100
	1.5V	39	20	Open	20	120
	1.8V	33	20	Open	22	140
	2.5V	33	20	Open	29	177
	3.3V	22	20	Open	41	230
8V	1.0V	200	10	Open	14	83
	1.2V	200	10	Open	16	90
	1.5V	150	10	Open	19	107
	1.8V	82	10	Open	20	138
	2.5V	68	10	Open	27	178
	3.3V	39	10	Open	36	239
6.6V	1.0V	200	10	Open	13	99
	1.2V	200	10	Open	15	105
	1.5V	200	10	Open	17	118
	1.8V	150	10	Open	19	138
	2.5V	100	10	Open	24	183
	3.3V	56	10	Open	32	250
5V	1.0V	200	10	Open	12	123
	1.2V	200	10	Open	13	132
	1.5V	200	10	Open	16	145
	1.8V	200	10	Open	17	156
	2.5V	100	10	Open	20	216
	3.3V	100	10	Open	21	253

Table 5: R_A, C_A, R_{CA} and R_{EA} Values for Various PVIN/VOUT Combinations: Best Performance vs. Smallest Solution Size. Use the equations in Figure 10 to calculate R_B.

Note 6: Output ripple is measured at no load and nominal deviation is for a 15A load transient step.

Note 7: For compensation values of output voltage in between the specified output voltages, choose compensation values of the lower output voltage setting.

Thermal Considerations

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for. The Enpirion PowerSoC helps alleviate some of those concerns.

The Enpirion EN23F0QI DC-DC converter is packaged in an 8x11x3mm 68-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 150°C.

The EN23F0QI is guaranteed to support the full 4A output current up to 85°C ambient temperature. The following example and calculations illustrate the thermal performance of the EN23F0QI.

Example:

V_{IN} = 12V

V_{OUT} = 1.2V

I_{OUT} = 15A

First calculate the output power.

P_{OUT} = 1.2V x 15A = 18W

Next, determine the input power based on the efficiency (η) shown in Figure 11.

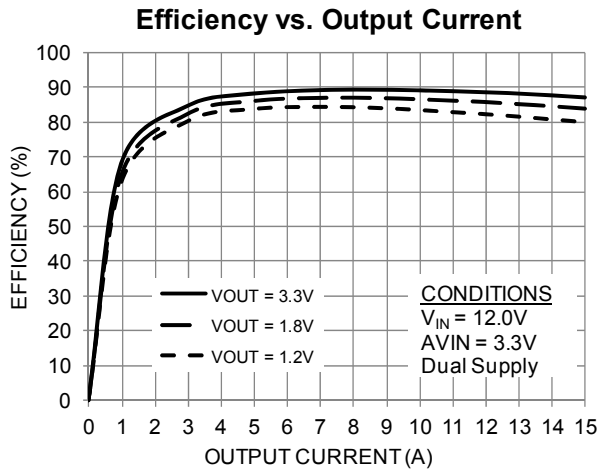


Figure 11: Efficiency vs. Output Current

For V_{IN} = 12V, V_{OUT} = 1.2V at 15A, η ≈ 80%

η = P_{OUT} / P_{IN} = 80% = 0.8

P_{IN} = P_{OUT} / η

P_{IN} ≈ 18W / 0.8 ≈ 22.5W

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

P_D = P_{IN} – P_{OUT}

≈ 22.5W – 18W ≈ 4.5W

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EN23F0QI has a θ_{JA} value of 13 ºC/W without airflow.

Determine the change in temperature (ΔT) based on P_D and θ_{JA}.

ΔT = P_D x θ_{JA}

ΔT ≈ 4.5W x 13°C/W = 58.5°C ≈ 59°C

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

T_J = T_A + ΔT

T_J ≈ 25°C + 59°C ≈ 84°C

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

T_{AMAX} = T_{JMAX} – P_D x θ_{JA}

≈ 125°C – 59°C ≈ 66°C

The maximum ambient temperature the device can reach is 66°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.

Engineering Schematic

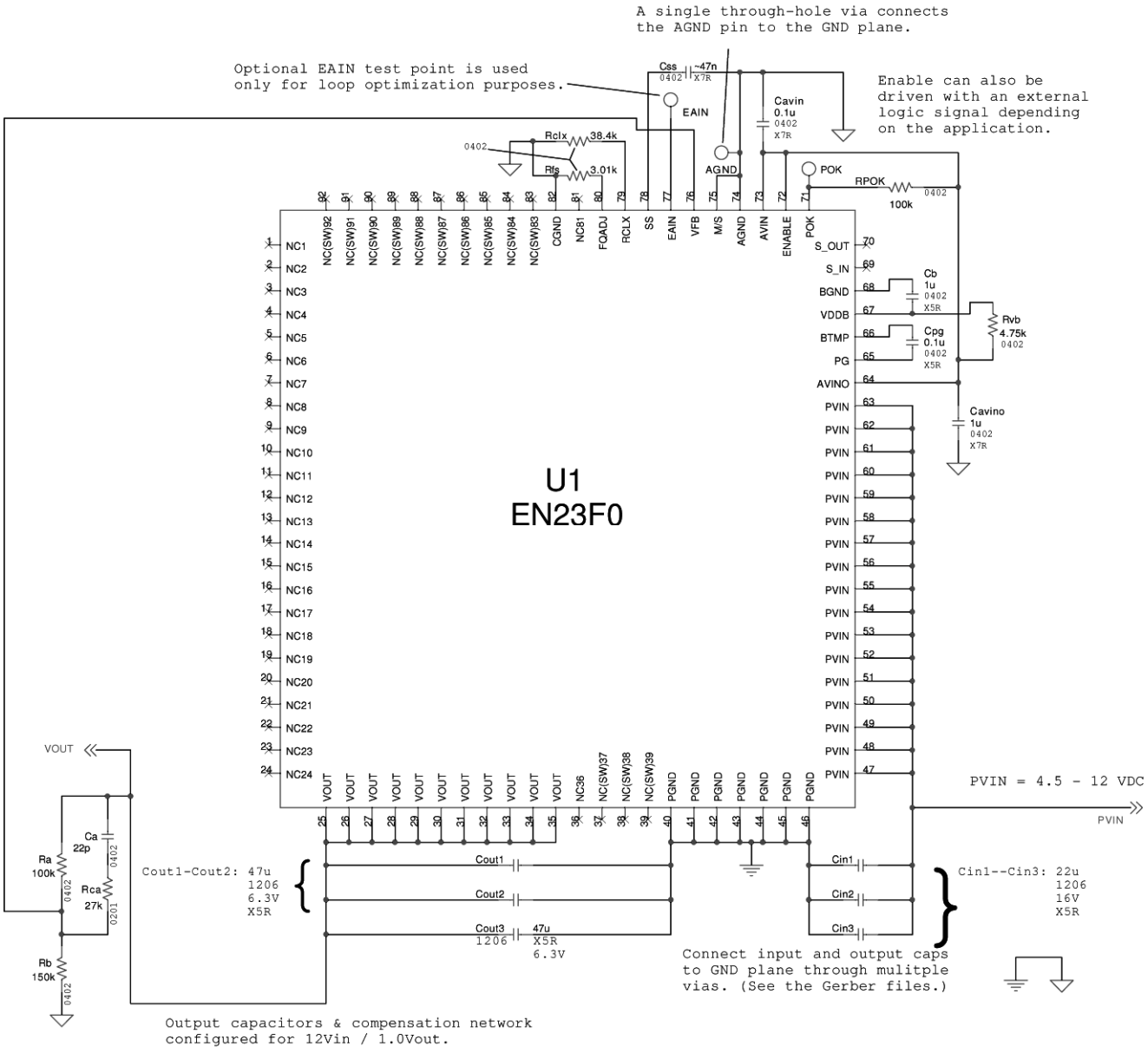


Figure 12: Critical Components Engineering Schematic

Layout Recommendation

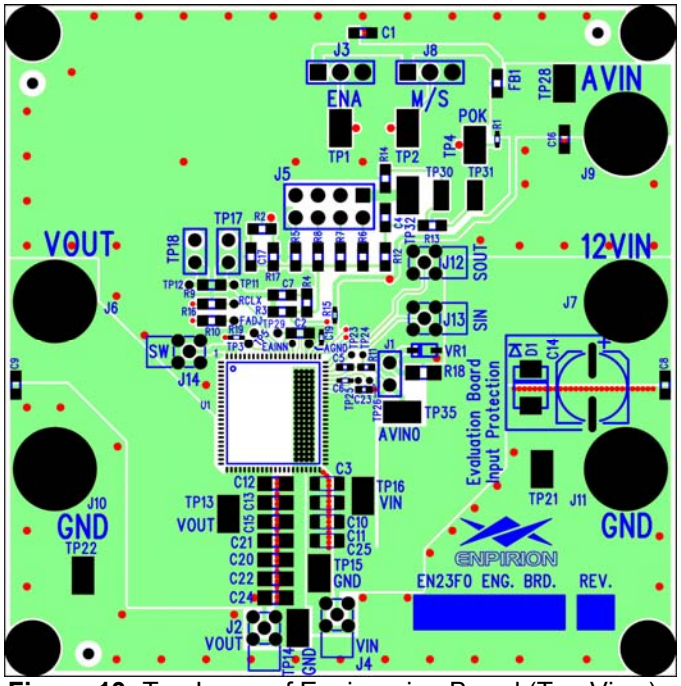


Figure 13: Top Layer of Engineering Board (Top View).

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN23F0QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN23F0QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The PGND connections for the input and output capacitors on layer 1 need to have a slit between them in order to provide some separation between input and output current loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

Recommendation 4: The thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. If vias cannot be placed under the capacitors, then place them on both sides of the slit in the top layer PGND copper.

Recommendation 6: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 13 this connection is made at the input capacitor.

Recommendation 7: The layer 1 metal under the device must not be more than shown in Figure 13. Refer to the section regarding Exposed Metal on Bottom of Package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 8: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node. Contact Enpirion Technical Support for any remote sensing applications.

Recommendation 9: Keep R_A, C_A, R_B, and R_{CA} close to the VFB pin (Refer to Figure 13). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pins 52 and 53 instead of going through the GND plane.

Recommendation 10: Follow all the layout recommendations as close as possible to optimize performance. Enpirion provides schematic and layout reviews for all customer designs. Contact Enpirion Applications Engineering for detailed support (techsupport@enpirion.com).

Design Considerations for Lead-Frame Based Modules

Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package, as shown in Figure 14.

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN23F0QI should be clear of any metal (copper pours, traces, or vias) except for the thermal pad. The “shaded-out” area in Figure 14 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the shaded-out area runs the risk of undesirable shorted connections even if it is covered by soldermask.

The solder stencil aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package. Please consult the Enpirion Manufacturing Application Note for more details and recommendations.

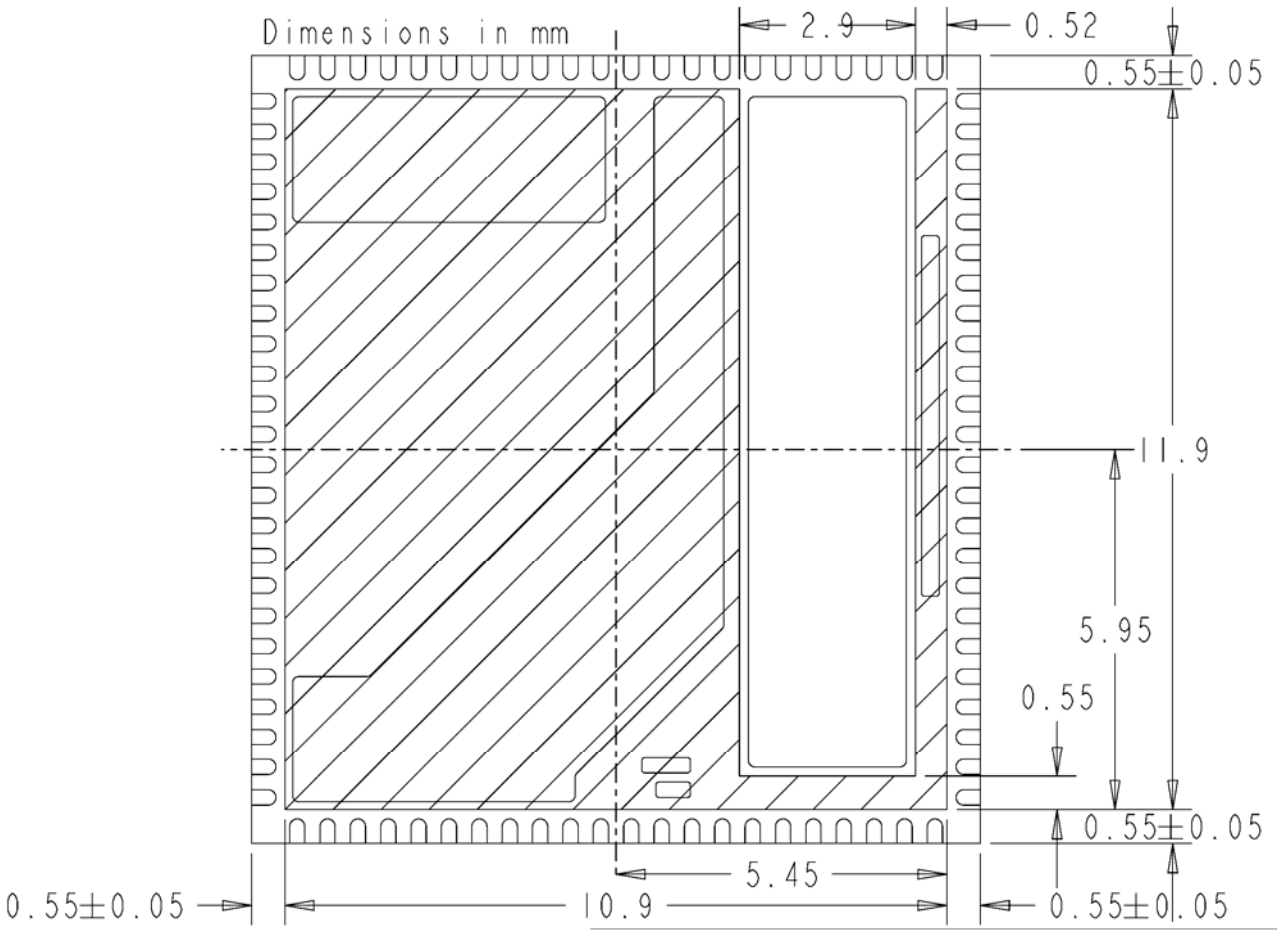


Figure 14: Lead-Frame exposed metal (Bottom View)

Shaded area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

Recommended PCB Footprint

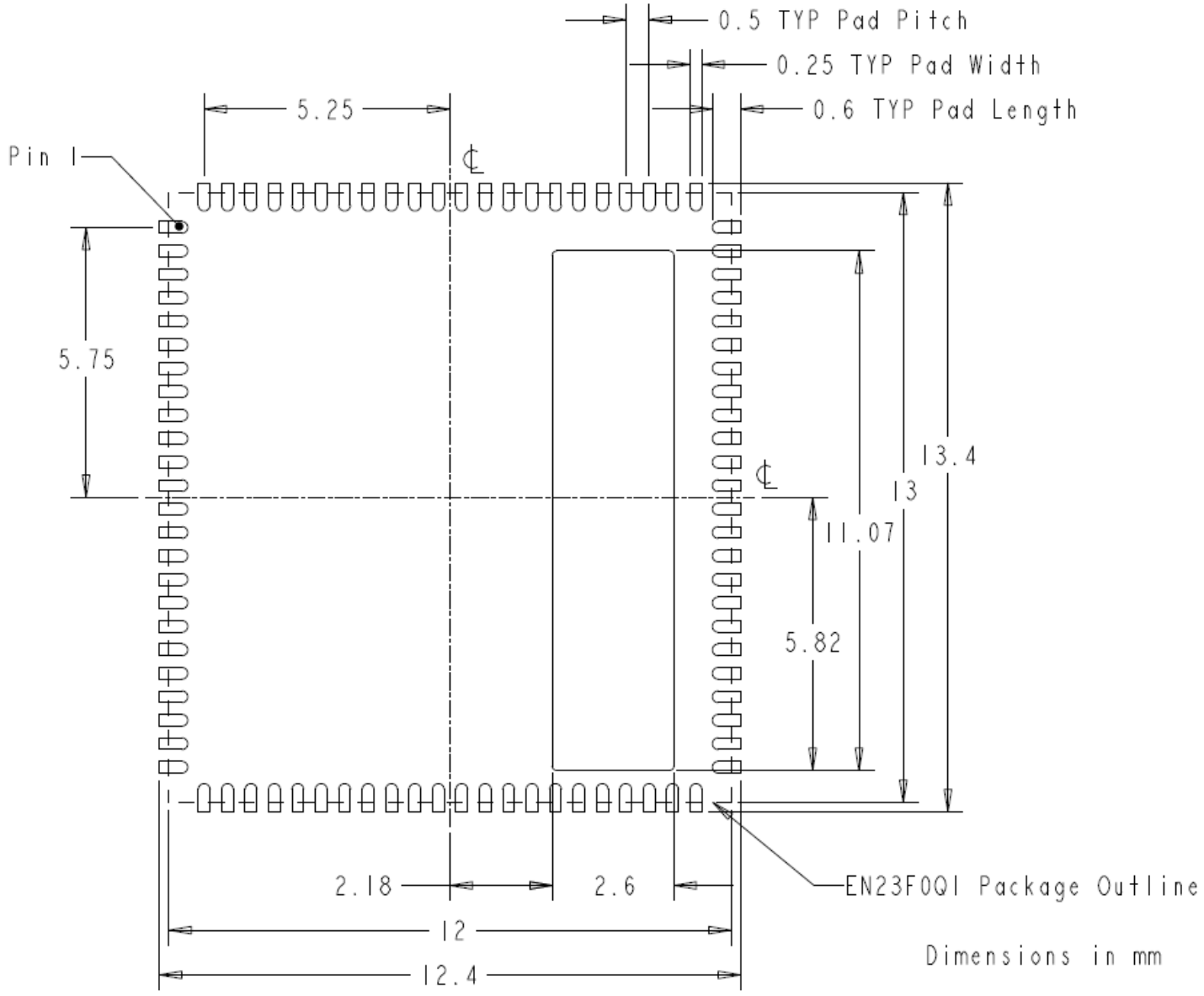


Figure 15: EN23F0QI PCB Footprint (Top View)

Package and Mechanical

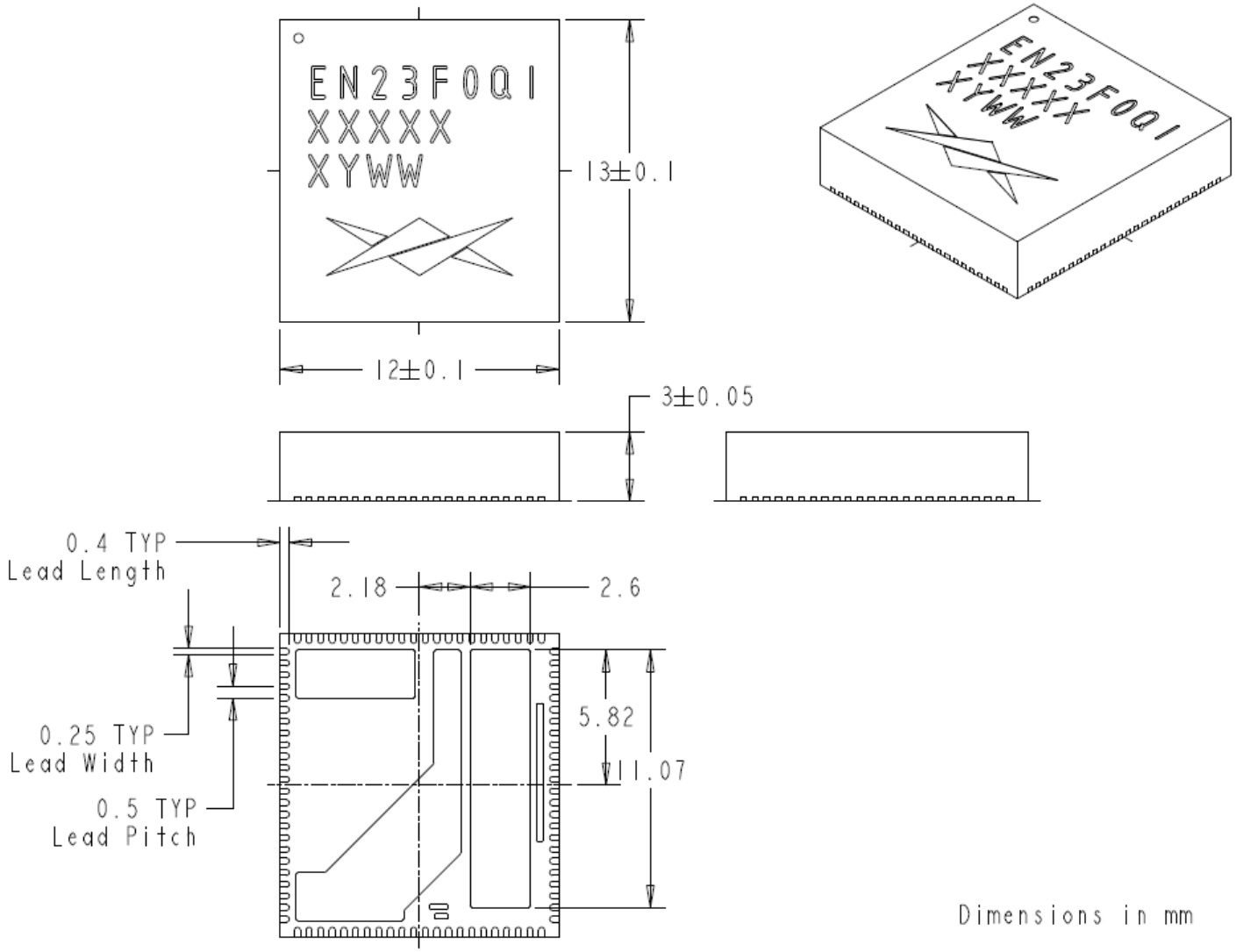


Figure 16: EN23F0QI Package Dimensions (Bottom View)

Packing and Marking Information: http://www.enpirion.com/resource-center-packing-and-marking-information.htm

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