



DATA SHEET

BIPOLAR ANALOG INTEGRATED CIRCUIT μ PC8187TB

SILICON MMIC HI-IP₃ FREQUENCY UP-CONVERTER FOR WIRELESS TRANSCEIVER

DESCRIPTION

The μ PC8187TB is a silicon monolithic integrated circuit designed as frequency up-converter for wireless transceiver. This IC is higher operating frequency, lower distortion and higher conversion gain than conventional μ PC8163TB.

This IC is manufactured using NEC's 30 GHz $f_{\max}$ UHS0 (Ultra High Speed Process) silicon bipolar process.

FEATURES

- High output frequency : $f_{RFout} = 0.8$ to 2.5 GHz
- High-density surface mounting : 6-pin super minimold package
- Supply voltage : $V_{CC} = 2.7$ to 3.3 V
- Higher IP₃ : OIP₃ = +10 dBm @ $f_{RFout} = 1.9$ GHz

APPLICATION

- TDMA, PCS, CDMA etc.

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
μ PC8187TB-E3-A	6-pin super minimold	C3G	• Embossed tape 8 mm wide. • Pin 1, 2, 3 face the tape perforation side. • Qty 3 kpcs/reel.

Remark To order evaluation samples, please contact your local sales office.

(Part number for sample order: μ PC8187TB-A)

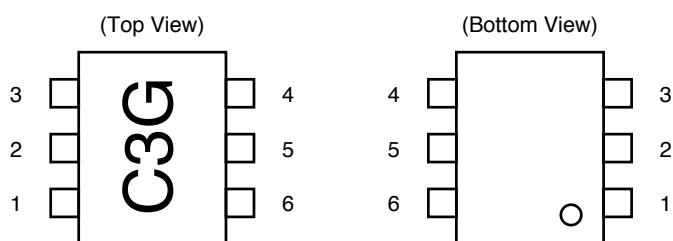
Caution Electro-static sensitive devices

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

CONTENTS

1. PIN CONNECTIONS.....	3
2. SERIES PRODUCTS.....	3
3. BLOCK DIAGRAM	3
4. SYSTEM APPLICATION EXAMPLES (SCHEMATICS OF IC LOCATION IN THE SYSTEM).....	4
5. PIN EXPLANATION.....	5
6. ABSOLUTE MAXIMUM RATINGS.....	6
7. RECOMMENDED OPERATING RANGE.....	6
8. ELECTRICAL CHARACTERISTICS	6
9. OTHER CHARACTERISTICS, FOR REFERENCE PURPOSES ONLY	7
10. TEST CIRCUITS.....	8
10.1 TEST CIRCUIT 1 ($f_{RFout} = 0.83$ GHz)	8
10.2 TEST CIRCUIT 2 ($f_{RFout} = 1.9$ GHz)	9
10.3 TEST CIRCUIT 3 ($f_{RFout} = 2.4$ GHz)	10
11. TYPICAL CHARACTERISTICS.....	12
11.1 $f_{RFout} = 0.83$ GHz	13
11.2 $f_{RFout} = 1.9$ GHz	17
11.3 $f_{RFout} = 2.4$ GHz	21
12. S-PARAMETERS FOR EACH PORT.....	25
13. S-PARAMETERS FOR MATCHED RF OUTPUT	26
14. PACKAGE DIMENSIONS.....	28
15. NOTE ON CORRECT USE	29
16. RECOMMENDED SOLDERING CONDITIONS.....	29

1. PIN CONNECTIONS



Pin No.	Pin Name
1	IFinput
2	GND
3	LOinput
4	GND
5	V _{CC}
6	RFoutput

2. SERIES PRODUCTS ($T_A = +25^\circ\text{C}$, $V_{CC} = V_{PS} = V_{RFout} = 3.0\text{ V}$, $Z_S = Z_L = 50\ \Omega$)

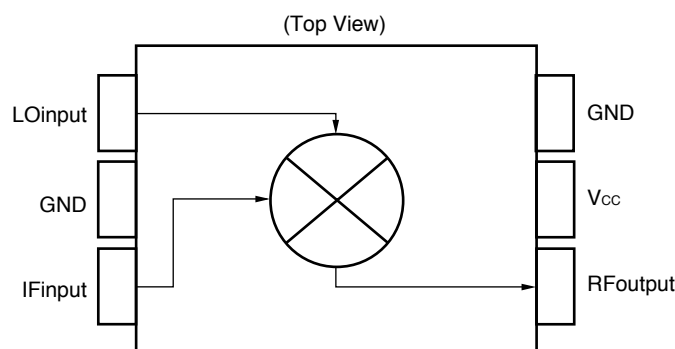
Part Number	I _{CC} (mA)	f _{RFout} (GHz)	CG (dB)		
			@RF 0.9 GHz ^{Note}	@RF 1.9 GHz	@RF 2.4 GHz
μ PC8187TB	15	0.8 to 2.5	11	11	10
μ PC8106TB	9	0.4 to 2.0	9	7	–
μ PC8172TB	9	0.8 to 2.5	9.5	8.5	8.0
μ PC8109TB	5	0.4 to 2.0	6	4	–
μ PC8163TB	16.5	0.8 to 2.0	9	5.5	–

Part Number	P _{O(sat)} (dBm)			OIP ₃ (dBm)		
	@RF 0.9 GHz ^{Note}	@RF 1.9 GHz	@RF 2.4 GHz	@RF 0.9 GHz ^{Note}	@RF 1.9 GHz	@RF 2.4 GHz
μ PC8187TB	+4	+2.5	+1	+10	+10	+8.5
μ PC8106TB	–2	–4	–	+5.5	+2.0	–
μ PC8172TB	+0.5	0	–0.5	+7.5	+6.0	+4.0
μ PC8109TB	–5.5	–7.5	–	+1.5	–1.0	–
μ PC8163TB	+0.5	–2	–	+9.5	+6.0	–

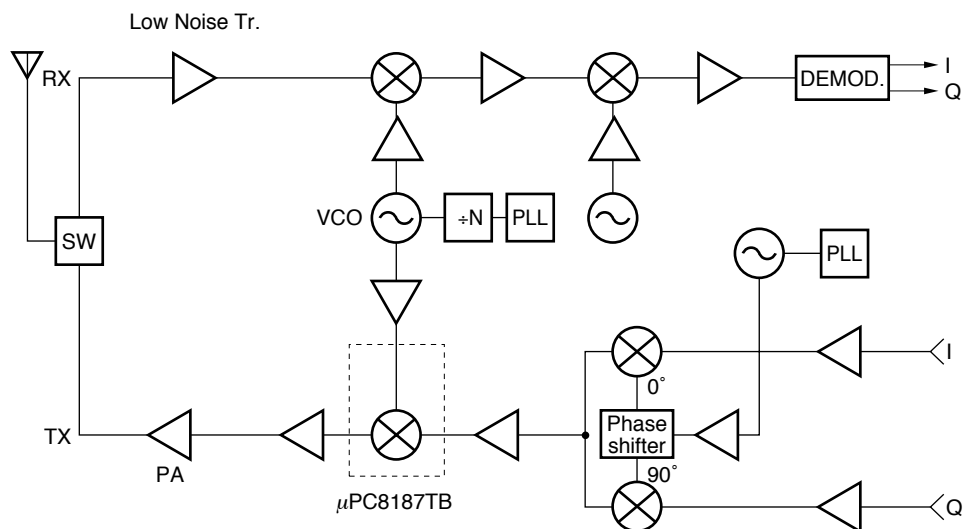
Note f_{RFout} = 0.83 GHz @ μ PC8163TB and μ PC8187TB

Remark Typical performance. Please refer to **8. ELECTRICAL CHARACTERISTICS** in detail.
To know the associated product, please refer to each latest data sheet.

3. BLOCK DIAGRAM



4. SYSTEM APPLICATION EXAMPLES (SCHEMATICS OF IC LOCATION IN THE SYSTEM)



5. PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V) ^{Note}	Function and Explanation	Equivalent Circuit
1	IFinput	–	1.2	This pin is IF input to double balanced mixer (DBM). The input is designed as high impedance. The circuit contributes to suppress spurious signal. Also this symmetrical circuit can keep specified performance insensitive to process-condition distribution. For above reason, double balanced mixer is adopted.	
2 4	GND	GND	–	GND pin. Ground pattern on the board should be formed as wide as possible. Track Length should be kept as short as possible to minimize ground impedance.	
3	LOinput	–	2.1	Local input pin. Recommendable input level is –10 to 0 dBm.	
5	V _{CC}	2.7 to 3.3	–	Supply voltage pin.	
6	RFoutput	Same bias as V _{CC} through external inductor	–	This pin is RF output from DBM. This pin is designed as open collector. Due to the high impedance output, this pin should be externally equipped with LC matching circuit to next stage.	

Note Each pin voltage is measured at $V_{CC} = V_{RFout} = 2.8$ V.

6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Rating	Unit
Supply Voltage	V_{CC}	$T_A = +25^{\circ}\text{C}$	3.6	V
Power Dissipation	P_D	Mounted on double-side copperclad 50 × 50 × 1.6 mm epoxy glass PWB, $T_A = +85^{\circ}\text{C}$	270	mW
Operating Ambient Temperature	T_A		–40 to +85	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		–55 to +150	$^{\circ}\text{C}$
Maximum Input Power	P_{in}		+10	dBm

7. RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Supply Voltage	V_{CC}	2.7	2.8	3.3	V	The same voltage should be applied to pin 5 and 6
Operating Ambient Temperature	T_A	–40	+25	+85	$^{\circ}\text{C}$	
Local Input Power	P_{LOin}	–10	–5	0	dBm	$Z_s = 50\ \Omega$ (without matching)
RF Output Frequency	f_{RFout}	0.8	–	2.5	GHz	With external matching circuit
IF Input Frequency	f_{IFin}	50	–	400	MHz	

8. ELECTRICAL CHARACTERISTICS

($T_A = +25^{\circ}\text{C}$, $V_{CC} = V_{RFout} = 2.8\text{ V}$, $f_{IFin} = 150\text{ MHz}$, $P_{LOin} = -5\text{ dBm}$)

Parameter	Symbol	Test Conditions ^{Note}	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No signal	11	15	19	mA
Conversion Gain	CG1	$f_{RFout} = 0.83\text{ GHz}$, $P_{IFin} = -20\text{ dBm}$	8	11	14	dB
	CG2	$f_{RFout} = 1.9\text{ GHz}$, $P_{IFin} = -20\text{ dBm}$	8	11	14	dB
	CG3	$f_{RFout} = 2.4\text{ GHz}$, $P_{IFin} = -20\text{ dBm}$	7	10	13	dB
Saturated Output Power	$P_{O(sat)1}$	$f_{RFout} = 0.83\text{ GHz}$, $P_{IFin} = 0\text{ dBm}$	+1.5	+4	–	dBm
	$P_{O(sat)2}$	$f_{RFout} = 1.9\text{ GHz}$, $P_{IFin} = 0\text{ dBm}$	0	+2.5	–	dBm
	$P_{O(sat)3}$	$f_{RFout} = 2.4\text{ GHz}$, $P_{IFin} = 0\text{ dBm}$	–1.5	+1	–	dBm

Note $f_{RFout} < f_{LOin}$ @ $f_{RFout} = 0.83\text{ GHz}$

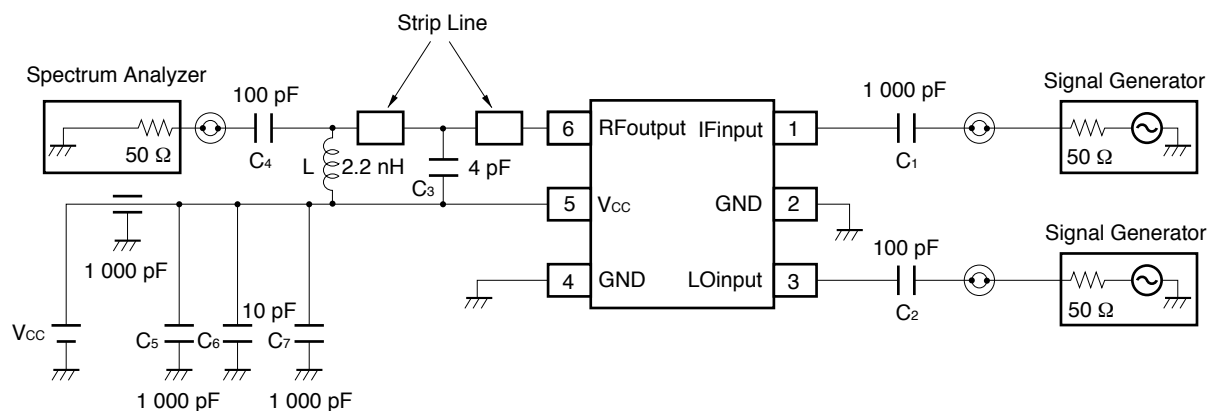
$f_{LOin} < f_{RFout}$ @ $f_{RFout} = 1.9\text{ GHz}/2.4\text{ GHz}$

9. OTHER CHARACTERISTICS, FOR REFERENCE PURPOSES ONLY(T_A = +25°C, V_{CC} = V_{RFout} = 2.8 V, P_{LOin} = -5 dBm)

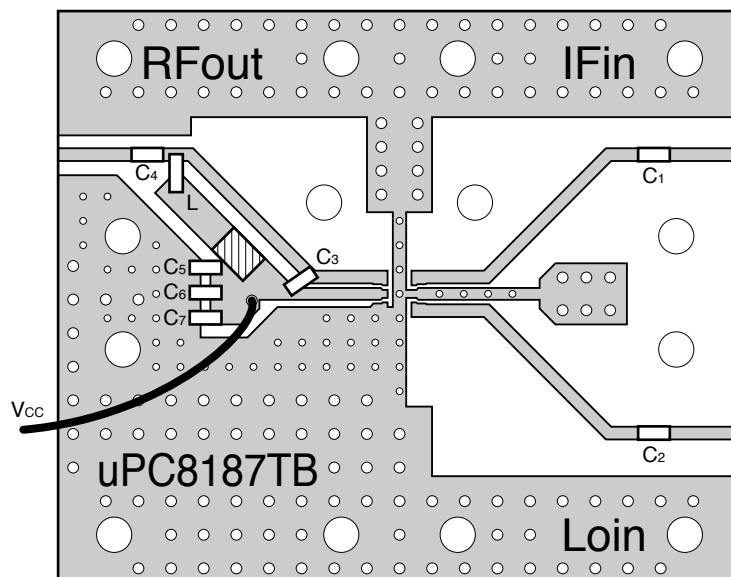
Parameter	Symbol	Test Conditions ^{Note}		Value	Unit
Output 3rd Order Distortion Intercept Point	OIP ₃₁	f _{RFout} = 0.83 GHz	f _{Fin1} = 150 MHz f _{Fin2} = 151 MHz	+10	dBm
	OIP ₃₂	f _{RFout} = 1.9 GHz		+10	dBm
	OIP ₃₃	f _{RFout} = 2.4 GHz		+8.5	dBm
Input 3rd Order Distortion Intercept Point	IIP ₃₁	f _{RFout} = 0.83 GHz	f _{Fin1} = 150 MHz f _{Fin2} = 151 MHz	-1.0	dBm
	IIP ₃₂	f _{RFout} = 1.9 GHz		-1.0	dBm
	IIP ₃₃	f _{RFout} = 2.4 GHz		-1.5	dBm
SSB Noise Figure	SSB•NF1	f _{RFout} = 0.83 GHz	f _{Fin} = 150 MHz	11	dB
	SSB•NF2	f _{RFout} = 1.9 GHz		12	dB
	SSB•NF3	f _{RFout} = 2.4 GHz		12.5	dB

Note f_{RFout} < f_{LOin} @ f_{RFout} = 0.83 GHzf_{LOin} < f_{RFout} @ f_{RFout} = 1.9 GHz/2.4 GHz

★ 10. TEST CIRCUITS

10.1 TEST CIRCUIT 1 ($f_{RFout} = 0.83$ GHz)

EXAMPLE OF TEST CIRCUIT 1 ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

Form	Symbol	Value
Chip capacitor	C1, C5, C7	1 000 pF
	C2, C4	100 pF
	C6	10 pF
	C3	4 pF
Chip inductor	L	2.2 nH ^{Note}

(*1) 35 × 42 × 0.4 mm polyimide board, double-sided copper clad

(*2) Ground pattern on rear of the board

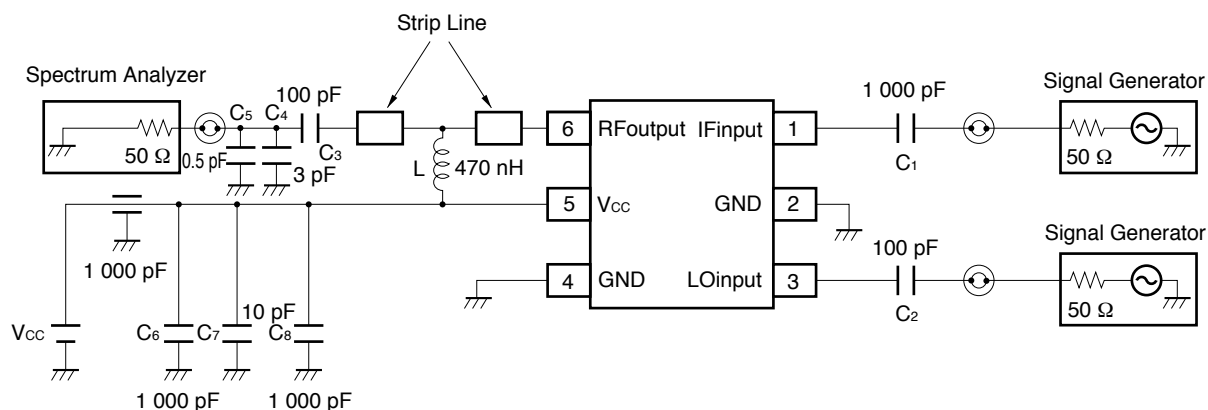
(*3) Solder plated patterns

(*4) ○○○ : Through holes

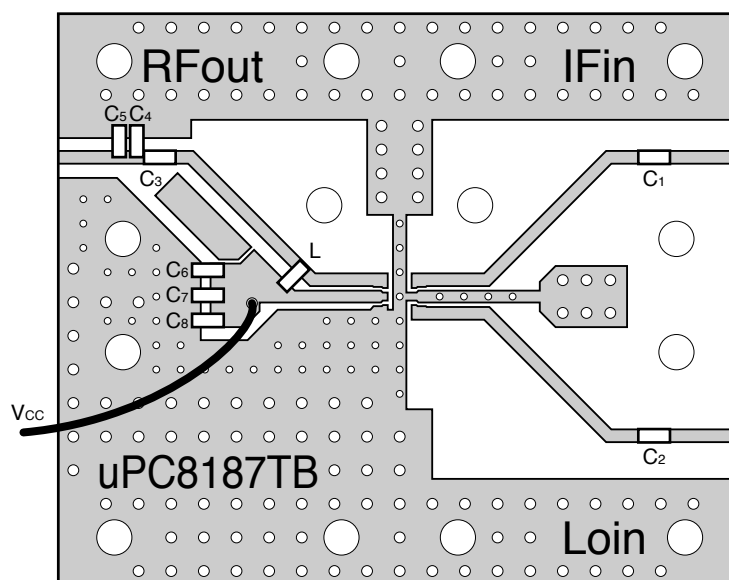
(*5)  : Join patterns with electrical tape

Note 2.2 nH: LL1608-FH2N25 (TOKO Co., Ltd.)

EXAMPLE OF TEST CIRCUIT 2 ASSEMBLED ON EVALUATION BOARD



EXAMPLE OF TEST CIRCUIT 2 ASSEMBLED ON EVALUATION BOARD

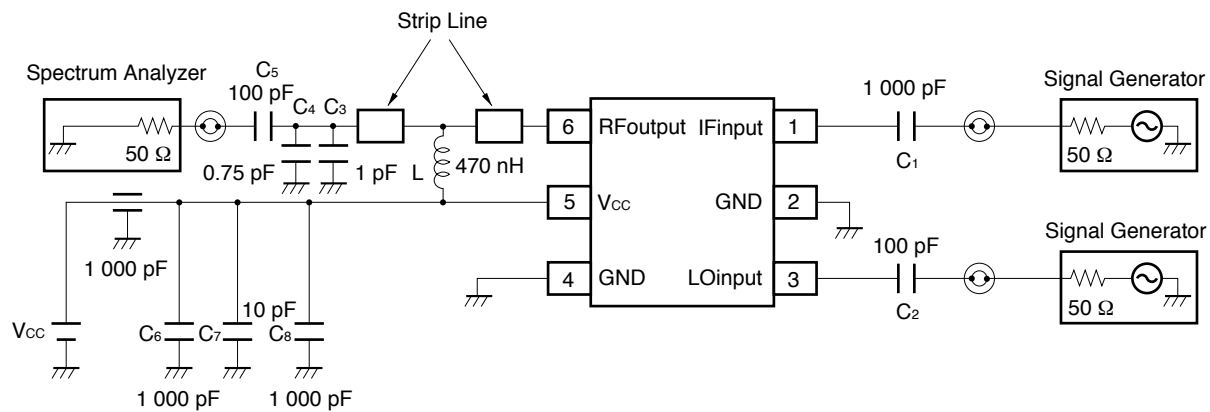
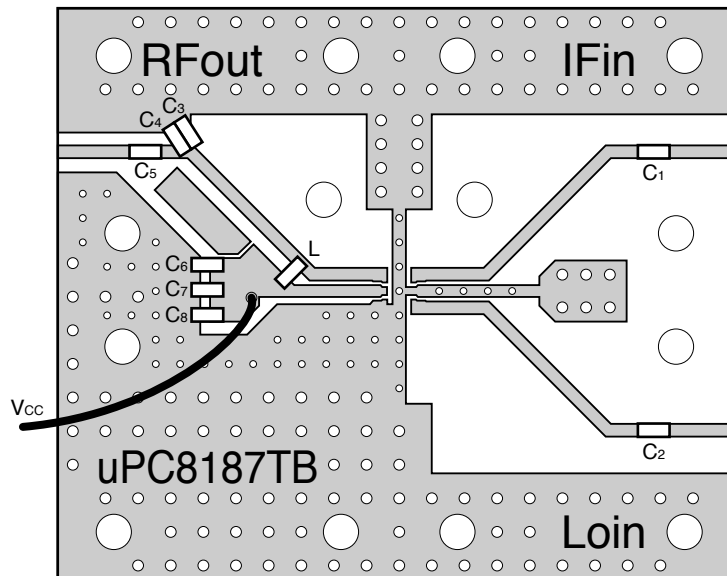


COMPONENT LIST

Form	Symbol	Value
Chip capacitor	C ₁ , C ₆ , C ₈	1 000 pF
	C ₂ , C ₃	100 pF
	C ₇	10 pF
	C ₄	3 pF
	C ₅	0.5 pF
Chip inductor	L	470 nH ^{Note}

Note 470 nH: LL2012-FR47 (TOKO Co., Ltd.)

- (*1) 35 × 42 × 0.4 mm polyimide board, double-sided copper clad
- (*2) Ground pattern on rear of the board
- (*3) Solder plated patterns
- (*4) ○○○: Through holes

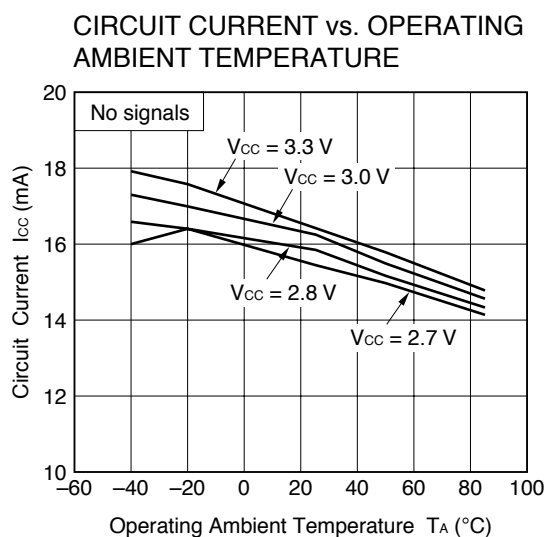
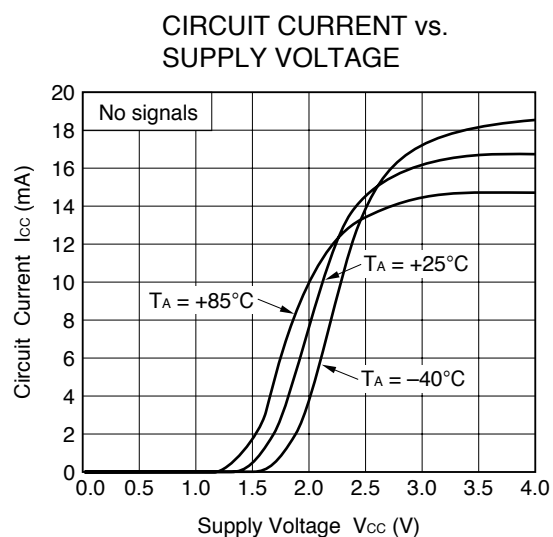
10.3 TEST CIRCUIT 3 ($f_{RFout} = 2.4$ GHz)**EXAMPLE OF TEST CIRCUIT 3 ASSEMBLED ON EVALUATION BOARD****COMPONENT LIST**

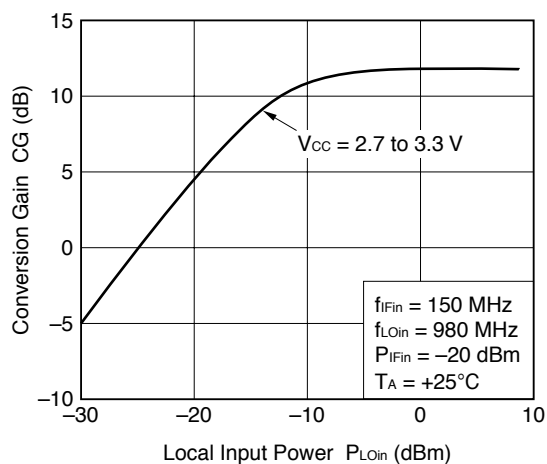
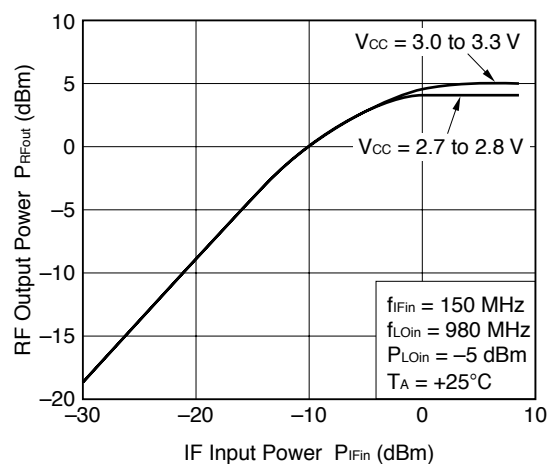
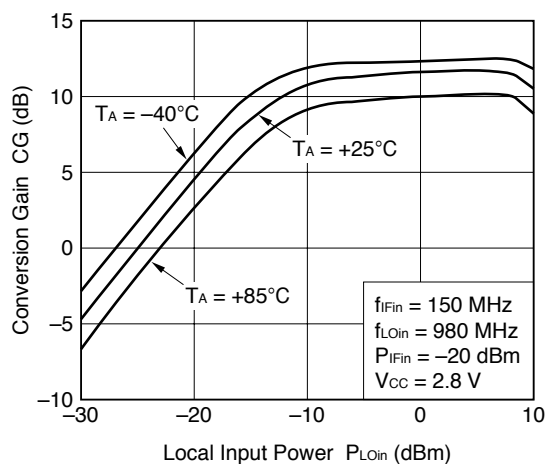
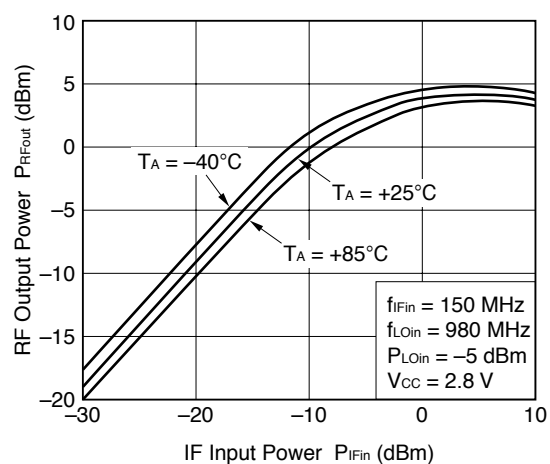
Form	Symbol	Value
Chip capacitor	C ₁ , C ₆ , C ₈	1 000 pF
	C ₂ , C ₅	100 pF
	C ₇	10 pF
	C ₃	1 pF
	C ₄	0.75 pF
Chip inductor	L	470 nH ^{Note}

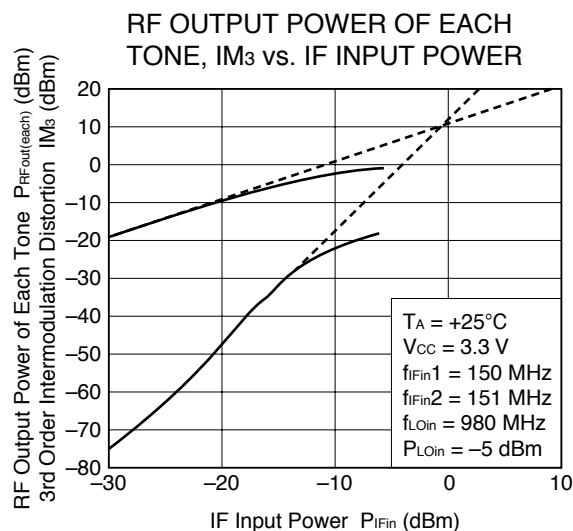
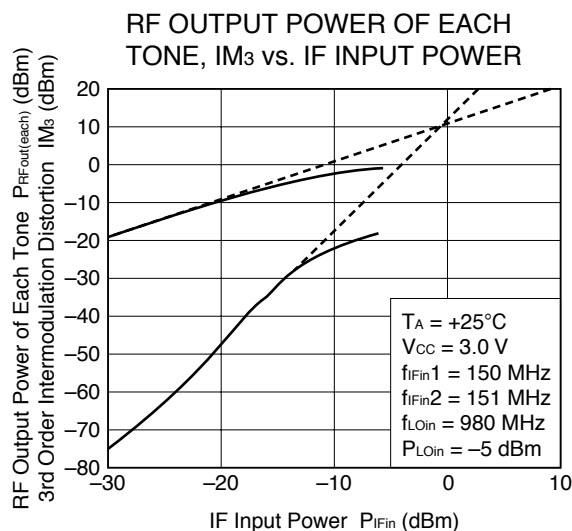
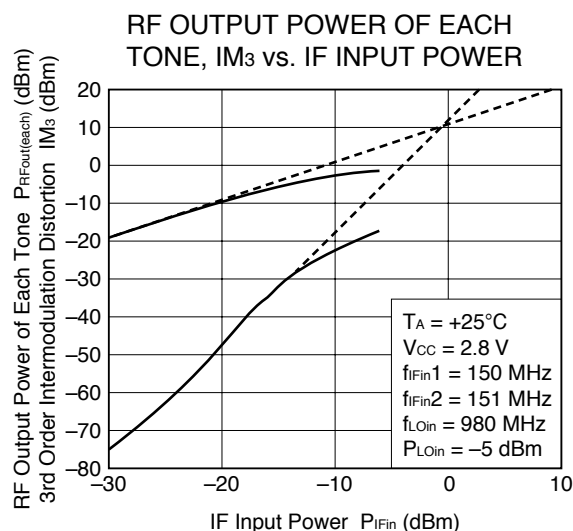
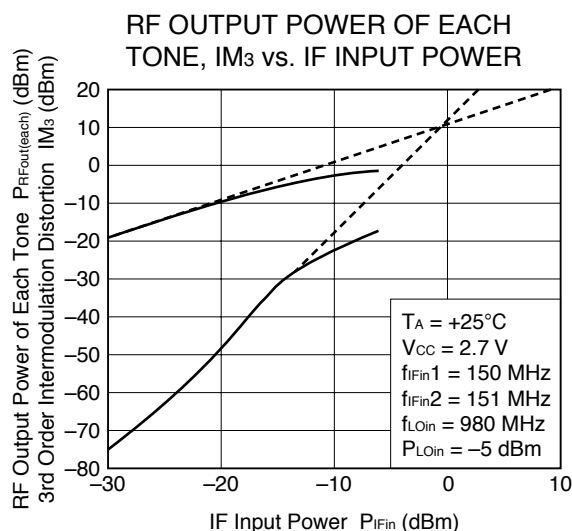
- (*)1 35 × 42 × 0.4 mm polyimide board, double-sided copper clad
 (*)2 Ground pattern on rear of the board
 (*)3 Solder plated patterns
 (*)4 ○○○: Through holes

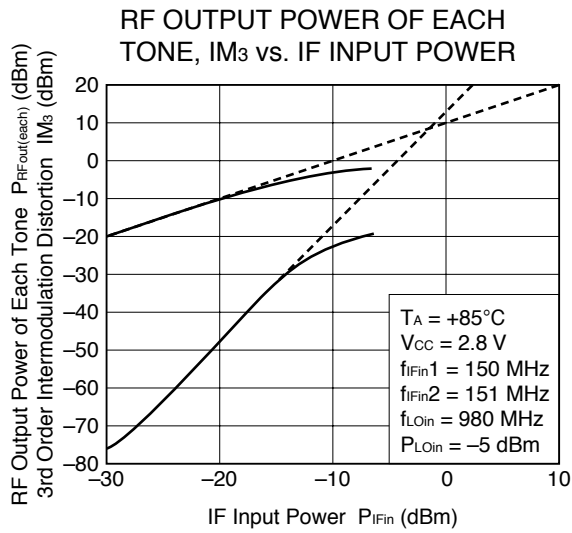
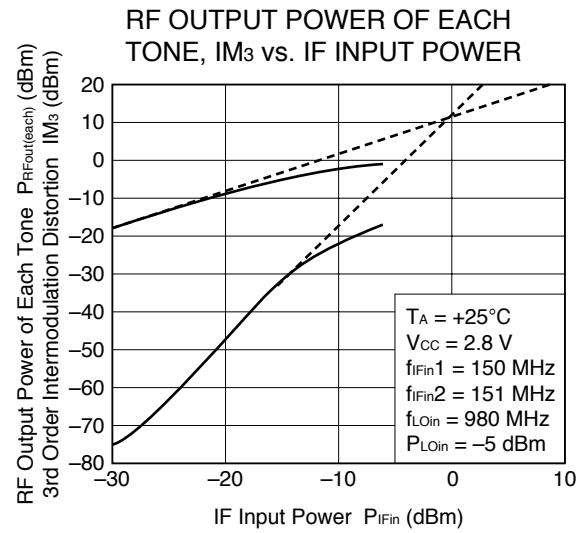
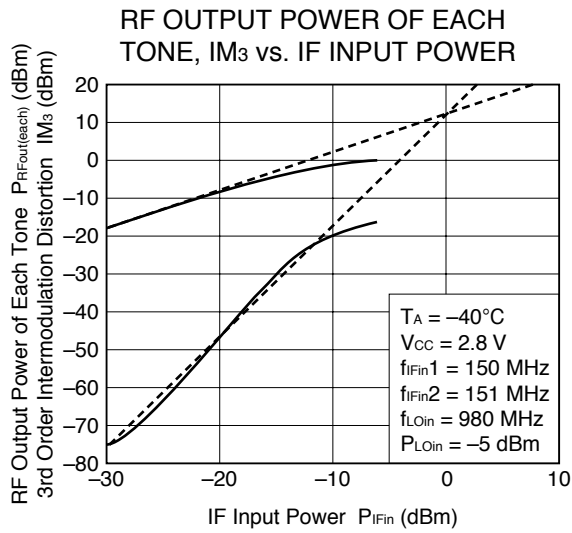
Note 470 nH: LL2012-FR47 (TOKO Co., Ltd.)

Caution The test circuits and board pattern on data sheet are for performance evaluation use only (They are not recommended circuits). In the case of actual design-in, matching circuit should be determined using S-parameter of desired frequency in accordance to actual mounting pattern.

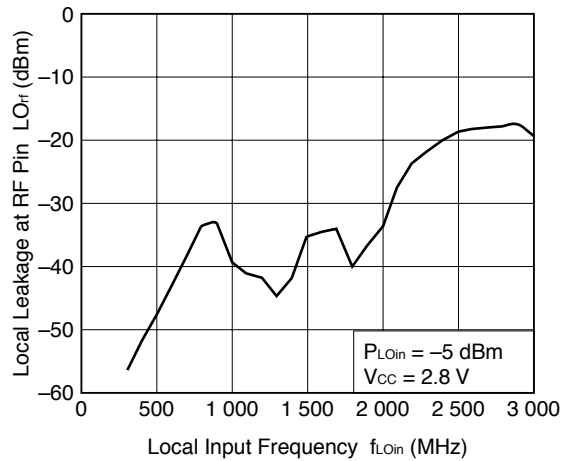
★ 11. TYPICAL CHARACTERISTICS (Unless otherwise specified, $T_A = +25^\circ\text{C}$, $V_{CC} = V_{RFout}$)

11.1 $f_{RFout} = 0.83 \text{ GHz}$ CONVERSION GAIN vs.
LOCAL INPUT POWERRF OUTPUT POWER vs.
IF INPUT POWERCONVERSION GAIN vs.
LOCAL INPUT POWERRF OUTPUT POWER vs.
IF INPUT POWER

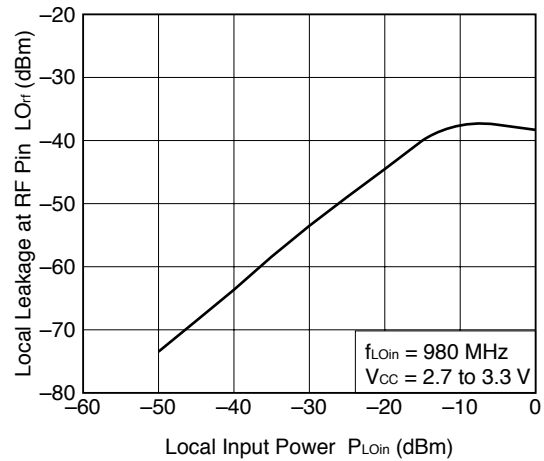




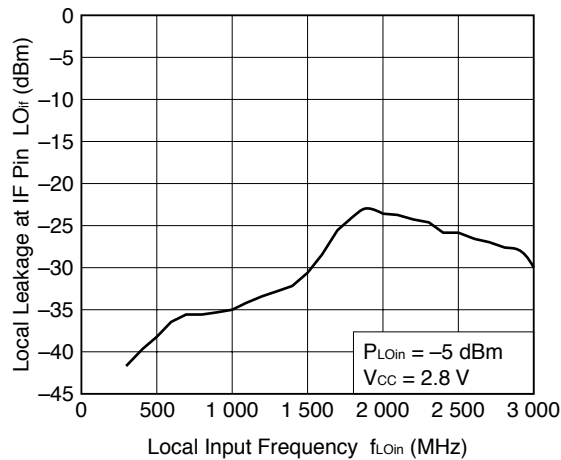
LOCAL LEAKAGE AT RF PIN vs.
LOCAL INPUT FREQUENCY



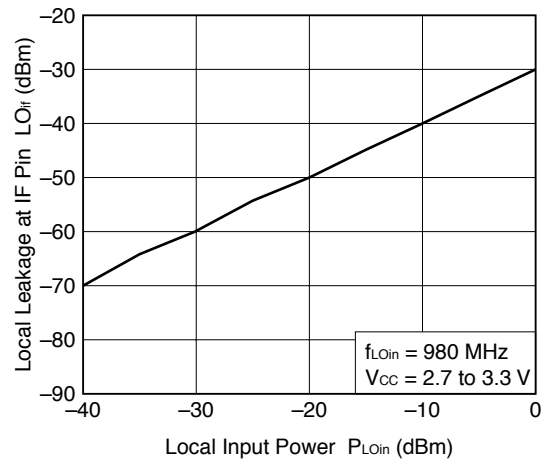
LOCAL LEAKAGE AT RF PIN vs.
LOCAL INPUT POWER



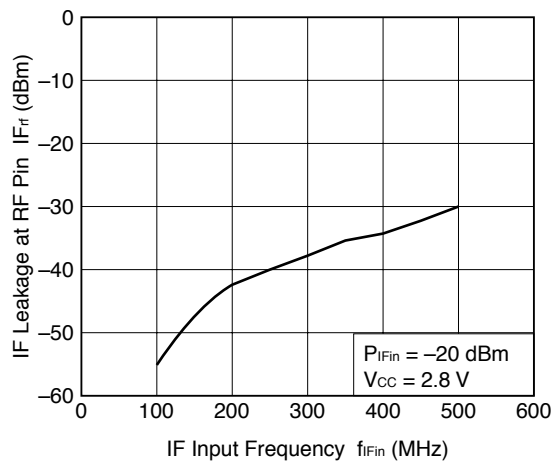
LOCAL LEAKAGE AT IF PIN vs.
LOCAL INPUT FREQUENCY



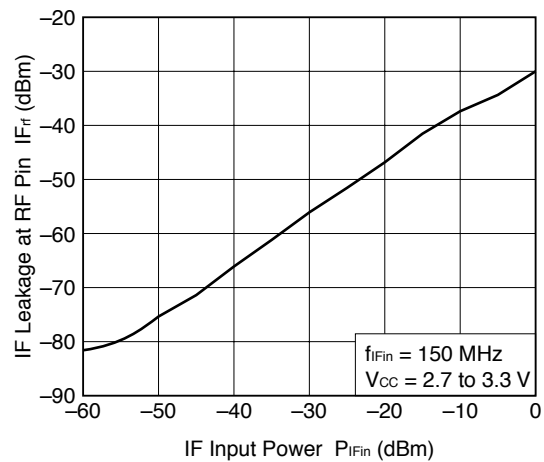
LOCAL LEAKAGE AT IF PIN vs.
LOCAL INPUT POWER

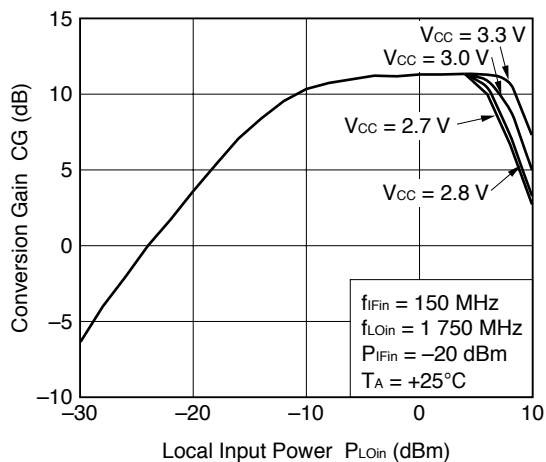
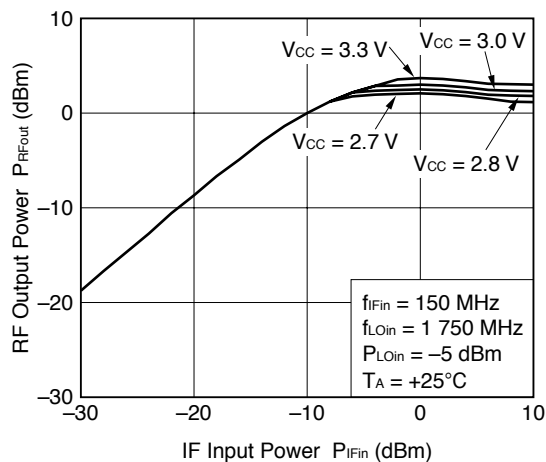
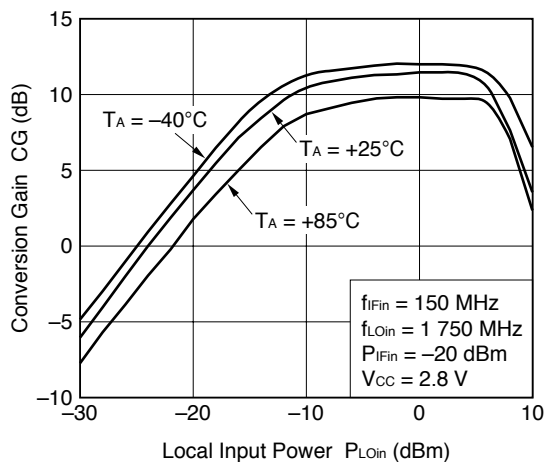
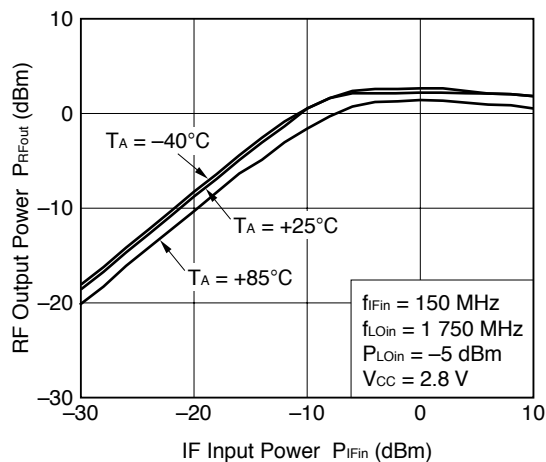


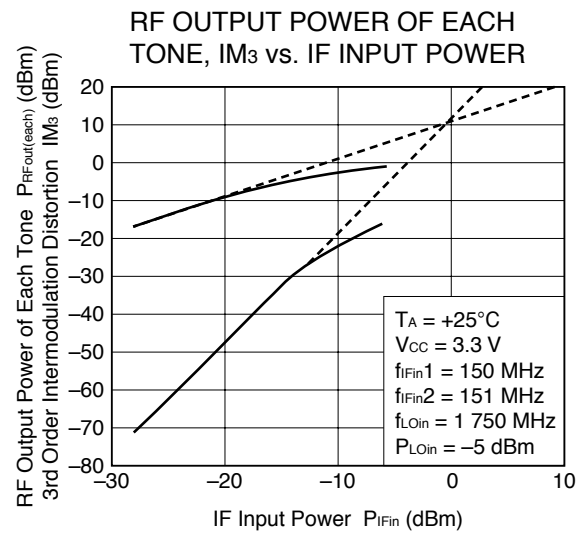
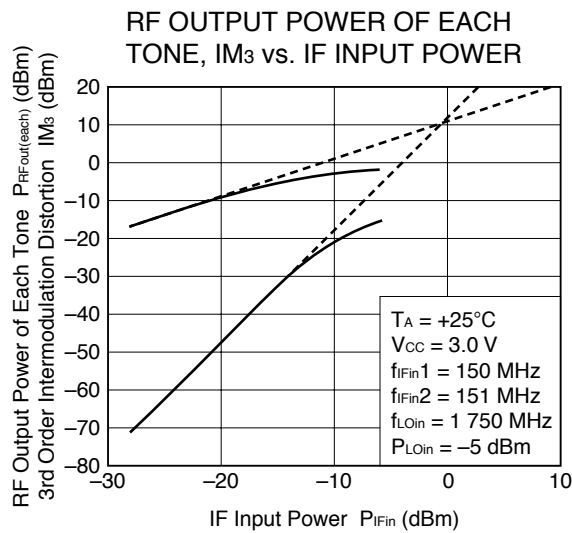
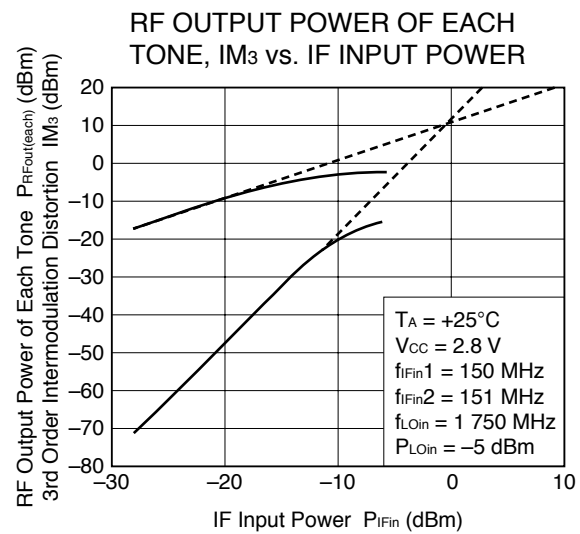
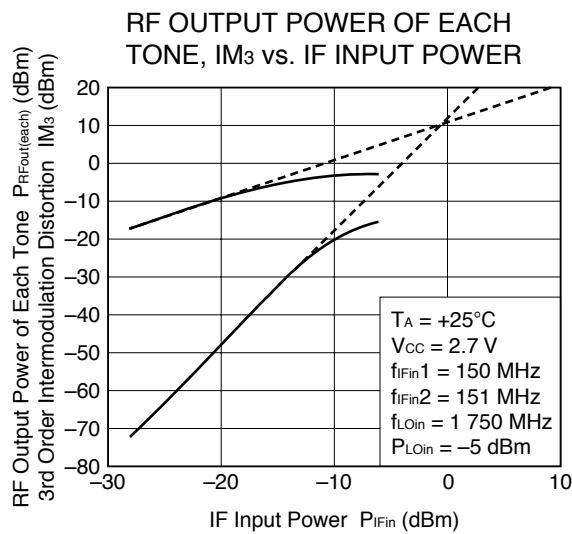
IF LEAKAGE AT RF PIN vs.
IF INPUT FREQUENCY

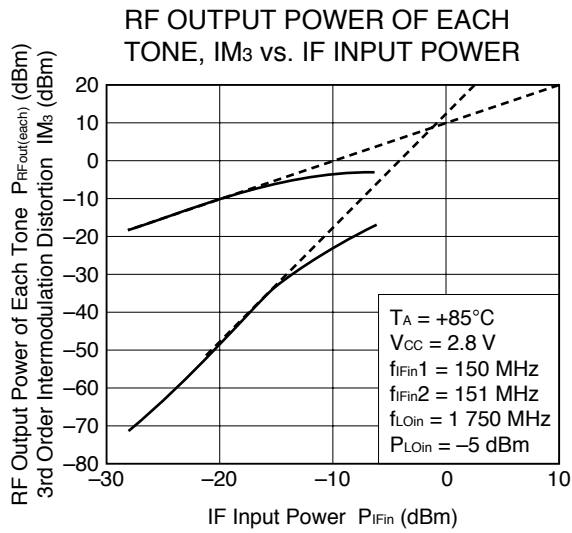
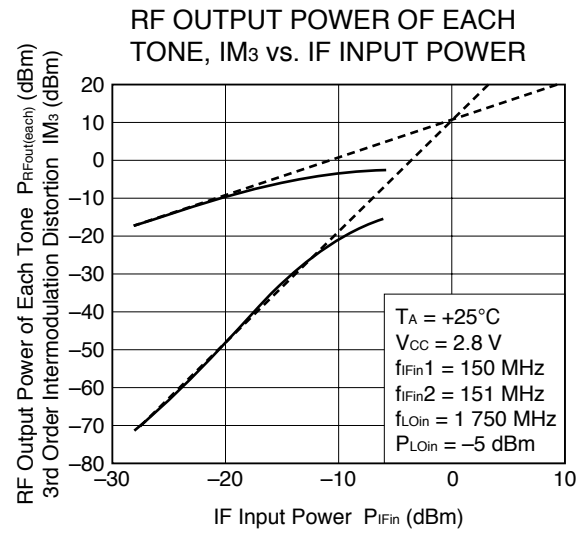
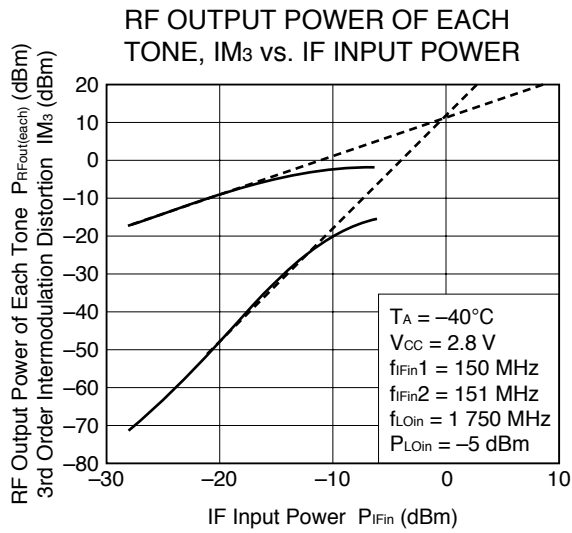


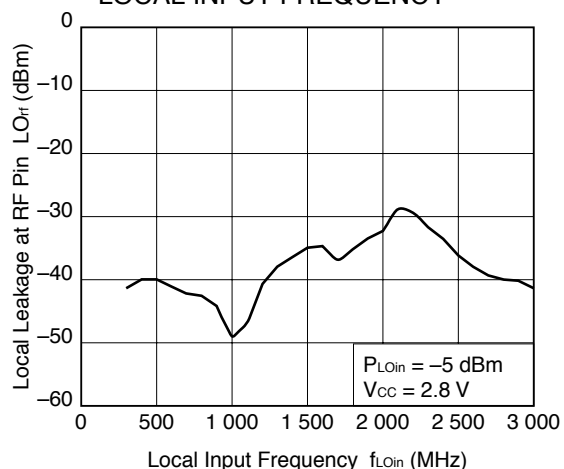
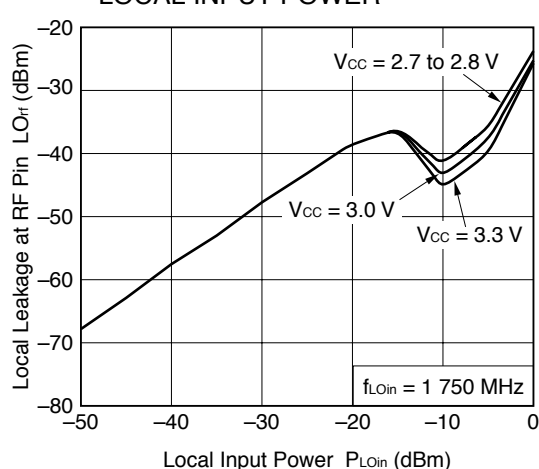
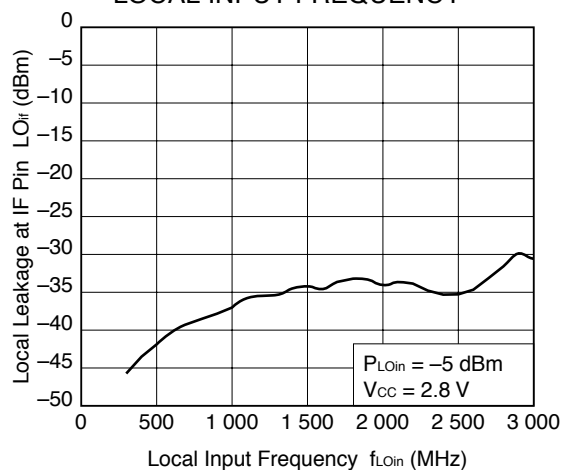
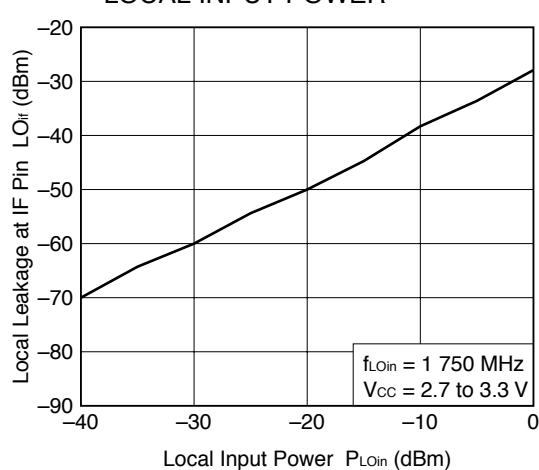
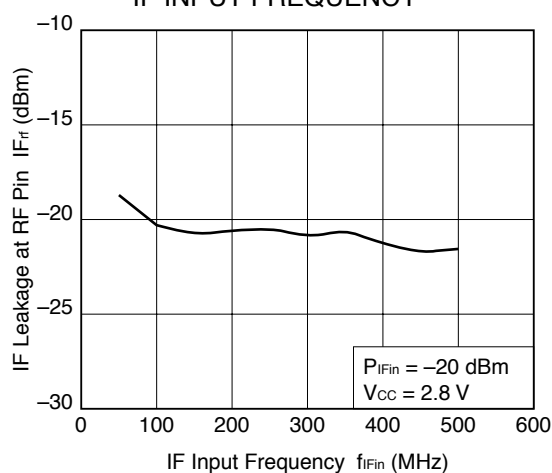
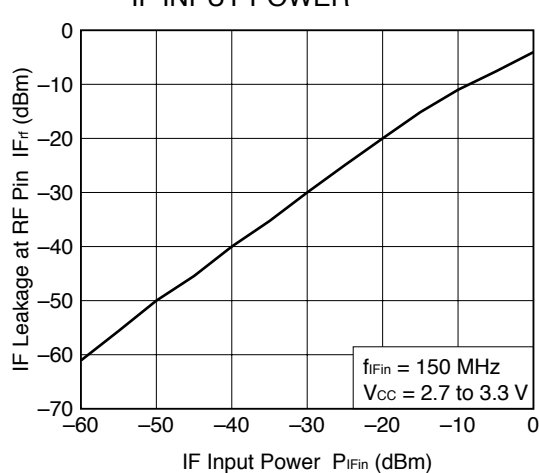
IF LEAKAGE AT RF PIN vs.
IF INPUT POWER



11.2 $f_{RFout} = 1.9$ GHzCONVERSION GAIN vs.
LOCAL INPUT POWERRF OUTPUT POWER vs.
IF INPUT POWERCONVERSION GAIN vs.
LOCAL INPUT POWERRF OUTPUT POWER vs.
IF INPUT POWER

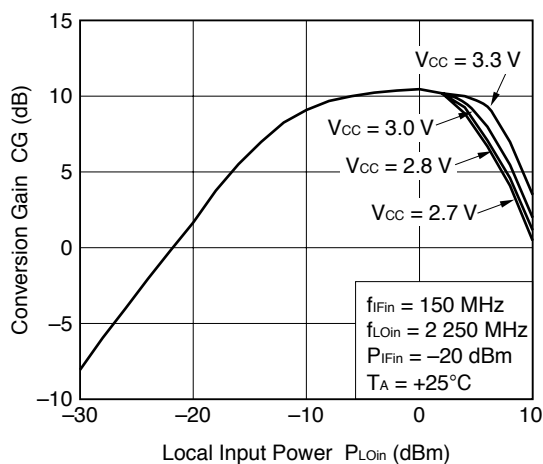




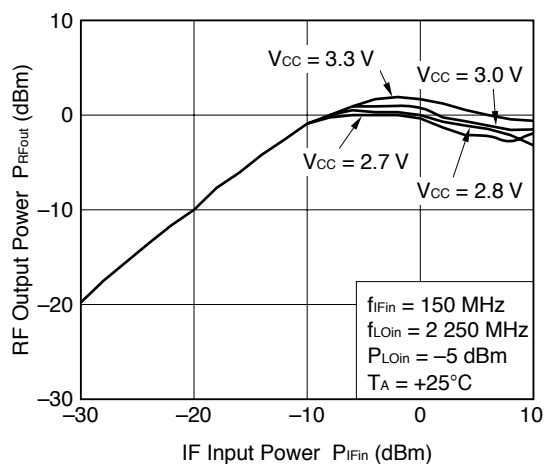
LOCAL LEAKAGE AT RF PIN vs.
LOCAL INPUT FREQUENCYLOCAL LEAKAGE AT RF PIN vs.
LOCAL INPUT POWERLOCAL LEAKAGE AT IF PIN vs.
LOCAL INPUT FREQUENCYLOCAL LEAKAGE AT IF PIN vs.
LOCAL INPUT POWERIF LEAKAGE AT RF PIN vs.
IF INPUT FREQUENCYIF LEAKAGE AT RF PIN vs.
IF INPUT POWER

11.3 $f_{RFout} = 2.4$ GHz

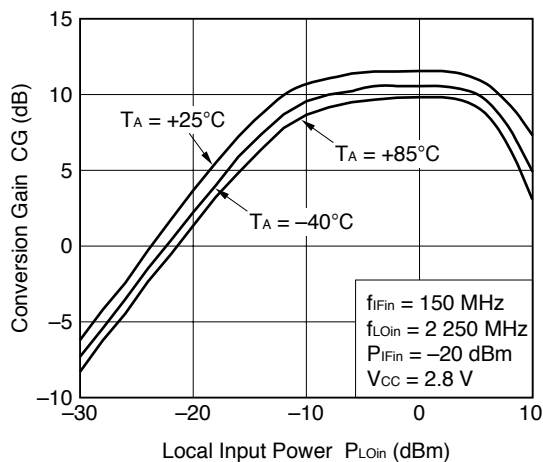
CONVERSION GAIN vs.
LOCAL INPUT POWER



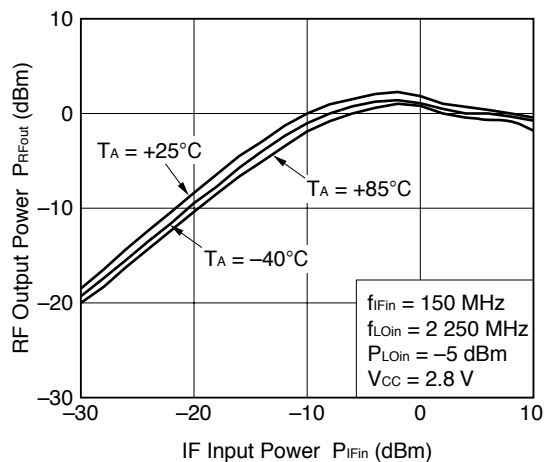
RF OUTPUT POWER vs.
IF INPUT POWER

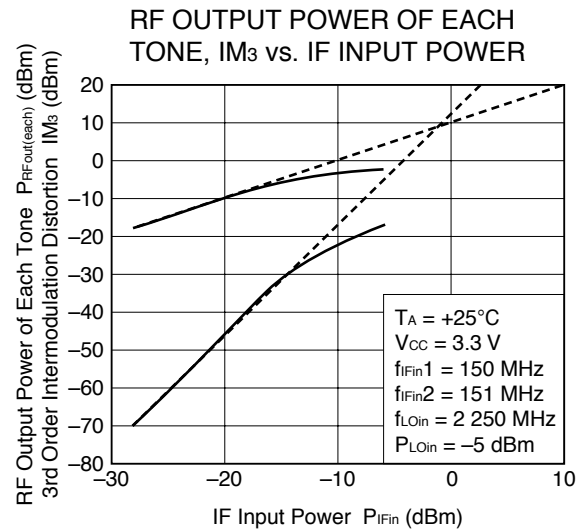
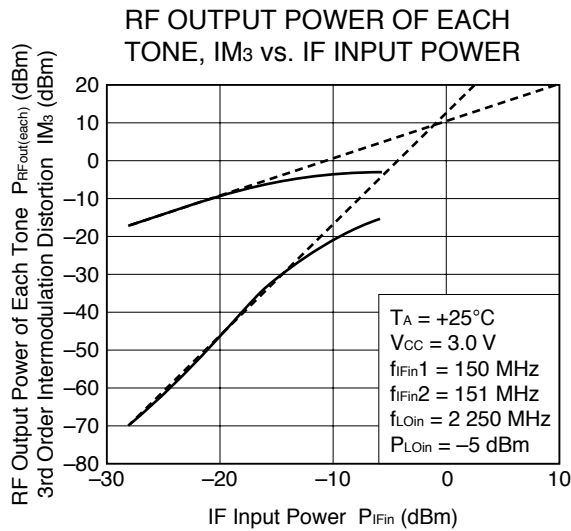
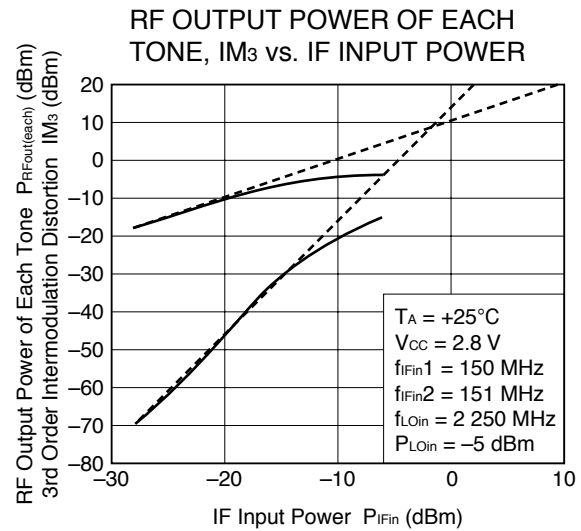
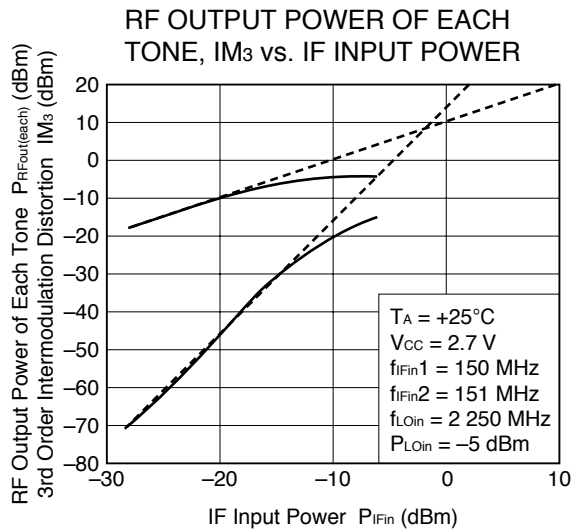


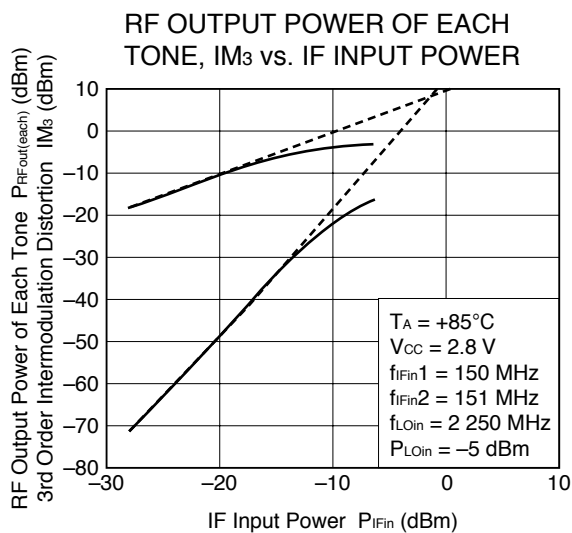
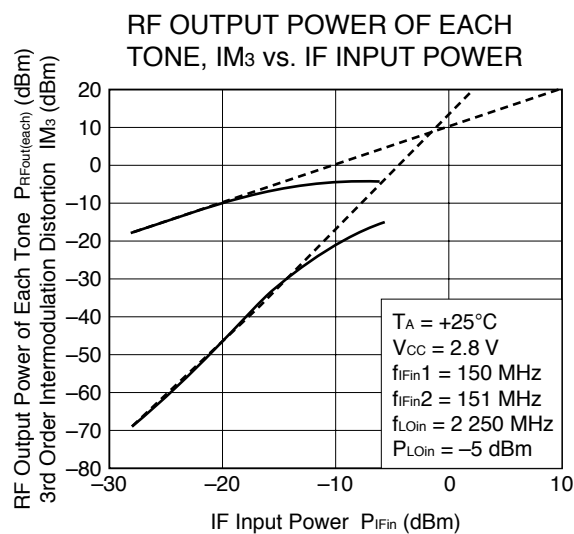
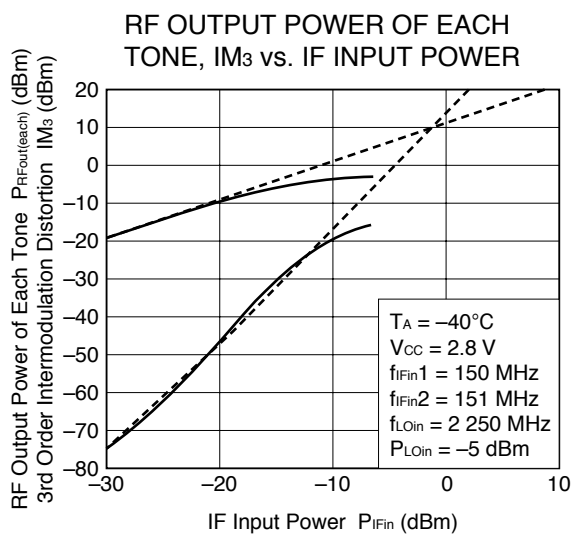
CONVERSION GAIN vs.
LOCAL INPUT POWER



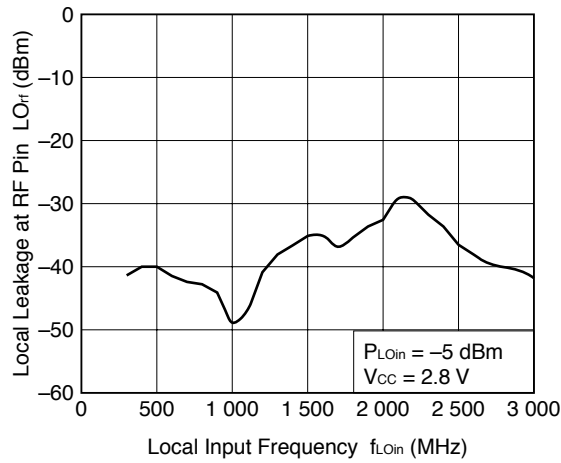
RF OUTPUT POWER vs.
IF INPUT POWER



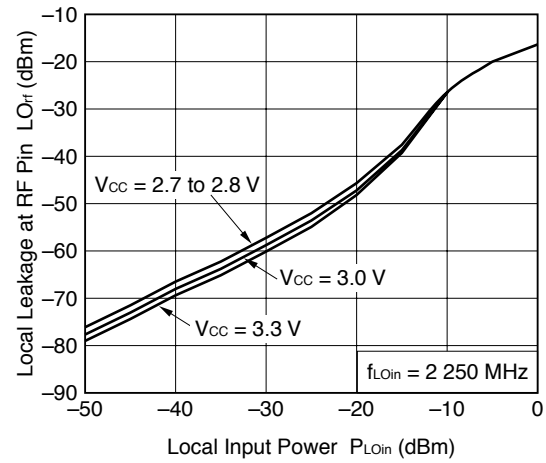




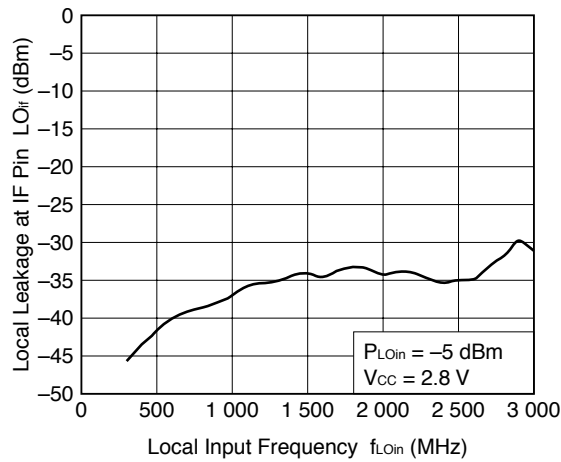
LOCAL LEAKAGE AT RF PIN vs.
LOCAL INPUT FREQUENCY



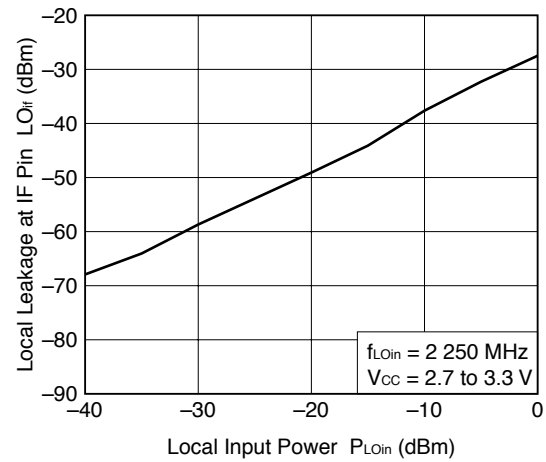
LOCAL LEAKAGE AT RF PIN vs.
LOCAL INPUT POWER



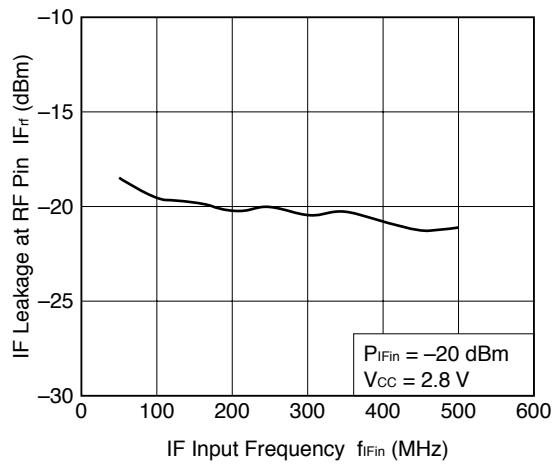
LOCAL LEAKAGE AT IF PIN vs.
LOCAL INPUT FREQUENCY



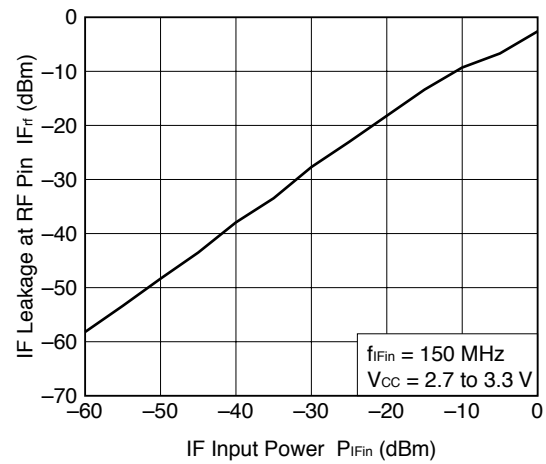
LOCAL LEAKAGE AT IF PIN vs.
LOCAL INPUT POWER



IF LEAKAGE AT RF PIN vs.
IF INPUT FREQUENCY



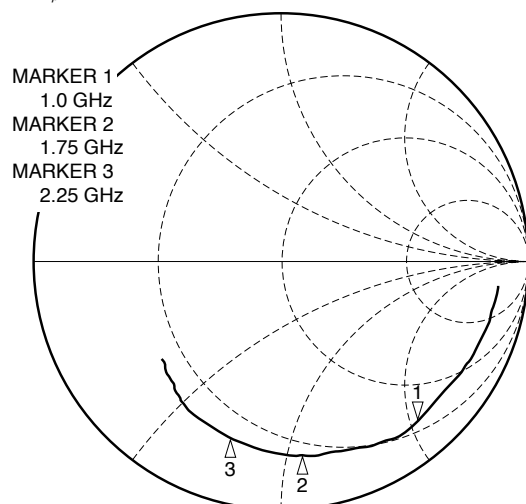
IF LEAKAGE AT RF PIN vs.
IF INPUT POWER



★ **12. S-PARAMETERS FOR EACH PORT ($V_{CC} = V_{RFout} = 2.8$ V)**
 (The parameters are monitored at DUT pins)

LO port

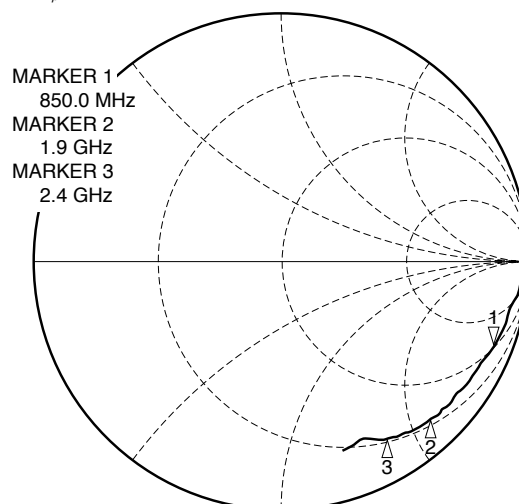
S_{11} Z
 REF 1.0 Units
 1 200.0 mUnits/
 ∇_{hp} 22.762 Ω -104.25 Ω



START 0.100000000 GHz
 STOP 3.100000000 GHz

RF port (without matching)

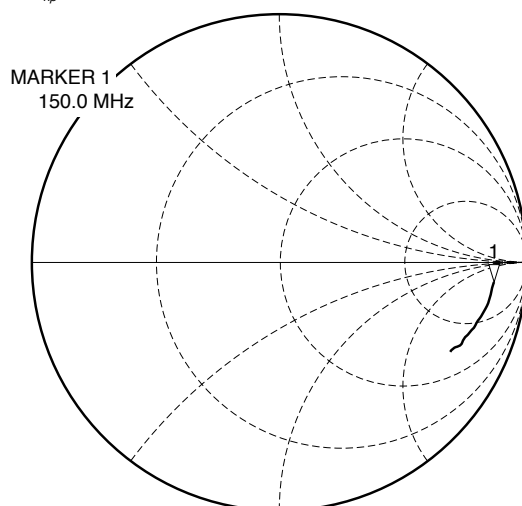
S_{22} Z
 REF 1.0 Units
 1 200.0 mUnits/
 ∇_{hp} 51.172 Ω -252.0 Ω



START 0.100000000 GHz
 STOP 3.100000000 GHz

IF port

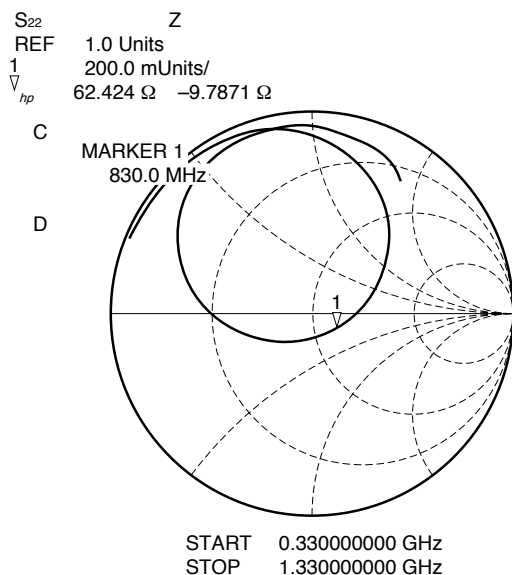
S_{11} Z
 REF 1.0 Units
 1 200.0 mUnits/
 ∇_{hp} 518.97 Ω -321.09 Ω



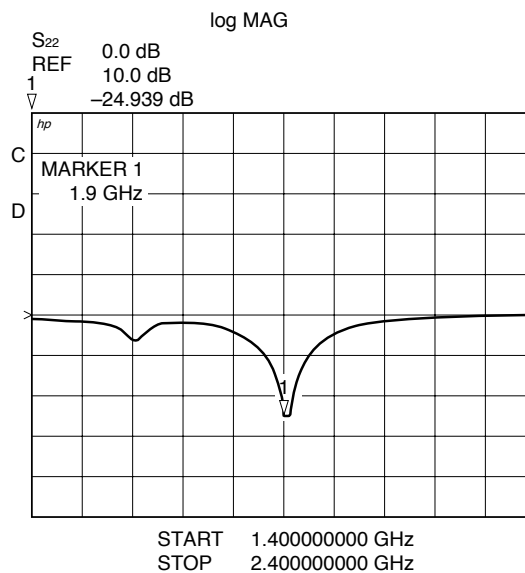
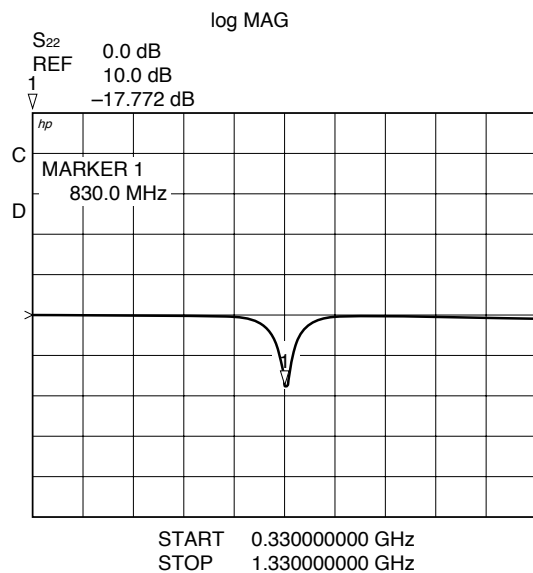
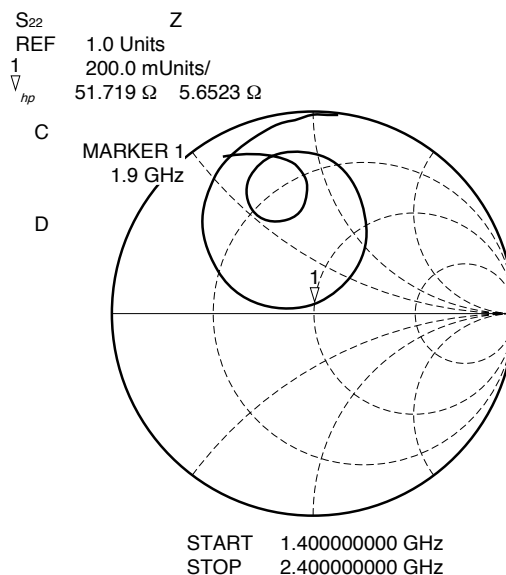
START 0.100000000 GHz
 STOP 1.000000000 GHz

★ 13. S-PARAMETERS FOR MATCHED RF OUTPUT ($V_{CC} = V_{RFout} = 2.8\text{ V}$)
 – ON EVALUATION BOARD – (S_{22} data are monitored at RF connector on board)

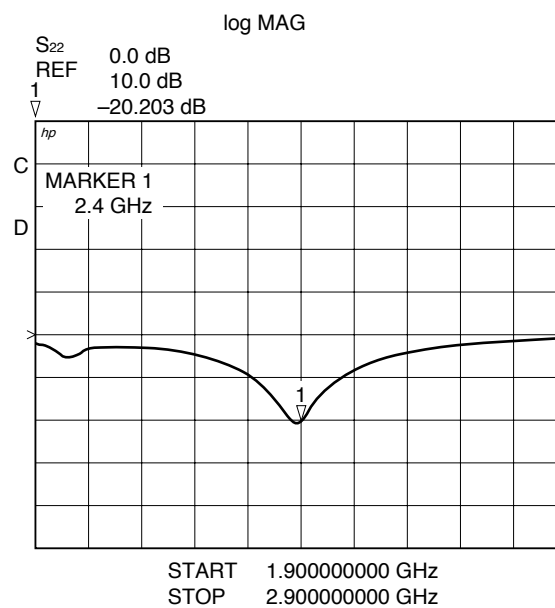
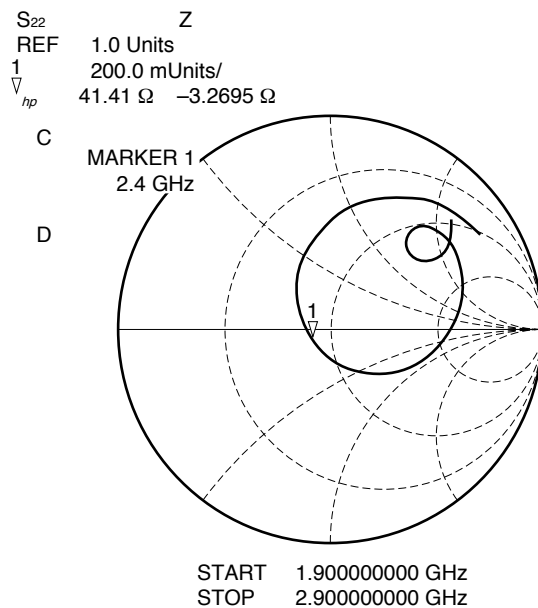
0.83 GHz (matched in test circuit 1)



1.9 GHz (matched in test circuit 2)

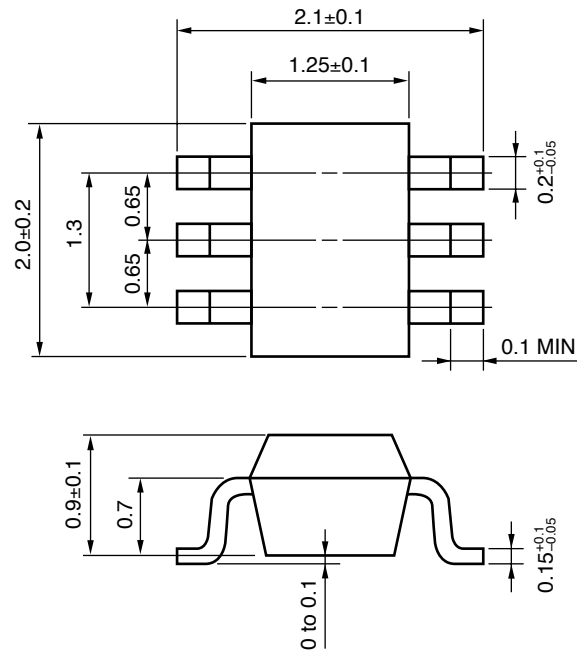


2.4 GHz (matched in test circuit 3)



14. PACKAGE DIMENSIONS

6-PIN SUPER MINIMOLD (UNIT: mm)



15. NOTE ON CORRECT USE

- (1) Observe precautions for handling because of electrostatic sensitive devices.
- (2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired oscillation).
- (3) Connect a bypass capacitor to the V_{CC} pin.
- (4) Connect a matching circuit to the RF output pin.
- (5) The DC cut capacitor must be each attached to the input and output pins.

16. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 3, Exposure limit: None ^{Note}	IR35-00-3
VPS	Package peak temperature: 215°C or below Time: 40 seconds or less (at 200°C) Count: 3, Exposure limit: None ^{Note}	VP15-00-3
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit: None ^{Note}	WS60-00-1
Partial Heating	Pin temperature: 300°C Time: 3 seconds or less (per side of device) Exposure limit: None ^{Note}	—

Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)**.

AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit www.ameya360.com

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com