

# 74LVT04

## 3.3 V Hex inverter

Rev. 2 — 28 April 2014

Product data sheet

### 1. General description

The 74LVT04 is a high-performance product designed for  $V_{CC}$  operation at 3.3 V.

The 74LVT04 provides six inverting buffers.

### 2. Features and benefits

- TTL input and output switching levels
- Latch-up protection
  - ◆ JESD78 class II exceeds 500 mA
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

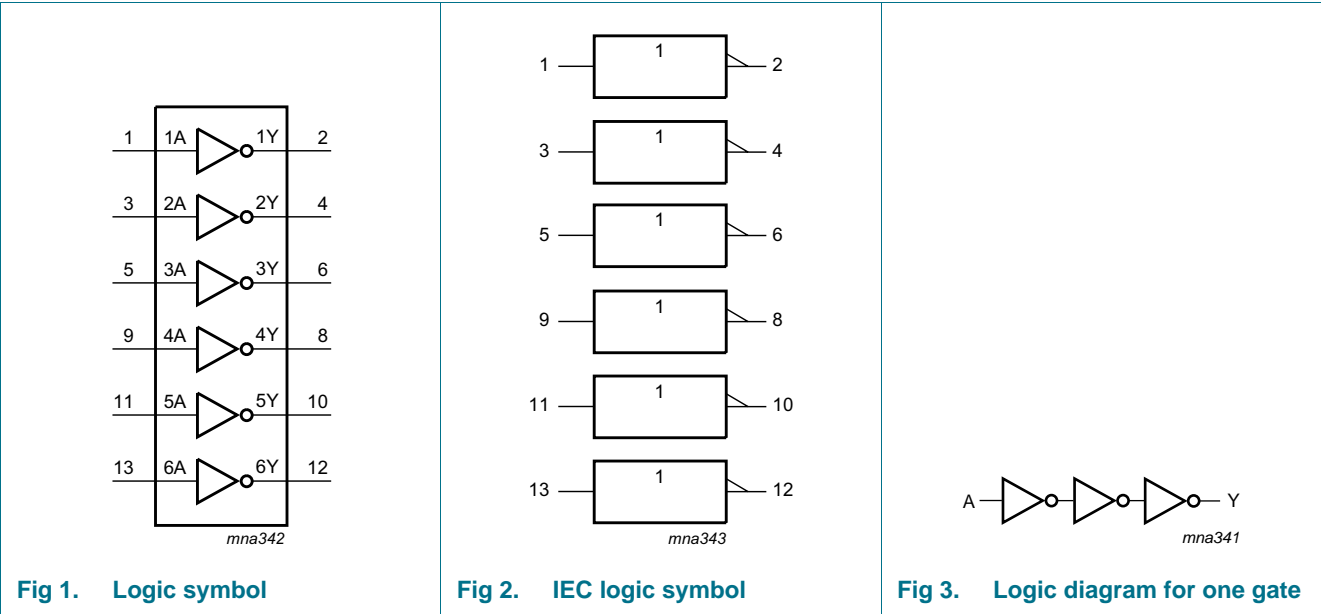
### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT04D	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVT04DB	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVT04PW	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

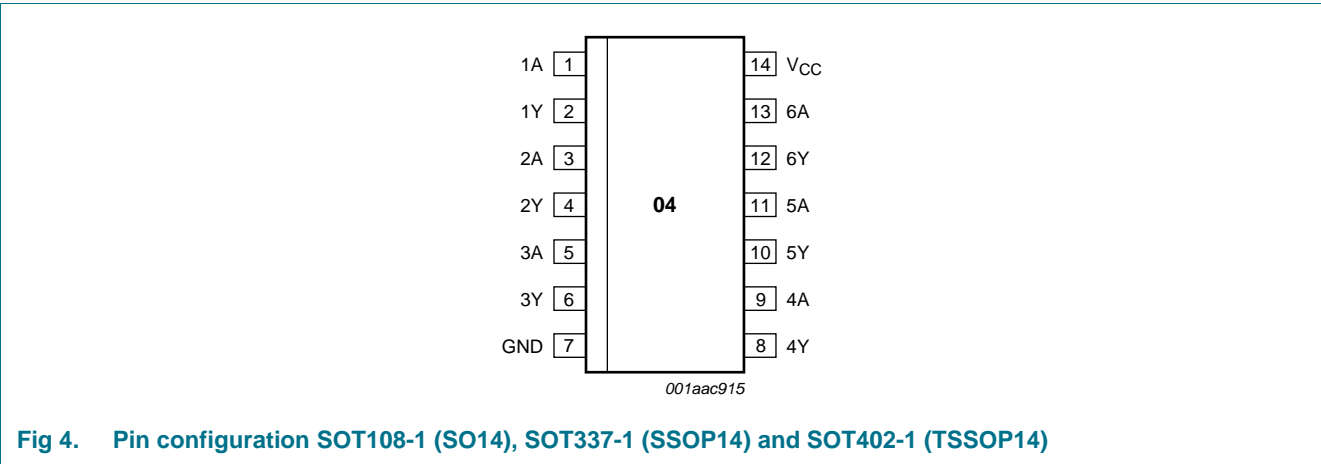


4. Functional diagram



5. Pinning information

5.1 Pinning



## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
nA	1, 3, 5, 9, 11, 13	data input
nY	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Input	Output
nA	nY
L	H
H	L

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		−0.5	+4.6	V
V <sub>I</sub>	input voltage		<sup>[1]</sup> −0.5	+7.0	V
V <sub>O</sub>	output voltage	output in OFF-state or HIGH-state	<sup>[1]</sup> −0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	−50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	−50	-	mA
I <sub>O</sub>	output current	output in LOW-state	-	64	mA
		output in HIGH-state	-	−32	mA
T <sub>stg</sub>	storage temperature		−65	+150	°C
T <sub>j</sub>	junction temperature		<sup>[2]</sup> -	150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = −40 °C to +85 °C	<sup>[3]</sup> -	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.

For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		2.7	3.6	V
$V_I$	input voltage		0	5.5	V
$V_{IH}$	HIGH-level input voltage		2.0	-	V
$V_{IL}$	LOW-level input voltage		-	0.8	V
$I_{OH}$	HIGH-level output current		-	-20	mA
$I_{OL}$	LOW-level output current		-	32	mA
$T_{amb}$	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
$V_{IK}$	input clamp voltage	$V_{CC} = 2.7\text{ V}$ ; $I_{IK} = -18\text{ mA}$	-	-	-1.2	V
$V_{OH}$	LOW-level input voltage	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$ ; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	-	-	V
		$V_{CC} = 2.7\text{ V}$ ; $I_{OH} = -6\text{ mA}$	2.4	-	-	V
		$V_{CC} = 3.0\text{ V}$ ; $I_{OH} = -20\text{ mA}$	2.0	-	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 2.7\text{ V}$ ; $I_{OL} = -100\text{ }\mu\text{A}$	-	-	0.2	V
		$V_{CC} = 2.7\text{ V}$ ; $I_{OL} = 24\text{ mA}$	-	-	0.5	V
		$V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 32\text{ mA}$	-	-	0.5	V
$I_I$	input leakage current	$V_{CC} = 0\text{ V or } 3.6\text{ V}$ ; $V_I = 5.5\text{ V}$	-	-	10	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}\text{ or GND}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{OFF}$	output off current	$V_{CC} = 0\text{ V}$ ; $V_I\text{ or } V_O = 0\text{ V to } 4.5\text{ V}$	-	-	$\pm 100$	$\mu\text{A}$
$I_{CCH}$	quiescent supply current	$V_{CC} = 3.6\text{ V}$ ; outputs HIGH; $V_I = \text{GND or } V_{CC}$ ; $I_O = 0\text{ V}$	-	-	0.02	mA
$I_{CCL}$	quiescent supply current	$V_{CC} = 3.6\text{ V}$ ; outputs LOW; $V_I = \text{GND or } V_{CC}$ ; $I_O = 0\text{ V}$	-	1.5	3	mA
$\Delta I_{CC}$	additional supply current per input pin <sup>[2]</sup>	$V_{CC} = 3\text{ V to } 3.6\text{ V}$ ; one input at $V_{CC} - 0.6\text{ V}$ ; other inputs at $V_{CC}\text{ or GND}$	-	-	0.2	$\mu\text{A}$
$C_I$	input capacitance	$V_I = 3\text{ V or } 0\text{ V}$	-	3	-	pF

[1] All typical values are at  $V_{CC} = 3.3\text{ V}$  and  $T_{amb} = 25^\circ\text{C}$ .

[2] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

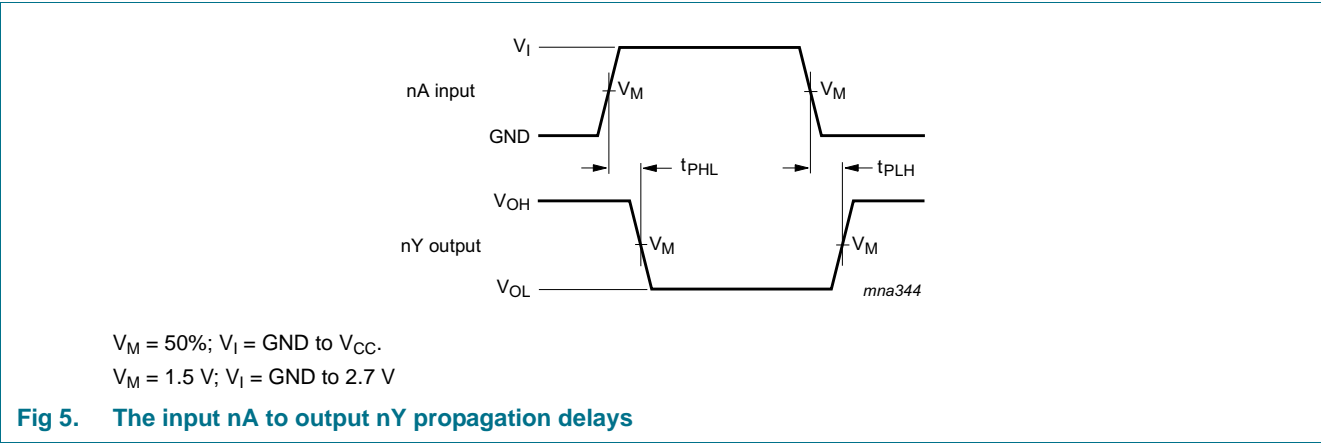
10. Dynamic characteristics

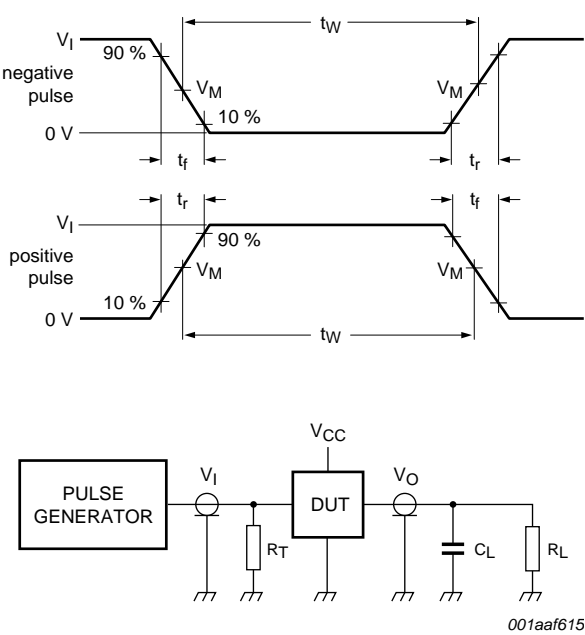
Table 7. Dynamic characteristics  
GND = 0 V; for test circuit, see Figure 6.

Symbol	Parameter	Conditions	−40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
t <sub>PLH</sub>	LOW to OFF-state propagation delay	nA to nY; see Figure 5				
		V <sub>CC</sub> = 2.7 V	-	-	4.7	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	1.0	2.6	3.9	ns
t <sub>PHL</sub>	OFF-state to LOW propagation delay	nA to nY; see Figure 5				ns
		V <sub>CC</sub> = 2.7 V	-	-	3.2	
		V <sub>CC</sub> = 3.3 V ± 0.3 V	1.0	2.5	3.5	ns

[1] All typical values are at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25°C.

11. Waveforms





Test data is given in [Table 8](#).  
Definitions test circuit:  
 $R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.  
 $C_L$  = load capacitance including jig and probe capacitance.  
 $R_L$  = Load resistance.

Fig 6. Test circuit for measuring switching times

Table 8. Test data

Input				Load	
$V_I$	$f_i$	$t_W$	$t_r, t_f$	$C_L$	$R_L$
2.7 V	$\leq 10$ MHz	500 ns	$\leq 2.5$ ns	50 pF	500 $\Omega$

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

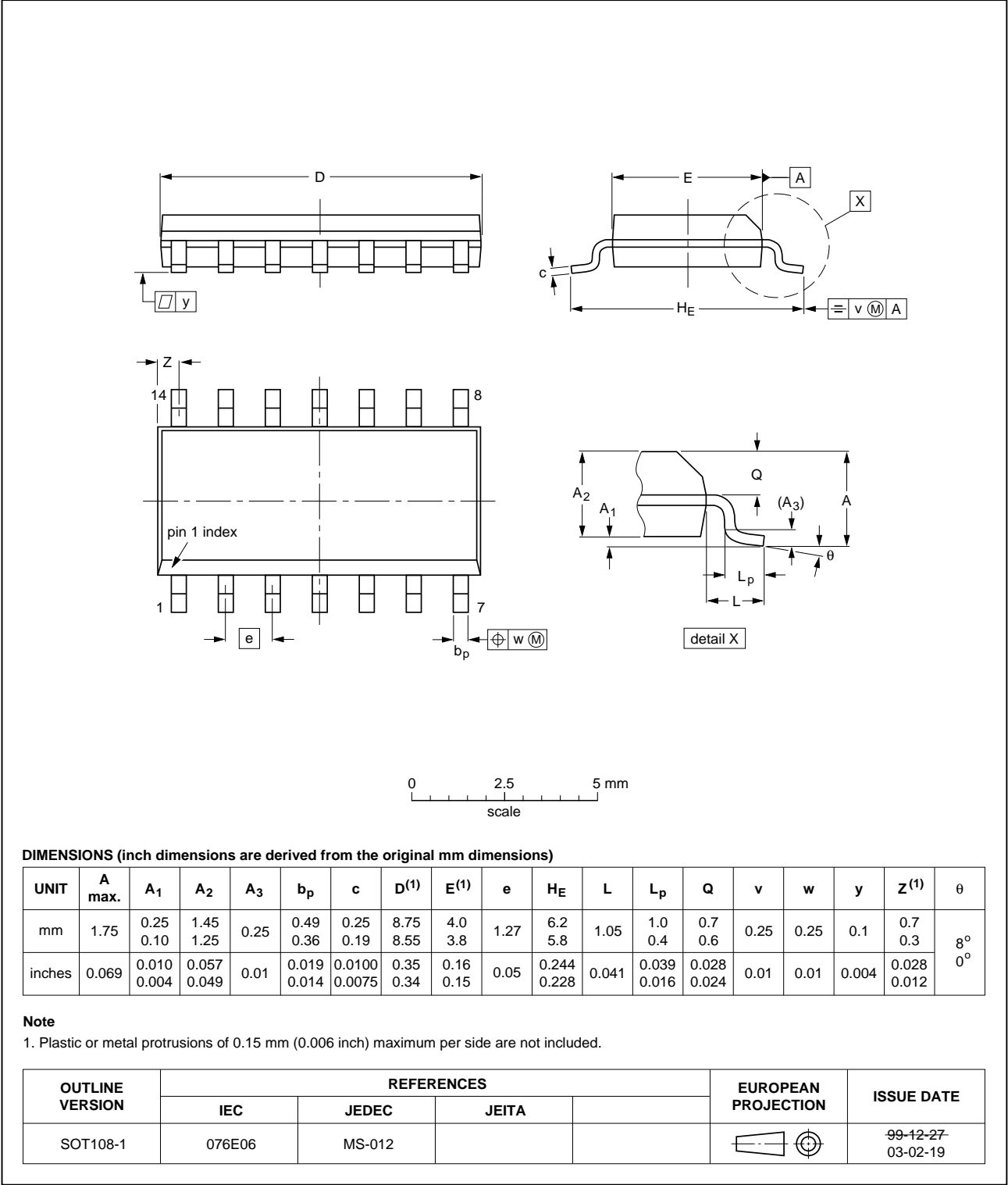


Fig 7. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

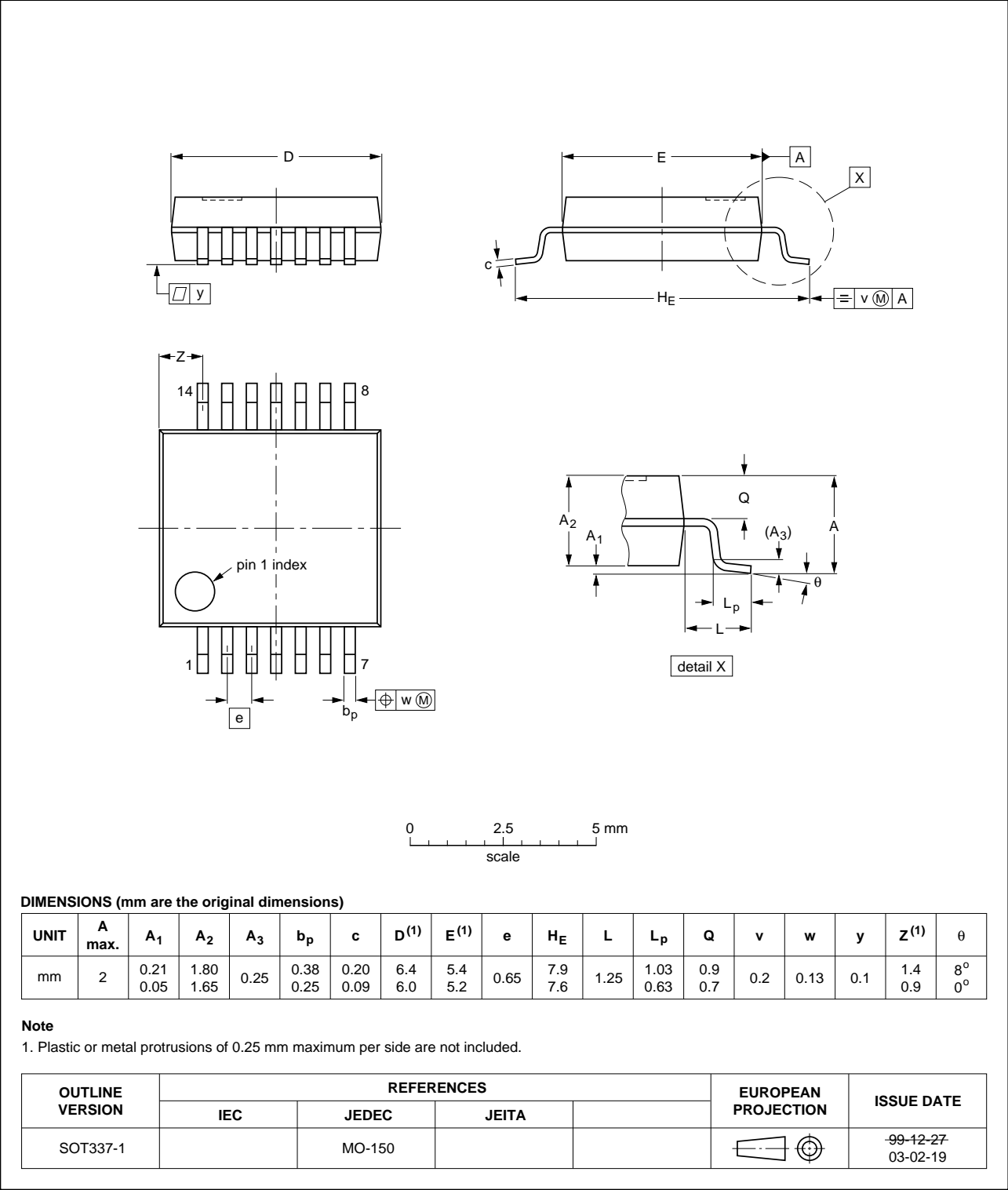


Fig 8. Package outline SOT337-1 (SSOP14)



TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

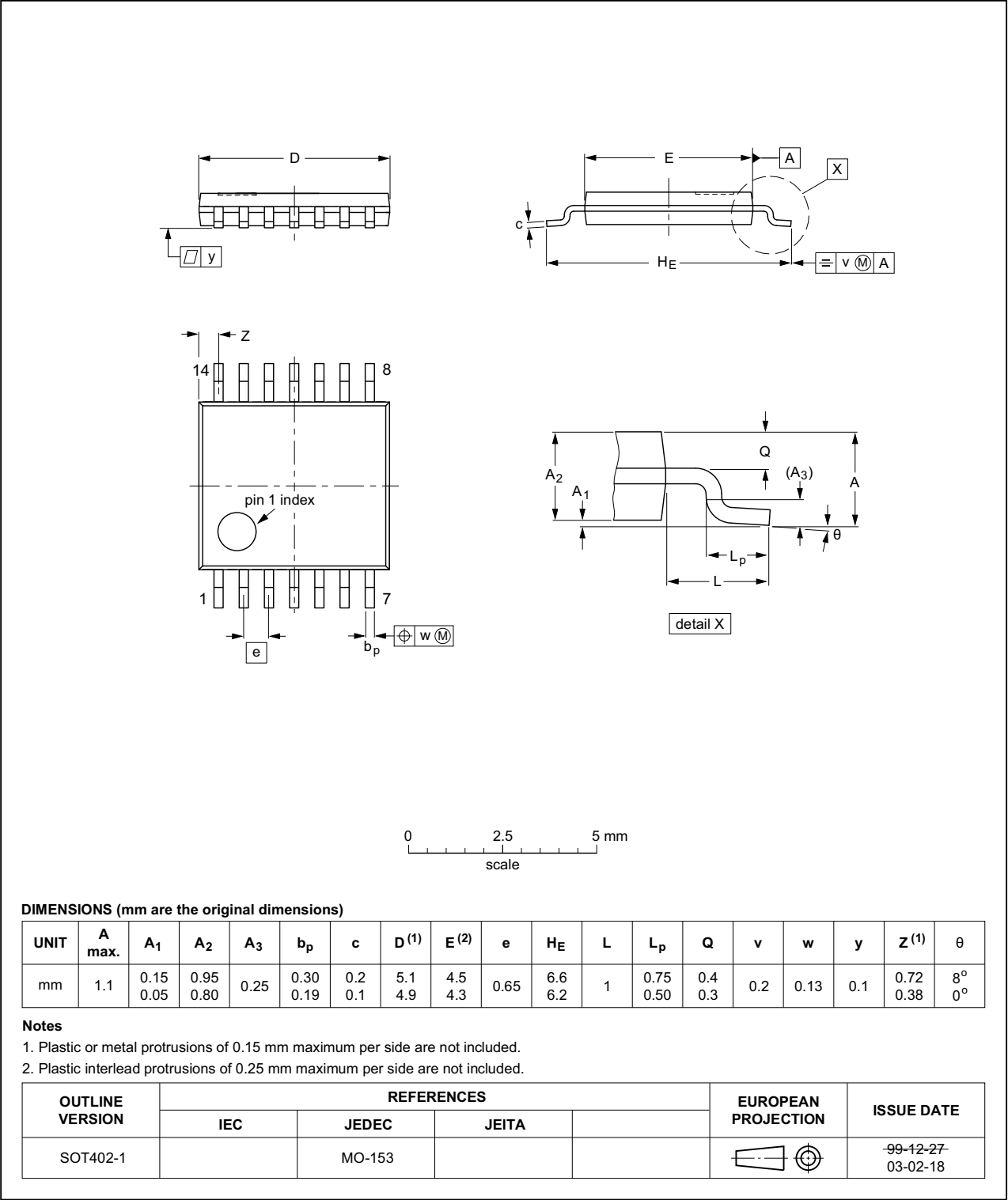


Fig 9. Package outline SOT402-1 (TSSOP14)

## 13. Abbreviations

Table 9. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model

## 14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT04 v.2	20140428	Product data sheet	-	74LVT04_1
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li>Imported the data sheet into the latest template</li></ul>			
74LVT04_1	19960828	Product specification	-	-

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### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 17. Contents

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<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>1</b>
<b>4</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>2</b>
5.1	Pinning .....	2
5.2	Pin description .....	3
<b>6</b>	<b>Functional description</b> .....	<b>3</b>
<b>7</b>	<b>Limiting values</b> .....	<b>3</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>4</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>4</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>5</b>
<b>11</b>	<b>Waveforms</b> .....	<b>5</b>
<b>12</b>	<b>Package outline</b> .....	<b>7</b>
<b>13</b>	<b>Abbreviations</b> .....	<b>10</b>
<b>14</b>	<b>Revision history</b> .....	<b>10</b>
<b>15</b>	<b>Legal information</b> .....	<b>11</b>
15.1	Data sheet status .....	11
15.2	Definitions .....	11
15.3	Disclaimers .....	11
15.4	Trademarks .....	12
<b>16</b>	<b>Contact information</b> .....	<b>12</b>
<b>17</b>	<b>Contents</b> .....	<b>13</b>

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