AS1372

350mA Dual Rail Linear Regulator

1 General Description

The AS1372 is a Dual Supply Rail Linear Regulator designed for powering very-low voltage circuits from a single Li-Ion cell or 3 cell NiMH batteries. In the typical post regulation application VBIAS is directly connected to the battery (range 2.5V...5.5V) and VIN is supplied by the output voltage of a host DC-DC Converter (range 0.7V...4.5V).

The device offers excellent dropout and transient features combined with very low quiescent currents. In shutdown (Enable pin pulled low), the device turns off and reduces quiescent current consumption to 10nA (typ) at both VBIAS and VIN terminals.

In shutdown, a 100ohms (typ) discharge path is connected between output and ground to provide rapid discharge of the overall load capacitance connected to the AS1372 output terminal. Auto-discharge minimizes the possibility that VOUT > VIN during shutdown. When VOUT > VIN, reverse current flows through the inherent body diode of the N-channel series pass transistor.

The AS1372 also features internal protection against over-temperature, over-current and under-voltage conditions.

The device is available in a tiny 5-bump CS-WLP package and is qualified for operation over the -40ºC to +85ºC temperature range.

The device is available in fixed output voltages from 0.5V up to 2.2V in 100mV steps (50mV from 0.5V to 1.1V). See Ordering Information on page 18.

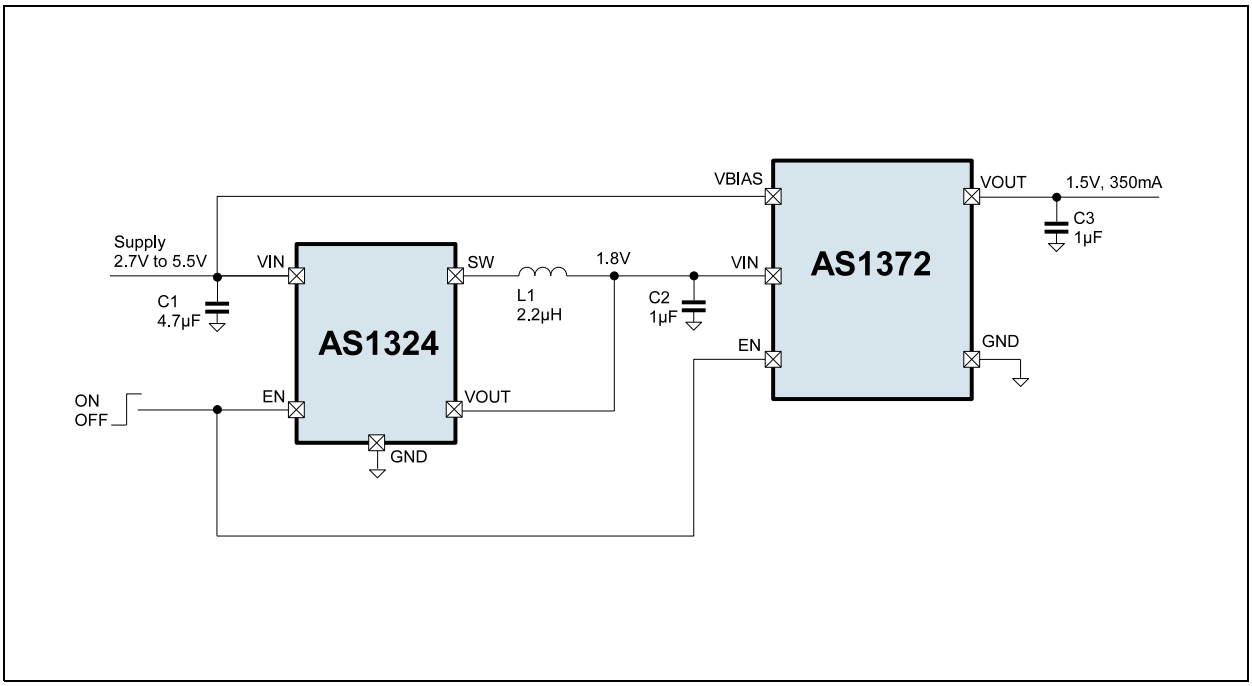
2 Key Features

- Input Voltage: 0.7V to 4.5V
- Bias Supply Voltage: 2.5V to 5.5V
- Output Voltage: 0.5V to 2.2V in 100mV steps
- Output Voltage Accuracy: ±1.5%
- Dropout Voltage 135mV @ 350mA load
- Max. Output Current: 350mA
- Load Transient Response: ±15mV (typ)
- Superior Efficiency
- Low Shutdown Current: 10nA
- High PSRR: >80dB @ 10Hz-1kHz, 60db @100kHz
- Noise Voltage: 50µ VRMS from 10Hz to 100kHz
- Integrated Overtemperature / Overcurrent Protection
- Chip Enable Input
- Operating Temperature Range: -40ºC to +85ºC
- 5-bumps CS-WLP Package

3 Applications

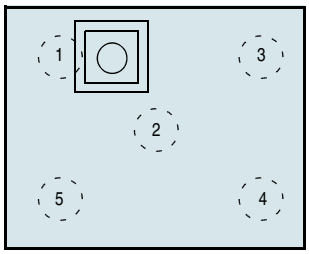
The devices are ideal for powering cordless and mobile phones, MP3 players, PDAs, hand-held computers, digital cameras, and any other hand-held and/or battery-powered device.

Figure 1. AS1372 - Typical Application Diagram



4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	VOUT	**Regulated Output Voltage**. Bypass this pin with a capacitor to GND.
2	GND	**Ground.**
3	EN	**Enable.** Pull this pin to low to disable the device. This pin has an internal 1.6MΩ (typ) pull-down resistor.
4	VBIAS	**Bias Supply Voltage.** 2.5V to 5.5V, Bypass this pin with a capacitor to GND.
5	VIN	**Unregulated Input Voltage**. 0.7V to 4.5V, $V_{IN} \leq V_{BIAS}$, Bypass this pin with a capacitor to GND.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Electrical Parameters				
VIN, VBIAS and EN to GND	-0.3	+6.5	V	VIN < VBIAS or equal in operating conditions
VOUT to GND	-0.3	V_{IN} + 0.3	V	
Output Short-Circuit Duration		Indefinite		
Latch-Up	-100	+100	mA	*JEDEC 78*
Electrostatic Discharge				
Electrostatic discharge (ESD)	2		kV	*HBM MIL-Std. 883E 3015.7* methods
Temperature Ranges and Storage Conditions				
Thermal Resistance θ_{JA}	95		ºC/W	Junction-to-ambient thermal resistance is very dependent on application and board-layout. In situations where high maximum power dissipation exists, special attention must be paid to thermal dissipation during board design.
Operating Temperature Range	-40	+85	ºC	
Storage Temperature Range	-65	+150	ºC	
Junction Temperature		+125	ºC	
Package Body Temperature	+260		ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/ JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed by production tests or SQC (Statistical Quality Control) methods.

V_{IN} = V_{OUT} + 0.2V, V_{BIAS} = V_{OUT} + 1.5V (or 2.5V whichever is larger), EN = V_{BIAS}, C_{IN} = C_{OUT} = C_{BIAS} = 1µF, T_{AMB} = -40ºC to +85ºC, Typical values are at T_{AMB} = +25ºC unless otherwise specified).

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage	$V_{IN} \leq V_{BIAS}$	0.7		4.5	V
V_{BIAS}	Bias Supply Voltage		2.5		5.5	V
V_{OUT}	Output Voltage	Available in 50mV or 100mV steps (see Ordering Information on page 18)	0.5		2.2	V
$V_{OUT(NOM)}$ - V_{OUT}	Output Voltage Accuracy V_{OUT} > 1.2V	I_{OUT} = 100µA	-1.5		+1.5	%
		I_{OUT} = 100µA to 350mA, V_{IN} = $V_{OUT(NOM)}$+0.2V to 4.5V, V_{BIAS} = $V_{OUT(NOM)}$+1.5V to 5.5V	-2		+2	
	Output Voltage Accuracy $V_{OUT} \leq$ 1.2V	I_{OUT} = 100µA	-2		+2	%
		I_{OUT} = 100µA to 350mA, V_{IN} = $V_{OUT(NOM)}$+0.2V to 4.5V, V_{BIAS} = $V_{OUT(NOM)}$+1.5V to 5.5V	-2.5		+2.5	
ΔV_{OUT} / ΔV_{IN}	Line Regulation V_{IN}	V_{IN} = $V_{OUT(NOM)}$+0.2V to 4.5V, V_{BIAS} = 5.5V, I_{OUT} = 100µA		40		µV/V
ΔV_{OUT} / ΔV_{BIAS}	Line Regulation V_{BIAS}	V_{BIAS} = $V_{OUT(NOM)}$+1.5V to 5.5V, I_{OUT} = 100µA		100		µV/V
ΔV_{LDR}	Load Regulation	I_{OUT} = 1mA to 350mA		6		µV/mA
I_{OUT}	Output Current[1]		350			mA
I_{LIM}	Current Limit			500		mA
V_{DROP} -V_{IN}	Output Voltage Dropout V_{IN}	V_{BIAS} = V_{OUT} + 1.5V, I_{OUT} = 350mA		135		mV
		V_{BIAS} = V_{OUT} + 1.8V, I_{OUT} = 350mA		115		
		V_{BIAS} = 5.5V, I_{OUT} = 350mA		110		
V_{DROP} - V_{BIAS}	Output Voltage Dropout V_{BIAS}	I_{OUT} = 100mA		1.1	1.5	V
E_N	Output Voltage Noise	$V_{OUT} \leq$ 1.2V, f = 10Hz to 100kHz		50		µV_{RMS}
PSRR -V_{IN}	Power-Supply Rejection Ratio Sine modulated V_{IN}	f = 100Hz		85		dB
		f = 1kHz		80		
		f = 10kHz		70		
		f = 100kHz		60		
PSRR - V_{BIAS}	Power-Supply Rejection Ratio Sine modulated V_{BIAS}	f = 100Hz		75		dB
		f = 1kHz		60		
		f = 10kHz		50		
		f = 100kHz		50		
I_{Q_VBIAS}	Quiescent Current into V_{BIAS}			40	75	µA
I_{Q_VIN}	Quiescent Current into V_{IN}	I_{OUT} = 0mA		6.5	10	

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{SHDN - VBIAS}$	Shutdown Current into V_{BIAS}	V_{EN} = 0V		10		nA
$I_{SHDN - VIN}$	Shutdown Current into V_{IN}			10		
Logic Levels						
V_{IH}	Enable Input Threshold		1			V
V_{IL}					0.4	
I_{EN}	Enable Input Bias Current	EN = GND		0.01		nA
Thermal Protection						
T_{SHDN}	Thermal Shutdown Temperature			150		ºC
ΔT_{SHDN}	Thermal Shutdown Hysteresis			25		ºC
Transient Characteristics						
ΔV_{OUT}	Dynamic Load Transient Response	Pulsed I_{LOAD} from 0mA to 300mA in 10µs rise time		15		mV
t_{ON}	Exit Delay from Shutdown	$V_{OUT} \leq$ 1.2V, setting to 95%		70		µs
C_{OUT}	Output Capacitor	Load Capacitor Range	1		10	µF
		Maximum ESR Load	1		500	mΩ

1. Guaranteed by design

7 Typical Operating Characteristics

VIN = 1.2V, VBIAS = 2.5V, VOUT = 1.0V, EN = VBIAS, CIN = COUT = CBIAS = 1µF, TAMB = -40ºC to +85ºC, Typical Values are at TAMB = +25ºC (unless otherwise specified).

Figure 3. Bias Supply Current vs. Bias Supply Voltage

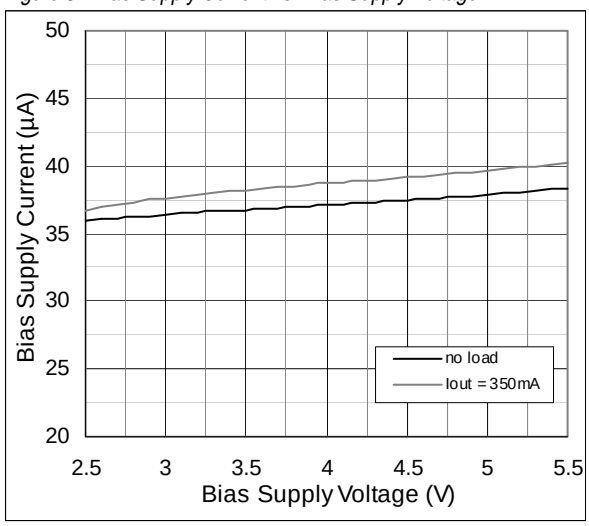


Figure 4. Bias Supply Current vs. Bias Supply Voltage

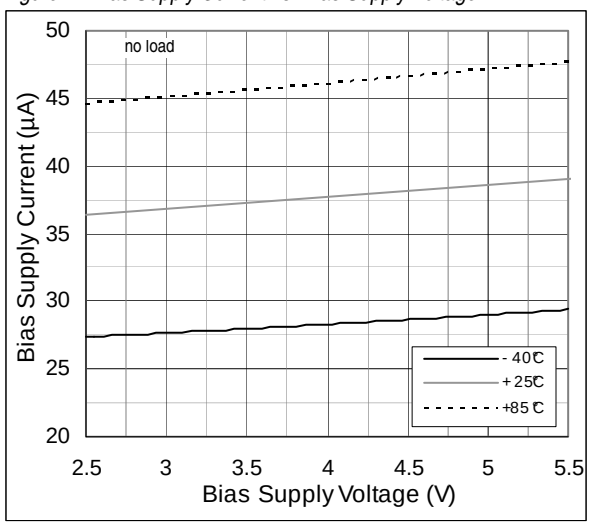


Figure 5. Ground Current vs. VIN; VBIAS = 5.5V

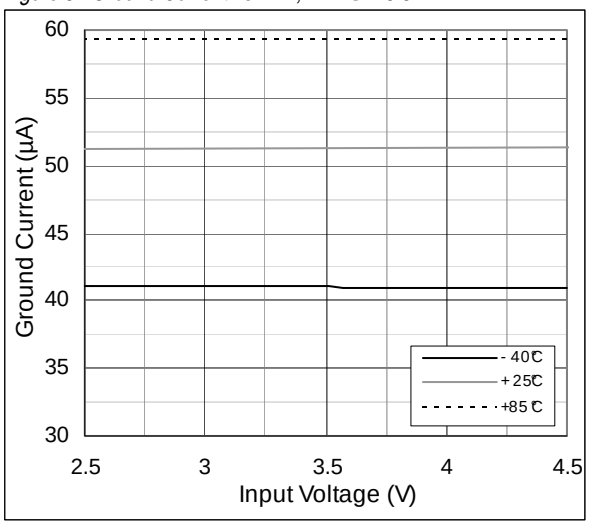


Figure 6. Ground Current vs. VIN / VBIAS;

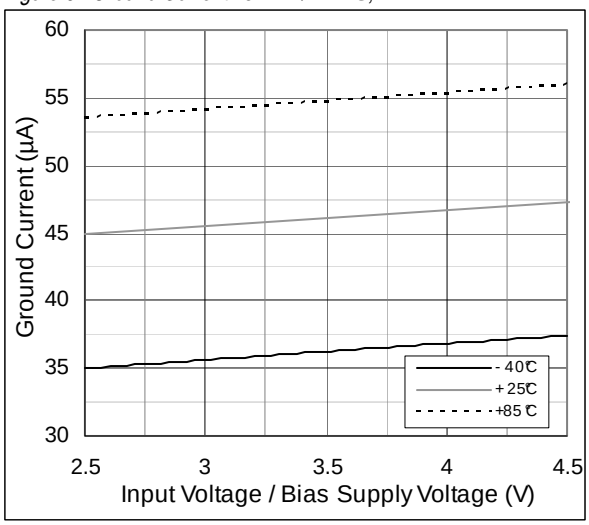


Figure 7. Ground Current vs. Bias Supply Voltage

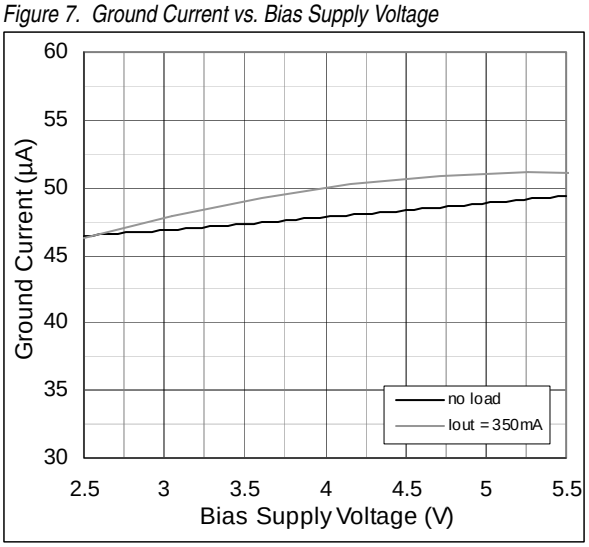


Figure 8. Ground Current vs. Load Current

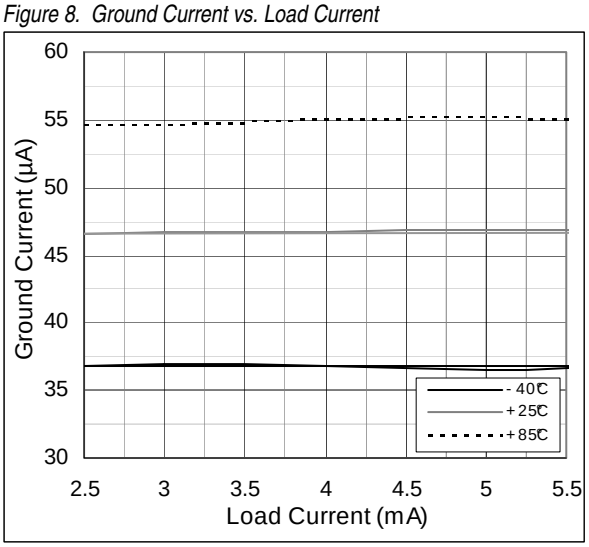


Figure 9. PSRR V_{IN}; V_{IN} = 3V_{DC} + 250mV_{pk}

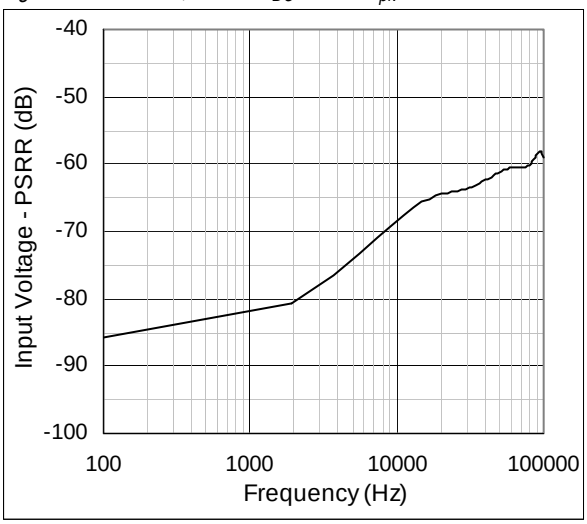


Figure 10. PSRR V_{BIAS}; V_{BIAS} = 3.5V_{DC} + 500mV_{pk}

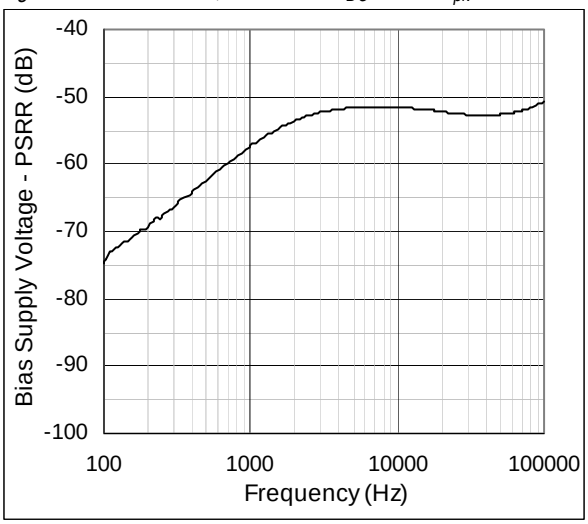


Figure 11. Line Regulation: V_{OUT} vs. V_{IN}; V_{BIAS} = 5.5V

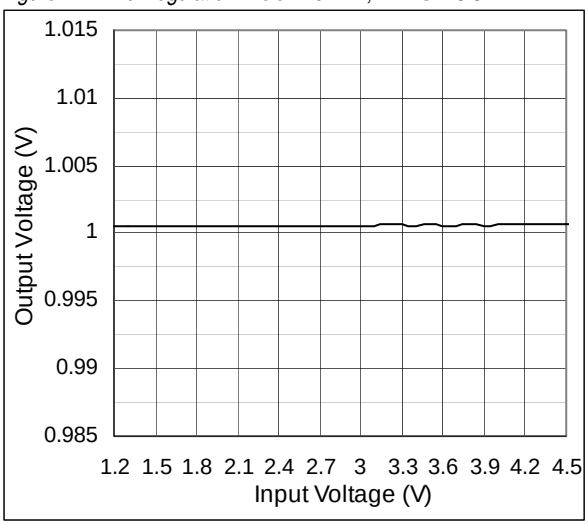


Figure 12. Line Regulation: V_{OUT} vs. V_{BIAS}

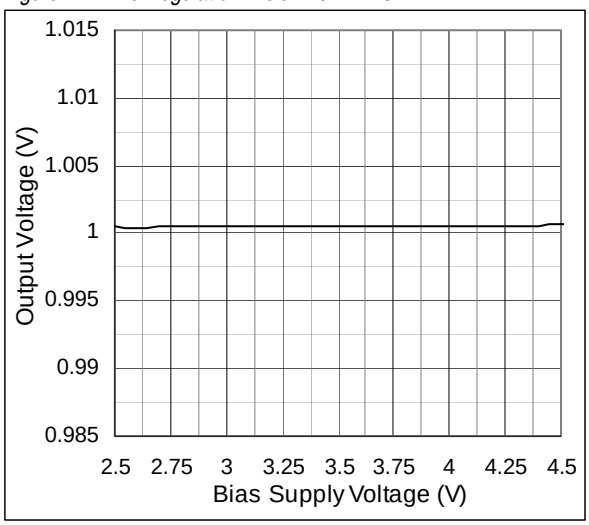


Figure 13. Load Regulation: V_{OUT} vs. I_{OUT}

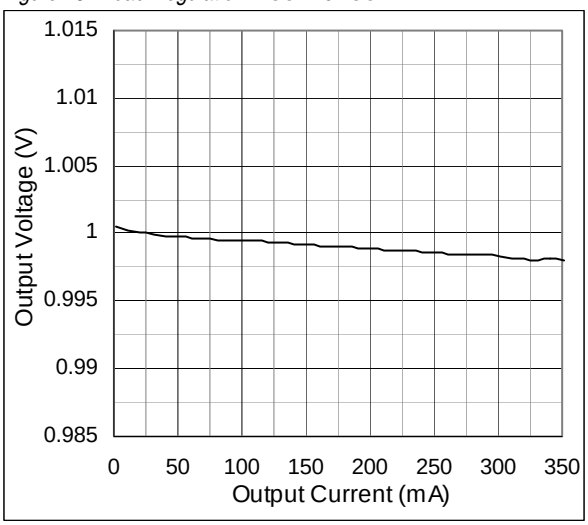


Figure 14. Output Voltage vs. Temperature; I_{OUT} = 1mA

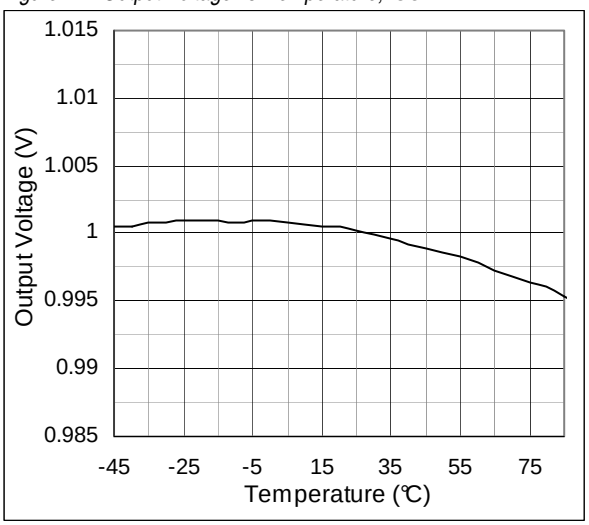


Figure 15. Dropout V_{IN} vs. Temp.; I_{OUT} = 350mA

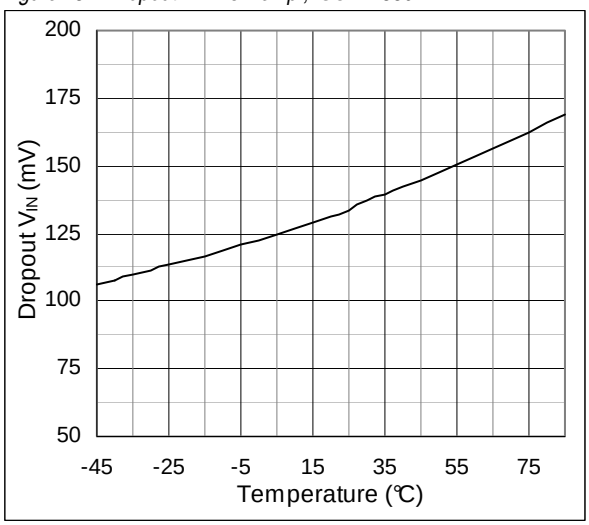


Figure 16. Enable Start-up

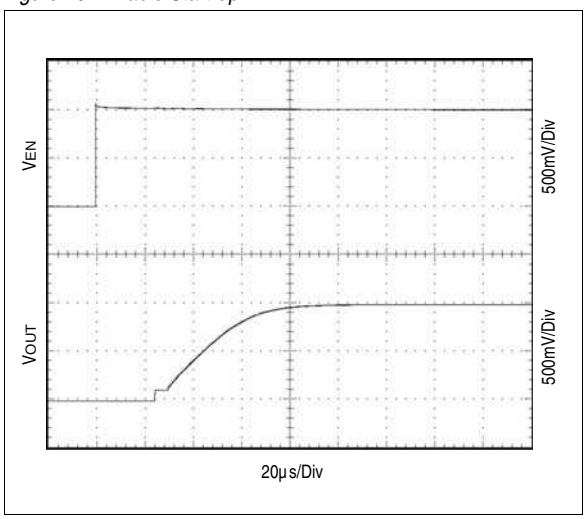


Figure 17. Line Transient Response; I_{OUT} = 350mA

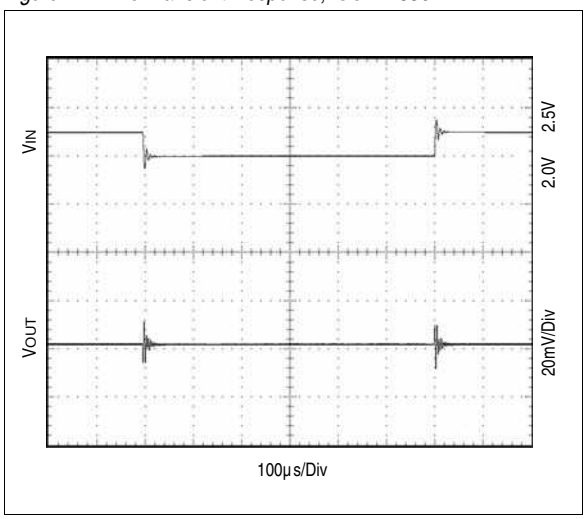
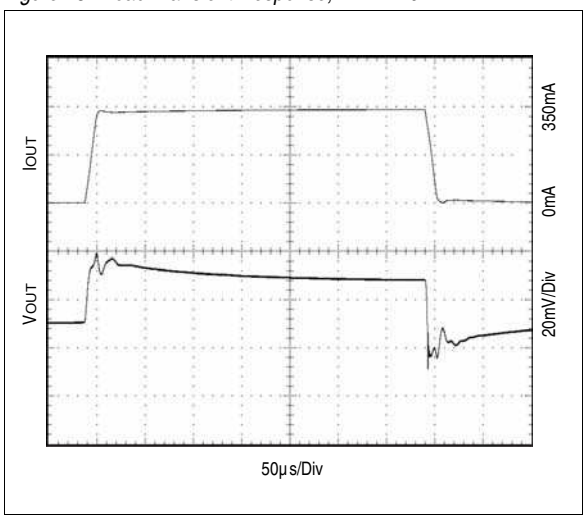


Figure 18. Load Transient Response; V_{IN} = 2.0V



8 Detailed Description

The AS1372 is a low-dropout, low-quiescent-current linear regulator intended for LDO regulator applications where output current load requirements range from no load to 350mA. All devices come with fixed output voltage from 0.5V to 2.2V (see Ordering Information on page 18).

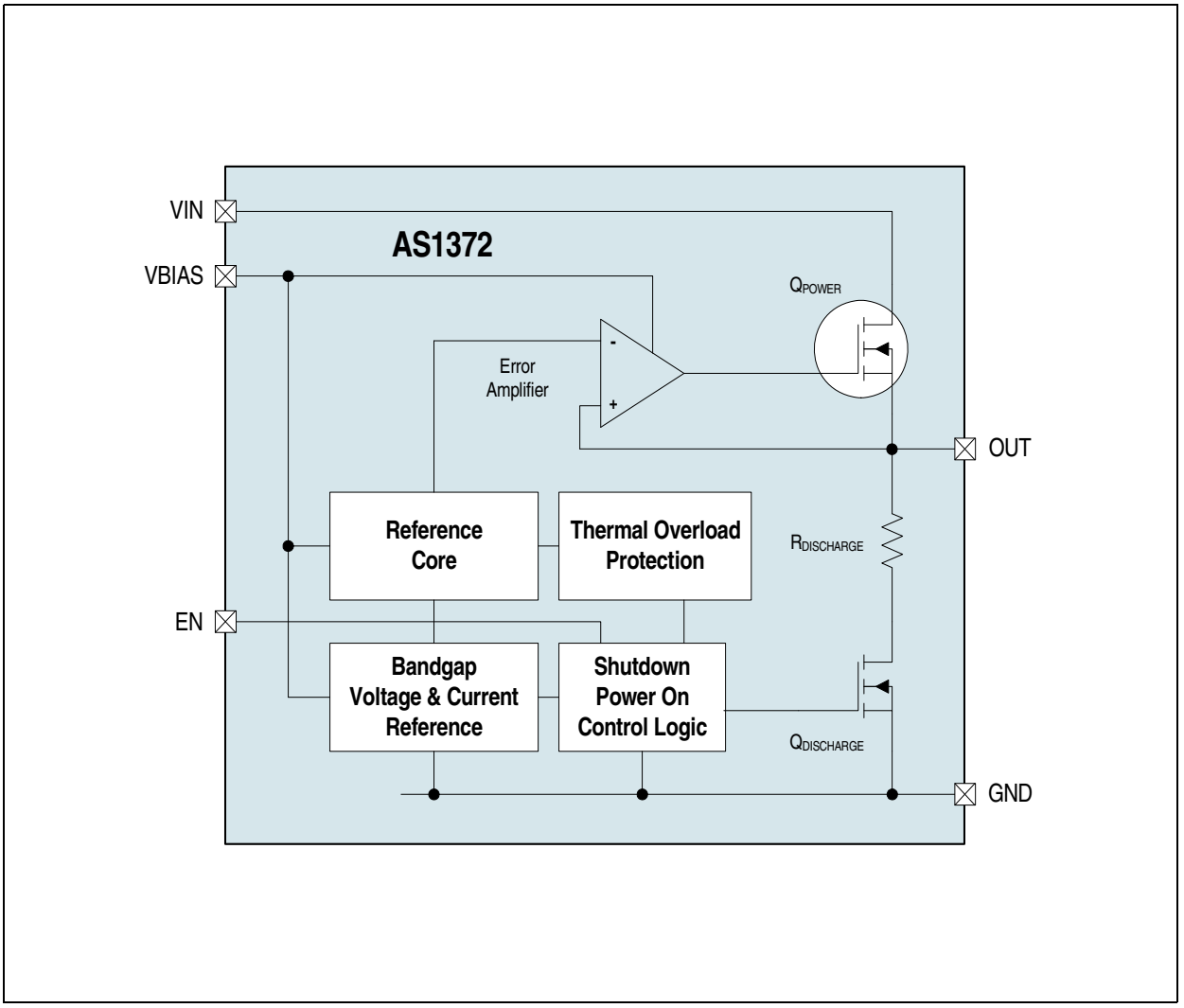
Shutdown current for the whole regulator is typically 10nA. The device features integrated short-circuit and over current protection. Under-Voltage lockout prevents erratic operation when the input voltage is slowly decaying (e.g. in a battery powered application). Thermal Protection shuts down the device when die temperature reaches 150°C. This is a useful protection when the device is under sustained short circuit conditions.

As illustrated in Figure 19, the devices comprise voltage reference, error amplifier, N-channel MOSFET pass transistor, internal voltage divider, current limiter, thermal sensor shutdown logic and output auto-discharge.

The bandgap reference is connected to the inverting input of the error amplifier. The error amplifier compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the N-channel MOSFET gate is pulled higher, allowing more current to pass to the output, and increases the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled down, allowing less current to pass to the output. The output voltage feeds back through an internal resistor voltage divider connected to pin OUT.

When the device enters shutdown, a separate low resistance path is enabled that discharges the output capacitors through a 100Ω (typ) resistance to ground.

Figure 19. AS1372 Block Diagram

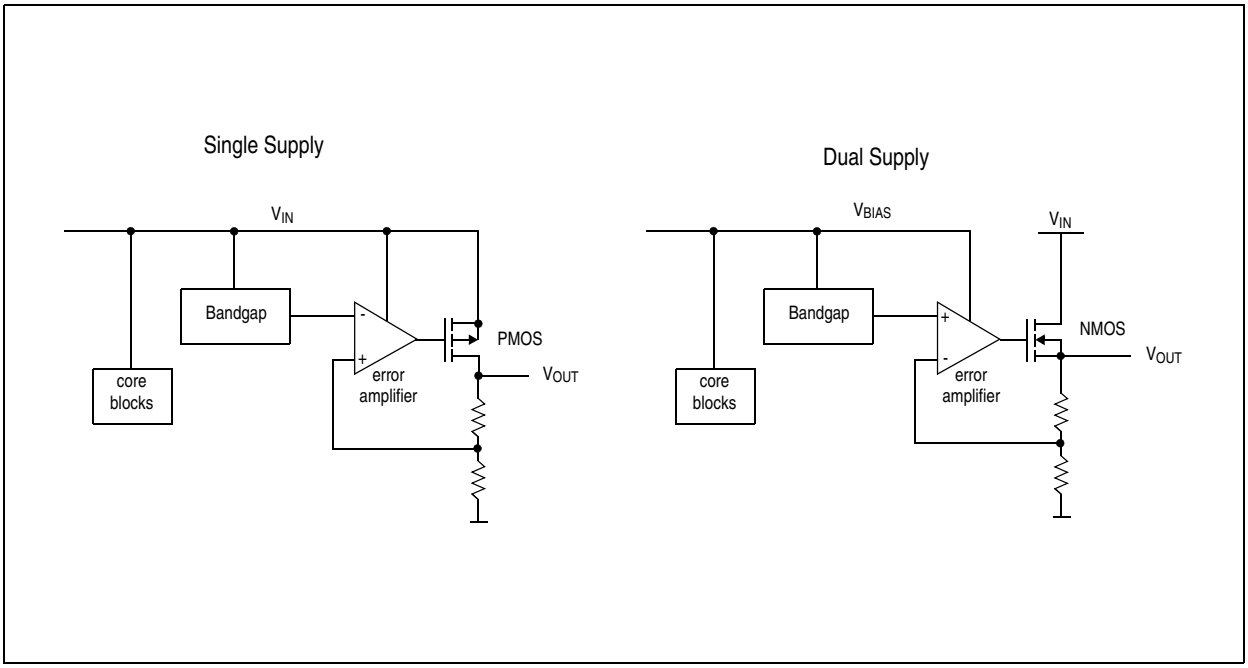


8.1 Advantages of Dual Supply Architecture vs. Traditional Single Supply Approach.

Compared to the traditional single supply approach, employing a P-channel series pass MOSFET, the dual rail architecture ensures improved performances in a LDO when operating at very low input voltages below the threshold of the internal series power N-channel MOSFET. The extra supply voltage at VBIAS (VBIAS > VIN) ensures that the N-channel MOSFET always operates above its threshold voltage.

Figure 20 shows simplified block diagrams of single supply P-channel LDO and dual rail N-channel series pass architectures.

Figure 20. N-channel and P-channel LDO Architectures



The P-channel LDO uses a PMOS output transistor connected in a common source configuration. During regulation, the P-channel gate-source voltage moves between VIN and GND as the load demands. The dual supply approach is based on an N-channel output transistor in common drain configuration where the source is connected to the regulated output. During regulation, the N-channel gate source voltage increases from VOUT to VBIAS as the load demands. As the drain voltage is not shared with the remaining blocks of the circuit, its value can be chosen independently. The N-channel source follower design allows improved efficiency and dropout at low input voltages and provides faster load transient response.

9 Application Information

9.1 Dropout Voltage

Dropout is the input to output voltage difference, below which the linear regulator ceases to regulate. At this point, the output voltage change follows the input voltage change. Dropout voltage may be measured at different currents and, in particular at the regulator maximum one. From this is obtained the MOSFET maximum series resistance over temperature etc. More generally:

$$V_{DROPOUT} = I_{LOAD} \times R_{SERIES} \quad \text{(EQ 1)}$$

Dropout is probably the most important specification when the regulator is used in a battery application. The dropout performance of the regulator defines the useful “end of life” of the battery before replacement or re-charge is required.

Figure 21. Graphical Representation of Dropout Voltage

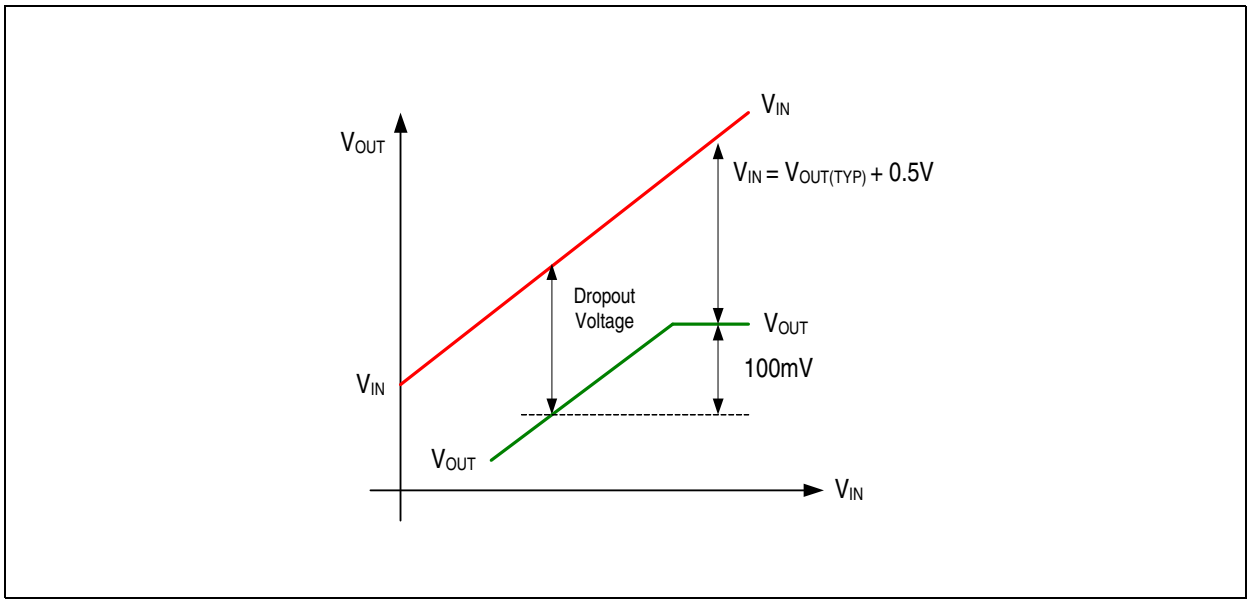


Figure 21 shows the variation of VOUT as VIN is varied for a certain load current. The practical value of dropout is the differential voltage (VOUT-VIN) measured at the point where the LDO output voltage has fallen by 100mV below the nominal, fully regulated output value. The nominal regulated output voltage of the LDO is that obtained when there is 500mV (or greater) input-output voltage differential.

9.2 Auto-Discharge

AS1372 features an auto-discharge function that discharges the load capacitance through a 100Ω (typ) path to ground when the device is placed in shutdown. This helps to minimizes the possibility that VOUT > VIN during shutdown caused by differing capacitance discharge rates at VIN and VOUT terminals.

When VOUT > VIN, reverse current flows through the inherent body diode of the N-channel series pass transistor. This current should be limited to 50mA or less. If this is not possible, then an external Schottky diode should be connected between VOUT (anode) and VIN (cathode) to bypass the discharge current around the AS1372.

9.3 Efficiency

Low quiescent current and low input-output voltage differential are important in battery applications amongst others, as the regulator efficiency is directly related to quiescent current and dropout voltage. Efficiency is given by:

$$\textit{Efficiency} = \frac{V_{LOAD} \times I_{LOAD}}{V_{IN}(I_Q + I_{LOAD})} \times 100\ \% \quad \text{(EQ 2)}$$

Where:
I_Q = Quiescent current of LDO measured at VBIAS

9.4 Power Dissipation

Maximum power dissipation (PD) of the LDO is the sum of the power dissipated by the internal series MOSFET and the quiescent current required to bias the internal voltage reference and the internal error amplifier, and is calculated as:

$$PD_{(MAX)}(Seriespass) = I_{LOAD(MAX)}(V_{IN(MAX)} - V_{OUT(MIN)}) \ \ Watts \qquad (EQ\ 3)$$

Internal power dissipation as a result of the bias current for the internal voltage reference and the error amplifier is calculated as:

$$PD_{(MAX)}(Bias) = V_{IN(MAX)}I_Q \ \ Watts \qquad (EQ\ 4)$$

Total LDO power dissipation is calculated as:

$$PD_{(MAX)}(Total) = PD_{(MAX)}(Seriespass) + PD_{(MAX)}(Bias) \ \ Watts \qquad (EQ\ 5)$$

9.5 Junction Temperature

Under all operating conditions, the maximum junction temperature should not be allowed to exceed 125ºC (unless the data sheet specifically allows). Limiting the maximum junction temperature requires knowledge of the heat path from junction to case (θ_{JC}ºC/W fixed by the IC manufacturer), and adjustment of the case to ambient heat path (θ_{CA}ºC/W) by manipulation of the PCB copper area adjacent to the IC position.

Figure 22. Package Physical Arrangements

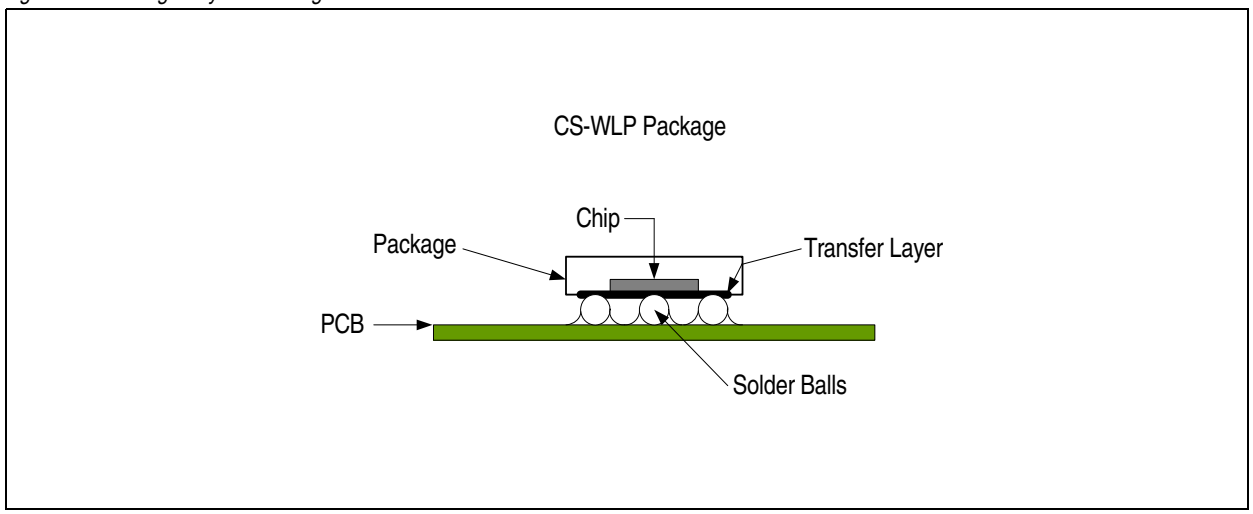
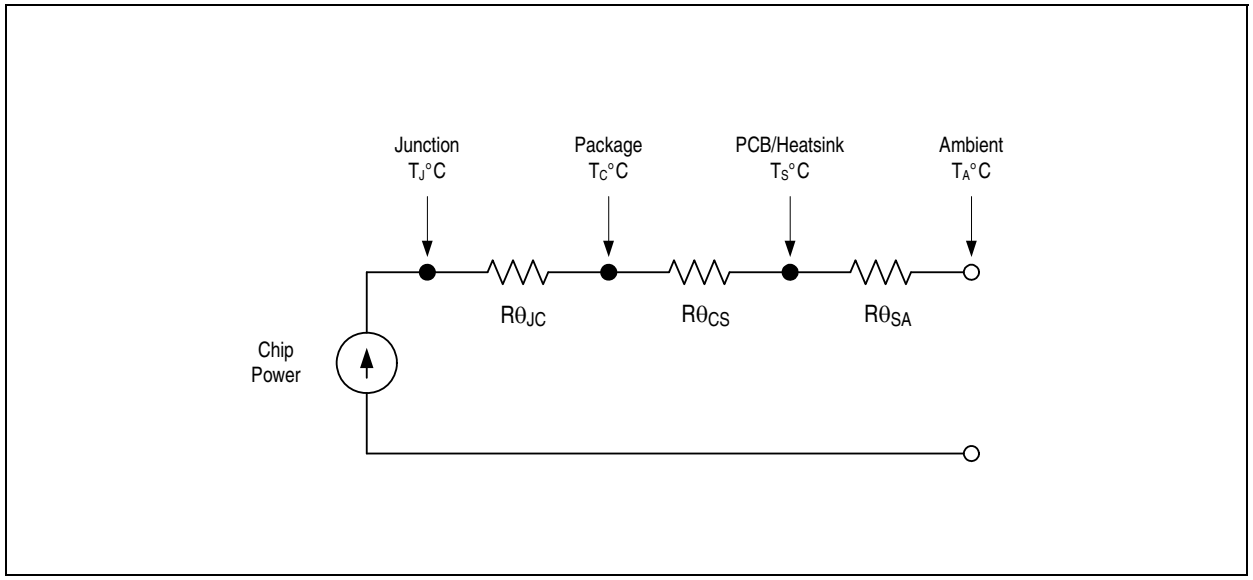


Figure 23. Steady State Heat Flow Equivalent Circuit



Total Thermal Path Resistance:

$$R\theta_{JA} = R\theta_{JC} + R\theta_{CS} + R\theta_{SA} \quad \textit{(EQ 6)}$$

Junction Temperature (T_JºC) is determined by:

$$T_J = (PD_{(MAX)} \times R\theta_{JA}) + T_{AMB} \ ºC \quad \textit{(EQ 7)}$$

9.6 Explanation of Steady State Specifications

9.6.1 Line Regulation

Line regulation is defined as the change in output voltage when the input (or line) voltage is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the input voltage changes. Line regulation is a measure of the DC open loop gain of the error amplifier. More generally:

Line Regulation = $\frac{\Delta V_{OUT}}{\Delta V_{IN}}$ and is a pure number

In practise, line regulation is referred to the regulator output voltage in terms of % / VOUT. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\textit{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{100}{V_{OUT}} \ \textit{\% / V} \quad \textit{(EQ 8)}$$

9.6.2 Load Regulation

Load regulation is defined as the change of the output voltage when the load current is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the load changes. Load regulation is a measure of the DC closed loop output resistance of the regulator. More generally:

$$\textit{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \ \textit{and is units of ohms } (\Omega) \quad \textit{(EQ 9)}$$

In practise, load regulation is referred to the regulator output voltage in terms of % / mA. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\textit{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \times \frac{100}{\Delta V_{OUT}} \ \textit{\% / mA} \quad \textit{(EQ 10)}$$

9.6.3 Setting Accuracy

Accuracy of the final output voltage is determined by the accuracy of the ratio of R1 and R2, the reference accuracy and the input offset voltage of the error amplifier. When the regulator is supplied pre-trimmed, the output voltage accuracy is fully defined in the output voltage specification.

When the regulator has a SET terminal, the output voltage may be adjusted externally. In this case, the tolerance of the external resistor network must be incorporated into the final accuracy calculation. Generally:

$$V_{OUT} = (V_{SET} \pm \Delta V_{SET})\left(1 + \frac{R1 \pm \Delta R1}{R2 \pm \Delta R2}\right) \quad \textit{(EQ 11)}$$

The reference tolerance is given both at 25ºC and over the full operating temperature range.

9.6.4 Total Accuracy

Away from dropout, total steady state accuracy is the sum of setting accuracy, load regulation and line regulation. Generally:

Total % Accuracy = Setting % Accuracy + Load Regulation % + Line Regulation % *(EQ 12)*

9.7 Explanation of Dynamic Specifications

9.7.1 Power Supply Rejection Ratio (PSRR)

Known also as Ripple Rejection, this specification measures the ability of the regulator to reject noise and ripple beyond DC. PSRR is a summation of the individual rejections of the error amplifier, reference and AC leakage through the series pass transistor. The specification, in the form of a typical attenuation plot with respect to frequency, shows up the gain bandwidth compromises forced upon the designer in low quiescent current conditions. Generally:

$$PSSR = 20Log\frac{\delta V_{OUT}}{\delta V_{IN}}\ dB \text{ using lower case } \delta \text{ to indicate AC values} \qquad (EQ\ 13)$$

Power supply rejection ratio is fixed by the internal design of the regulator. Additional rejection must be provided externally.

9.7.2 Output Capacitor ESR

The series regulator is a negative feedback amplifier, and as such is conditionally stable. The ESR of the output capacitor is usually used to cancel one of the open loop poles of the error amplifier in order to produce a single pole response. Excessive ESR values may actually cause instability by excessive changes to the closed loop unity gain frequency crossover point. The range of ESR values for stability is usually shown either by a plot of stable ESR versus load current, or a limit statement in the datasheet.

Some ceramic capacitors exhibit large capacitance and ESR variations with temperature and DC bias. Z5U and Y5V capacitors may be required to ensure stability at temperatures below T_{AMB} = -10ºC. With X7R or X5R capacitors, a 1µF capacitor should be sufficient at all operating temperatures.

Larger output capacitor values (10µF max) help to reduce noise and improve load transient-response, stability and power-supply rejection.

9.7.3 Input Capacitor

If the AS1372 is used stand alone, an input capacitor at V_{IN} is required for stability. It is recommended that a 1.0µF capacitor be connected between the AS1372 power supply input pin V_{IN} and ground (capacitance value may be increased without limit).

This capacitor must be located at a distance of not more than 1cm from the V_{IN} pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

A capacitor at V_{BIAS} is not required if the distance to the supply does not exceed 5cm.

If the AS1372 device is used in the typical application as post regulator after a DC-DC regulator, no input capacitors are required at all as the capacitors of the DC-DC regulator (C_{IN} and C_{OUT}) are sufficient if both components are mounted close to each other and a proper GND plane is used. If the distance between the output capacitor of the DC-DC regulator and the V_{IN} pin of the AS1372 is larger than 5cm, a capacitor at V_{IN} is recommended.

9.7.4 Noise

The regulator output is a DC voltage with noise superimposed on the output. The noise comes from three sources; the reference, the error amplifier input stage, and the output voltage setting resistors. Noise is a random fluctuation and if not minimized in some applications, will produce system problems.

9.7.5 Transient Response

The series regulator is a negative feedback system, and therefore any change at the output will take a finite time to be corrected by the error loop. This “propagation time” is related to the bandwidth of the error loop. The initial response to an output transient comes from the output capacitance, and during this time, ESR is the dominant mechanism causing voltage transients at the output. More generally:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times R_{ESR} \quad \text{Units are Volts, Amps, Ohms.} \qquad (EQ\ 14)$$

Thus an initial +50mA change of output current will produce a -12mV transient when the ESR=240mΩ. Remember to keep the ESR within stability recommendations when reducing ESR by adding multiple parallel output capacitors.

After the initial ESR transient, there follows a voltage droop during the time that the LDO feedback loop takes to respond to the output change. This drift is approx. linear in time and sums with the ESR contribution to make a total transient variation at the output of:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times \left(R_{ESR} + \frac{T}{C_{LOAD}}\right) \quad \text{Units are Volts, Seconds, Farads, Ohms.} \qquad (EQ\ 15)$$

Where:
C_{LOAD} is output capacitor
T = Propagation delay of the LDO

This shows why it is convenient to increase the output capacitor value for a better support for fast load changes. Of course the formula holds for t < “propagation time”, so that a faster LDO needs a smaller cap at the load to achieve a similar transient response. For instance 50mA load current step produces 50mV output drop if the LDO response is 1usec and the load cap is 1µF.

There is also a steady state error caused by the finite output impedance of the regulator. This is derived from the load regulation specification discussed above.

9.7.6 Exit from Shutdown Delay

This specification defines the time taken for the LDO to awake from shutdown. The time is measured from the release of the enable pin to the time that the output voltage is within 5% of the final value. It assumes that the voltage at VIN is stable and within the regulator min and max limits. Shutdown reduces the quiescent current to very low, mostly leakage values (<1µA).

9.7.7 Thermal Protection

To prevent operation under extreme fault conditions, such as a permanent short circuit at the output, thermal protection is built into the device. Die temperature is measured, and when a 150ºC threshold is reached, the device enters shutdown. When the die cools sufficiently, the device will restart (assuming input voltage exists and the device is enabled). Hysteresis of 25ºC prevents low frequency oscillation between start-up and shutdown around the temperature threshold.

9.7.8 Power Supply Sequencing

The AS1372 requires two different supply voltages active at the same time for correct operation. They are as given below.

1. VIN, the power input voltage, that is regulated to provide the fixed output voltage.
2. VBIAS, the bias input voltage, supplies internal circuitry.

It's important that VIN does not exceed VBIAS at any time. If the device is used in the typical post regulation application as shown in Figure 1, the sequencing of the two power supplies is not an issue as VBIAS supplies both, the DC-DC regulator and the AS1372. The output voltage of the DC-DC regulator will take some time to rise up and supply VIN of AS1372. In this application VIN will always ramp up more slowly than VBIAS. In case VIN is shorted to VBIAS, the voltages at the two supply pins will ramp up simultaneously causing no problem. Only in applications with two independent supplies connected to the AS1372 special care must be taken to guarantee that VIN is always = VBIAS.

9.7.9 Auto-Discharge

When the AS1372 is placed in shutdown, a 100Ω path to ground is connected at the output. This path speeds up the discharge of the capacitor(s) connected to the regulator output. Assuming that VIN remains constant and always >VOUT, output discharge time is calculated from the following relationship:

$$V(t) = V_{REG} e^{-\frac{t}{RC}} \quad \text{(EQ 16)}$$

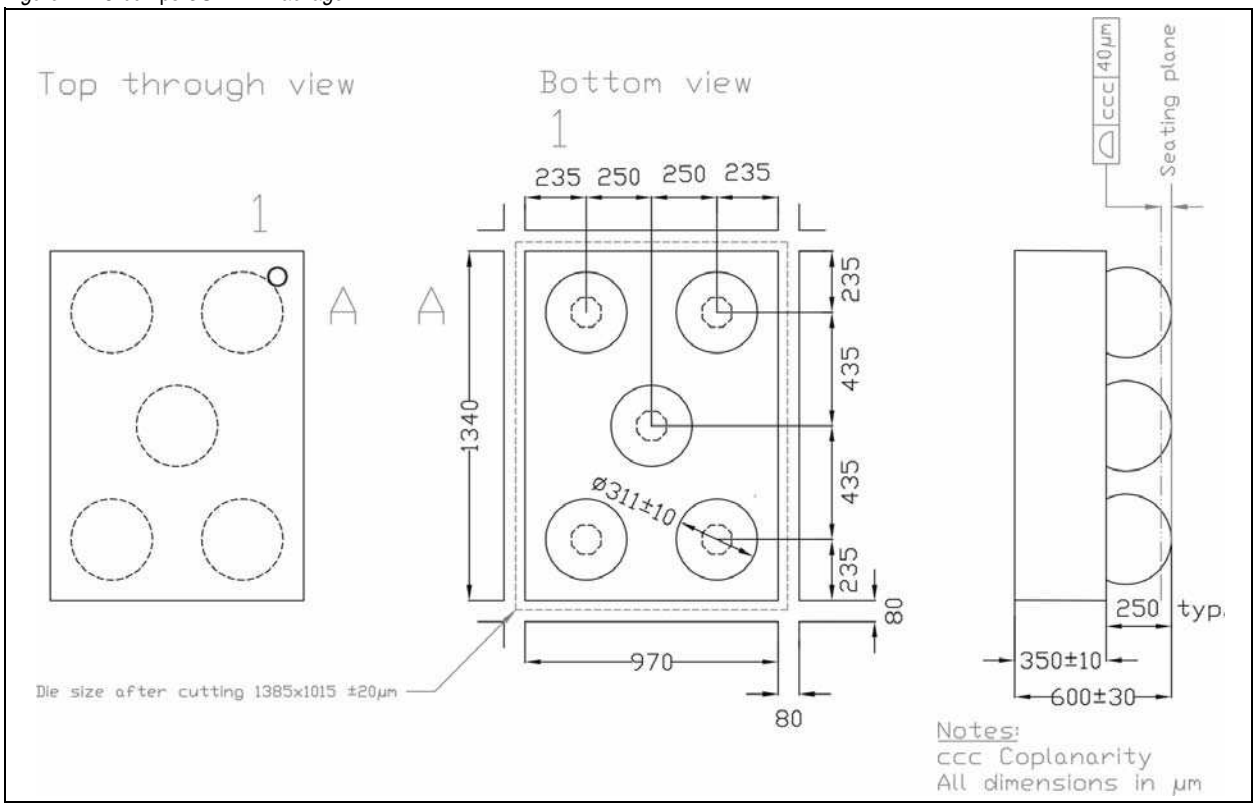
Where:
t = specified time after regulator shutdown (sec)
VREG = Regulated output voltage (initial condition)
R = 100Ω (typ) discharge resistance
C = Output capacitance (Farad)

Put more simply, the output discharge will reach 90% below the regulated output voltage in 2.2RC seconds, R and C defined as above.

10 Package Drawings and Markings

The device is available in a 5-bumps CS-WLP package.

Figure 24. 5-bumps CS-WLP *Package*



Revision History

Revision	Date	Owner	Description
1.1			Initial revision
1.3	07 Sep, 2011	afe	Changes made across document for version 1.3
1.4	12 dec, 2011		Updated equations in Power Dissipation section

Note: Typos may not be explicitly mentioned under revision history.

11 Ordering Information

The device is available as the standard products listed in Table 4.

Table 4. Ordering Information

Ordering Code	Marking	Output	Description	Delivery Form	Package
AS1372-BWLT-07	Available on request	0.7V	350mA Dual Rail Linear Regulator	Tape and Reel	5-bumps CS-WLP
AS1372-BWLT-10	ASSN	1.0V			
AS1372-BWLT-12	ASSQ	1.2V			
AS1372-BWLT-13	ASSO	1.3V			
AS1372-BWLT-14	Available on request	1.4V			
AS1372-BWLT-15	ASSR	1.5V			
AS1372-BWLT-16	Available on request	1.6V			
AS1372-BWLT-18	ASSS	1.8V			
AS1372-BWLT-20	Available on request	2.0V			

Non-standard devices from 0.5V to 1.1V are available in 50mV steps and from 1.1V to 2.2V in 100mV steps. For more information and inquiries, contact http://www.austriamicrosystems.com/contact

Note: All products are RoHS compliant.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

Technical Support is available at http://www.austriamicrosystems.com/Technical-Support

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
or find your local distributor at http://www.austriamicrosystems.com/distributor

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