



CDCLVP1216 16 LVPECL Output, High-Performance Clock Buffer

1 Features

- 2:16 Differential Buffer
- Selectable Clock Inputs Through Control Pin
- Universal Inputs Accept LVPECL, LVDS, and LVCMOS/LVTTL
- 16 LVPECL Outputs
- Maximum Clock Frequency: 2 GHz
- Maximum Core Current Consumption: 110 mA
- Very Low Additive Jitter: <100 fs,rms in 10-kHz to 20-MHz Offset Range:
 - 57 fs, rms (typ) @ 122.88 MHz
 - 48 fs, rms (typ) @ 156.25 MHz
 - 30 fs, rms (typ) @ 312.5 MHz
- 2.375 V to 3.6 V Device Power Supply
- Maximum Propagation Delay: 550 ps
- Maximum Output Skew: 30 ps
- LVPECL Reference Voltage, V_{AC_REF} , Available for Capacitive-Coupled Inputs
- Industrial Temperature Range: -40°C to $+85^{\circ}\text{C}$
- ESD Protection Exceeds 2 kV (HBM)
- Available in 7 mm x 7 mm QFN-48 (RGZ) Package

2 Applications

- Wireless Communications
- Telecommunications/Networking
- Medical Imaging
- Test and Measurement Equipment

3 Description

The CDCLVP1216 is a highly versatile, low additive jitter buffer that can generate 16 copies of LVPECL clock outputs from one of two selectable LVPECL, LVDS, or LVCMOS inputs for a variety of communication applications. It has a maximum clock frequency up to 2 GHz. The CDCLVP1216 features an on-chip multiplexer (MUX) for selecting one of two inputs that can be easily configured solely through a control pin. The overall additive jitter performance is less than 0.1 ps, RMS from 10 kHz to 20 MHz, and overall output skew is as low as 30 ps, making the device a perfect choice for use in demanding applications.

The CDCLVP1216 clock buffer distributes one of two selectable clock inputs (IN0, IN1) to 16 pairs of differential LVPECL clock outputs (OUT0, OUT15) with minimum skew for clock distribution. The CDCLVP1216 can accept two clock sources into an input multiplexer. The inputs can be LVPECL, LVDS, or LVCMOS/LVTTL.

The CDCLVP1216 is specifically designed for driving 50- Ω transmission lines. When driving the inputs in single-ended mode, the LVPECL bias voltage (V_{AC_REF}) should be applied to the unused negative input pin. However, for high-speed performance up to 2 GHz, differential mode is strongly recommended.

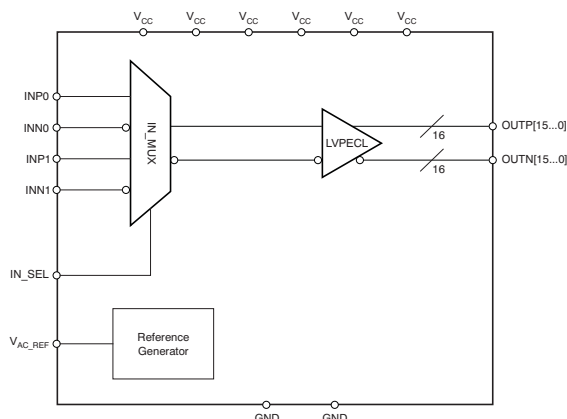
The CDCLVP1216 is packaged in a small 48-pin, 7-mm x 7-mm QFN package and is characterized for operation from -40°C to $+85^{\circ}\text{C}$.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE (NOM)
CDCLVP1216	QFN (48)	7.00 mm x 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Functional Block Diagram



Differential Output Peak-to-Peak Voltage vs Frequency

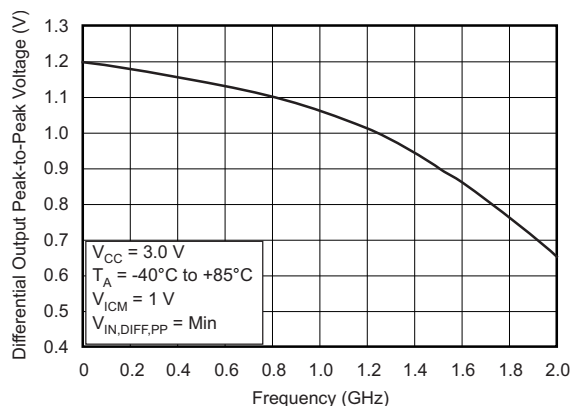


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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (June 2014) to Revision E	Page
• Added titles to first page images	1
• Added "NOTE" at the beginning of "Applications and Implementation" section	19
• Changed JEDEC symbol to $R_{\theta JA}$	22

Changes from Revision C (August 2011) to Revision D	Page
• Added data sheet flow and layout to conform with new TI standards. Added the following sections: Application and Implementation; Power Supply Recommendations; Layout; Device and Documentation Support; Mechanical, Packaging, and Ordering Information	1
• Added $f_{IN} = 125\text{ MHz, }312.5\text{ MHz}$ for $V_{OUT, DIFF, PP}$	7
• Typical values, Max values, and footnotes for 122.88 MHz, 156.25 MHz, and 312.5 MHz test conditions corresponding to Random Additive Jitter for Electrical Characteristics: LVPECL Output, at $V_{CC} = 2.375\text{ V to }2.625\text{ V}$	8
• Typical values, Max values, and footnotes for 122.88 MHz, 156.25 MHz, and 312.5 MHz test conditions corresponding to Random Additive Jitter for Electrical Characteristics: LVPECL Output, at $V_{CC} = 3.0\text{ V to }3.6\text{ V}$	9

Changes from Revision B (May, 2010) to Revision C	Page
• Revised description of pin 8	5
• Corrected V_{IL} parameter description in <i>Electrical Characteristics</i> table for LVCMOS input	7
• Added footnote "Internally generated bias voltage ..." to <i>Electrical Characteristics</i> table for LVPECL Output, $V_{CC} = 2.375\text{ V to }2.625\text{ V}$	7
• Changed recommended resistor values in Figure 12	15
• Changed recommended resistor values in Figure 16	17

Changes from Revision A (July, 2009) to Revision B
Page

• Changed description of INN1, INN0 and INP1, INP0 pins in Pin Descriptions table	4
• Changed descriptions of all output pins in Pin Descriptions table.....	4

CDCLVP1216

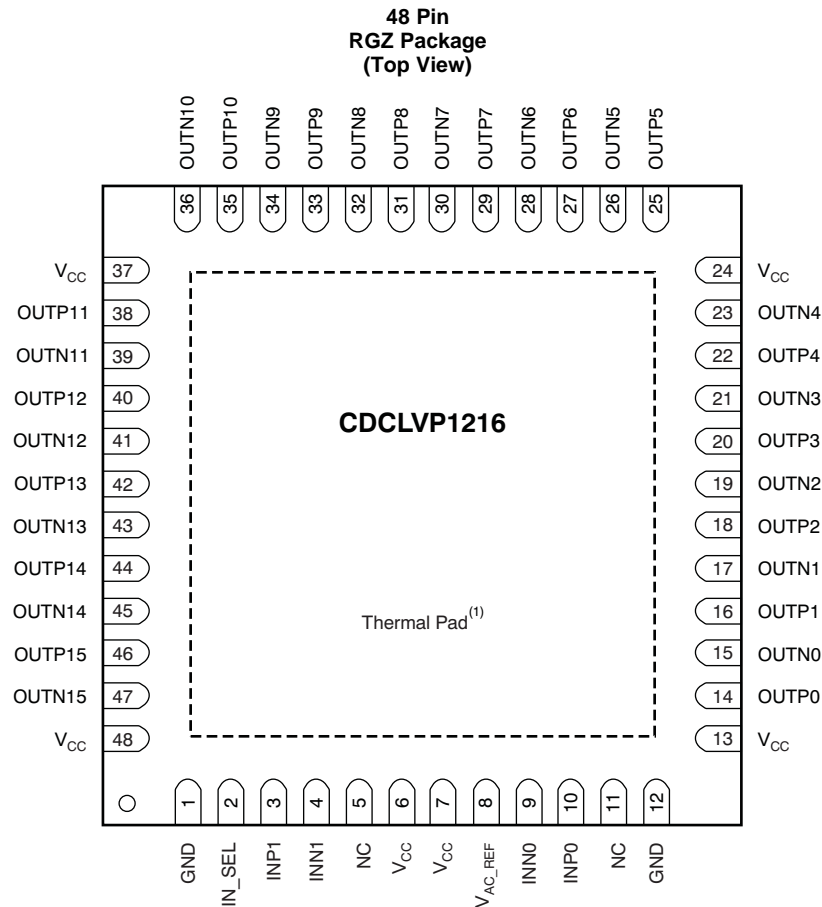
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6 Device Comparison Table

PACKAGED DEVICES	T _A	FEATURES
CDCLVP1216RGZT	–40°C to +85°C	48-pin QFN (RGZ) package, small tape and reel
CDCLVP1216RGZR	–40°C to +85°C	48-pin QFN (RGZ) package, tape and reel

7 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
V _{CC}	6, 7, 13, 24, 37, 48	Power	2.5-/3.3-V supplies for the device
GND	1, 12	Ground	Device grounds
INP0, INN0	10, 9	Input	Differential input pair or single-ended input. Unused input pair can be left floating.
INP1, INN1	3, 4	Input	Redundant differential input pair or single-ended input. Unused input pair can be left floating.
OUTP15, OUTN15	46, 47	Output	Differential LVPECL output pair no. 15. Unused output pair can be left floating.
OUTP14, OUTN14	44, 45	Output	Differential LVPECL output pair no. 14. Unused output pair can be left floating.
OUTP13, OUTN13	42, 43	Output	Differential LVPECL output pair no. 13. Unused output pair can be left floating.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
OUTP12, OUTN12	40, 41	Output	Differential LVPECL output pair no. 12. Unused output pair can be left floating.
OUTP11, OUTN11	38, 39	Output	Differential LVPECL output pair no. 11. Unused output pair can be left floating.
OUTP10, OUTN10	35, 36	Output	Differential LVPECL output pair no. 10. Unused output pair can be left floating.
OUTP9, OUTN9	33, 34	Output	Differential LVPECL output pair no. 9. Unused output pair can be left floating.
OUTP8, OUTN8	31, 32	Output	Differential LVPECL output pair no. 8. Unused output pair can be left floating.
OUTP7, OUTN7	29, 30	Output	Differential LVPECL output pair no. 7. Unused output pair can be left floating.
OUTP6, OUTN6	27, 28	Output	Differential LVPECL output pair no. 6. Unused output pair can be left floating.
OUTP5, OUTN5	25, 26	Output	Differential LVPECL output pair no. 5. Unused output pair can be left floating.
OUTP4, OUTN4	22, 23	Output	Differential LVPECL output pair no. 4. Unused output pair can be left floating.
OUTP3, OUTN3	20, 21	Output	Differential LVPECL output pair no. 3. Unused output pair can be left floating.
OUTP2, OUTN2	18, 19	Output	Differential LVPECL output pair no. 2. Unused output pair can be left floating.
OUTP1, OUTN1	16, 17	Output	Differential LVPECL output pair no. 1. Unused output pair can be left floating.
OUTP0, OUTN0	14, 15	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating.
IN_SEL	2	Input	Pulldown (see Pin Characteristics) MUX select input for input choice (see Table 1)
V _{AC_REF}	8	Output	Bias voltage output for capacitive coupled inputs. Do not use V _{AC_REF} at V _{CC} < 3.0 V. If used, it is recommended to use a 0.1-μF capacitor to GND on this pin. The output current is limited to 2 mA.
NC	5, 11	—	Do not connect

Table 1. Input Selection Table

IN_SEL	ACTIVE CLOCK INPUT
0	INP0, INN0
1	INP1, INN1

8 Specifications

8.1 Pin Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
R _{PULLDOWN}	Input pulldown resistor		150		kΩ

8.2 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).⁽¹⁾

		MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾	–0.5		4.6	V
V _{IN}	Input voltage range ⁽³⁾	–0.5		V _{CC} +0.5	V
V _{OUT}	Output voltage range ⁽³⁾	–0.5		V _{CC} +0.5	V
I _{IN}	Input current			20	mA
I _{OUT}	Output current			50	mA
T _A	Specified free-air temperature range (no airflow)	–40		+85	°C
T _J	Maximum junction temperature			+125	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All supply voltages must be supplied simultaneously.
- (3) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

8.3 Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature range		–65	+150	°C
V _(ESD) ⁽¹⁾	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽²⁾	2		kV

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
- (2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

8.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage	2.375	2.50/3.30	3.60	V
T _A	Ambient temperature	–40		+85	°C

8.5 Thermal Information⁽¹⁾⁽²⁾

THERMAL METRIC ⁽³⁾		CDCLVP1216	UNIT
		RGZ Package	
		48 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	33.8, 0 LFM ⁽⁴⁾	°C/W
		22.6, 150 LFM ⁽⁴⁾	
		19.2, 400 LFM ⁽⁴⁾	
θ _{JP} ⁽⁵⁾	Junction-to-pad thermal resistnace	3.67 ⁽⁴⁾	

- (1) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC 2S2P (high-K board).
- (2) Connected to GND with 16 thermal vias (0.3-mm diameter).
- (3) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (4) 4 × 4 Vias On Pad
- (5) θ_{JP} (junction-to-pad) is used for the QFN package, because the primary heat flow is from the junction to the GND pad of the QFN package.

8.6 Electrical Characteristics: LVCMOS Input⁽¹⁾

At $V_{CC} = 2.375\text{ V}$ to 3.6 V and $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{IN} Input frequency				200	MHz
V_{th} Input threshold voltage	External threshold voltage applied to complementary input	1.1		1.8	V
V_{IH} Input high voltage		$V_{th} + 0.1$		V_{CC}	V
V_{IL} Input low voltage		0		$V_{th} - 0.1$	V
I_{IH} Input high current	$V_{CC} = 3.6\text{ V}$, $V_{IH} = 3.6\text{ V}$			40	μA
I_{IL} Input low current	$V_{CC} = 3.6\text{ V}$, $V_{IL} = 0\text{ V}$			-40	μA
$\Delta V/\Delta T$ Input edge rate	20% to 80%	1.5			V/ns
I_{CAP} Input capacitance			5		pF

(1) Figure 6 and Figure 7 show dc test setup.

8.7 Electrical Characteristics: Differential Input⁽¹⁾

At $V_{CC} = 2.375\text{ V}$ to 3.6 V and $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{IN} Input frequency	Clock input			2000	MHz
$V_{IN, DIFF, PP}$ Differential input peak-peak voltage	$f_{IN} \leq 1.5\text{ GHz}$	0.1		1.5	V
	$1.5\text{ GHz} \leq f_{IN} \leq 2\text{ GHz}$	0.2		1.5	V
V_{ICM} Input common-mode level		1.0		$V_{CC} - 0.3$	V
I_{IH} Input high current	$V_{CC} = 3.6\text{ V}$, $V_{IH} = 3.6\text{ V}$			40	μA
I_{IL} Input low current	$V_{CC} = 3.6\text{ V}$, $V_{IL} = 0\text{ V}$			-40	μA
$\Delta V/\Delta T$ Input edge rate	20% to 80%	1.5			V/ns
I_{CAP} Input capacitance			5		pF

(1) Figure 5 and Figure 8 show dc test setup. Figure 9 shows ac test setup.

8.8 Electrical Characteristics: LVPECL Output, at $V_{CC} = 2.375\text{ V}$ to 2.625 V ⁽¹⁾

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} Output high voltage		$V_{CC} - 1.26$		$V_{CC} - 0.9$	V
V_{OL} Output low voltage		$V_{CC} - 1.7$		$V_{CC} - 1.3$	V
$V_{OUT, DIFF, PP}$ Differential output peak-peak voltage	$f_{IN} \leq 2\text{ GHz}$	0.5		1.35	V
	$f_{IN} = 125\text{ MHz}$, 312.5 MHz		1.15		V
V_{AC_REF} Input bias voltage ⁽²⁾	$I_{AC_REF} = 2\text{ mA}$	$V_{CC} - 1.6$		$V_{CC} - 1.1$	V
t_{PD} Propagation delay	$V_{IN, DIFF, PP} = 0.1\text{ V}$			550	ps
	$V_{IN, DIFF, PP} = 0.3\text{ V}$			550	ps
$t_{SK, PP}$ Part-to-part skew				150	ps
$t_{SK, O}$ Output skew				30	ps
$t_{SK, P}$ Pulse skew (with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, $f_{OUT} = 100\text{ MHz}$	-50		50	ps

(1) Figure 10 and Figure 11 show dc and ac test setup.

(2) Internally generated bias voltage (V_{AC_REF}) is for 3.3 V operation only. It is recommended to apply externally generated bias voltage for $V_{CC} < 3.0\text{ V}$.

Electrical Characteristics: LVPECL Output, at $V_{CC} = 2.375\text{ V}$ to $2.625\text{ V}^{(1)}$ (continued)
 $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RJIT}	$f_{OUT} = 100\text{ MHz}$, $V_{IN,SE} = V_{CC}$, $V_{th} = 1.25\text{ V}$, 10 kHz to 20 MHz		0.11		ps, RMS
	$f_{OUT} = 100\text{ MHz}$, $V_{IN,SE} = 0.9\text{ V}$, $V_{th} = 1.1\text{ V}$, 10 kHz to 20 MHz		0.128		ps, RMS
	$f_{OUT} = 2\text{ GHz}$, $V_{IN,DIFF,PP} = 0.2\text{ V}$, $V_{ICM} = 1\text{ V}$, 10 kHz to 20 MHz		0.053		ps, RMS
	$f_{OUT} = 100\text{ MHz}$, $V_{IN,DIFF,PP} = 0.15\text{ V}$, $V_{ICM} = 1\text{ V}$, 10 kHz to 20 MHz		0.093		ps, RMS
	$f_{OUT} = 100\text{ MHz}$, $V_{IN,DIFF,PP} = 1\text{ V}$, $V_{ICM} = 1\text{ V}$, 10 kHz to 20 MHz		0.092		ps, RMS
	$f_{OUT} = 122.88\text{ MHz}^{(4)(5)}$ Square Wave, $V_{IN,PP} = 1\text{ V}$, 12 kHz to 20 MHz		0.057	0.088	ps, RMS
	$f_{OUT} = 122.88\text{ MHz}^{(4)(5)}$ Square Wave, $V_{IN,PP} = 1\text{ V}$, 10 kHz to 20 MHz		0.057	0.088	ps, RMS
	$f_{OUT} = 122.88\text{ MHz}^{(4)(5)}$ Square Wave, $V_{IN,PP} = 1\text{ V}$, 1 kHz to 40 MHz		0.086	0.121	ps, RMS
	$f_{OUT} = 156.25\text{ MHz}^{(5)(6)}$ Square Wave, $V_{IN,PP} = 1\text{ V}$, 12 kHz to 20 MHz		0.048	0.071	ps, RMS
	$f_{OUT} = 156.25\text{ MHz}^{(5)(6)}$ Square Wave, $V_{IN,PP} = 1\text{ V}$, 10 kHz to 20 MHz		0.048	0.071	ps, RMS
	$f_{OUT} = 156.25\text{ MHz}^{(5)(6)}$ Square Wave, $V_{IN,PP} = 1\text{ V}$, 1 kHz to 40 MHz		0.068	0.097	ps, RMS
	$f_{OUT} = 312.5\text{ MHz}^{(5)(7)}$ Square Wave, $V_{IN,PP} = 1\text{ V}$, 12 kHz to 20 MHz		0.030	0.048	ps, RMS
	$f_{OUT} = 312.5\text{ MHz}^{(5)(7)}$ Square Wave, $V_{IN,PP} = 1\text{ V}$, 10 kHz to 20 MHz		0.030	0.048	ps, RMS
	$f_{OUT} = 312.5\text{ MHz}^{(5)(7)}$ Square Wave, $V_{IN,PP} = 1\text{ V}$, 1 kHz to 40 MHz		0.045	0.068	ps, RMS
t_R/t_F	Output rise/fall time	20% to 80%		200	ps
I_{EE}	Supply internal current	Outputs unterminated		110	mA
I_{CC}	Output and internal supply current	All outputs terminated, $50\ \Omega$ to $V_{CC} - 2$		618	mA

(3) Parameter is specified by characterization. Not tested in production.

(4) Input source: 122.88 MHz Rohde & Schwarz SMA100A Signal Generator.

(5) Input source RMS Jitter (t_{RJIT_IN}) and Total RMS Jitter (t_{RJIT_OUT}) measured using Agilent E5052 Phase Noise Analyzer. Buffer device random additive jitter computed as: $t_{RJIT} = \text{SQRT}[(t_{RJIT_OUT})^2 - (t_{RJIT_IN})^2]$.

(6) Input source: 156.25 MHz Rohde & Schwarz SMA100A Signal Generator.

(7) Input source: 312.5 MHz Rohde & Schwarz SMA100A Signal Generator.

8.9 Electrical Characteristics: LVPECL Output, at $V_{CC} = 3.0\text{ V to }3.6\text{ V}^{(1)}$

 $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output high voltage		$V_{CC} - 1.26$		$V_{CC} - 0.9$	V
V_{OL}	Output low voltage		$V_{CC} - 1.7$		$V_{CC} - 1.3$	V
$V_{OUT, DIFF, PP}$	Differential output peak-peak voltage	$f_{IN} \leq 2\text{ GHz}$	0.65		1.35	V
V_{AC_REF}	Input bias voltage	$I_{AC_REF} = 2\text{ mA}$	$V_{CC} - 1.6$		$V_{CC} - 1.1$	V
t_{PD}	Propagation delay	$V_{IN, DIFF, PP} = 0.1\text{ V}$			550	ps
		$V_{IN, DIFF, PP} = 0.3\text{ V}$			550	ps
$t_{SK, PP}$	Part-to-part skew				150	ps
$t_{SK, O}$	Output skew				30	ps
$t_{SK, P}$	Pulse skew (with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, $f_{OUT} = 100\text{ MHz}$	-50		50	ps
t_{RJIT}	Random additive jitter (with 50% duty cycle input) ⁽²⁾	$f_{OUT} = 100\text{ MHz}$, $V_{IN, SE} = V_{CC}$, $V_{th} = 1.65\text{ V}$, 10 kHz to 20 MHz		0.101		ps, RMS
		$f_{OUT} = 100\text{ MHz}$, $V_{IN, SE} = 0.9\text{ V}$, $V_{th} = 1.1\text{ V}$, 10 kHz to 20 MHz		0.130		ps, RMS
		$f_{OUT} = 2\text{ GHz}$, $V_{IN, DIFF, PP} = 0.2\text{ V}$, $V_{ICM} = 1\text{ V}$, 10 kHz to 20 MHz		0.069		ps, RMS
		$f_{OUT} = 100\text{ MHz}$, $V_{IN, DIFF, PP} = 0.15\text{ V}$, $V_{ICM} = 1\text{ V}$, 10 kHz to 20 MHz		0.094		ps, RMS
		$f_{OUT} = 100\text{ MHz}$, $V_{IN, DIFF, PP} = 1\text{ V}$, $V_{ICM} = 1\text{ V}$, 10 kHz to 20 MHz		0.094		ps, RMS
		$f_{OUT} = 122.88\text{ MHz}$, ⁽³⁾⁽⁴⁾ Square Wave, $V_{IN, PP} = 1\text{ V}$, 12 kHz to 20 MHz		0.057		ps, RMS
		$f_{OUT} = 122.88\text{ MHz}$, ⁽³⁾⁽⁴⁾ Square Wave, $V_{IN, PP} = 1\text{ V}$, 10 kHz to 20 MHz		0.057		ps, RMS
		$f_{OUT} = 122.88\text{ MHz}$, ⁽³⁾⁽⁴⁾ Square Wave, $V_{IN, PP} = 1\text{ V}$, 1 kHz to 40 MHz		0.086		ps, RMS
		$f_{OUT} = 156.25\text{ MHz}$, ⁽⁴⁾⁽⁵⁾ Square Wave, $V_{IN, PP} = 1\text{ V}$, 12 kHz to 20 MHz		0.048		ps, RMS
		$f_{OUT} = 156.25\text{ MHz}$, ⁽⁴⁾⁽⁵⁾ Square Wave, $V_{IN, PP} = 1\text{ V}$, 10 kHz to 20 MHz		0.048		ps, RMS
		$f_{OUT} = 156.25\text{ MHz}$, ⁽⁴⁾⁽⁵⁾ Square Wave, $V_{IN, PP} = 1\text{ V}$, 1 kHz to 40 MHz		0.068		ps, RMS
		$f_{OUT} = 312.5\text{ MHz}$, ⁽⁴⁾⁽⁶⁾ Square Wave, $V_{IN, PP} = 1\text{ V}$, 12 kHz to 20 MHz		0.030		ps, RMS
		$f_{OUT} = 312.5\text{ MHz}$, ⁽⁴⁾⁽⁶⁾ Square Wave, $V_{IN, PP} = 1\text{ V}$, 10 kHz to 20 MHz		0.030		ps, RMS
		$f_{OUT} = 312.5\text{ MHz}$, ⁽⁴⁾⁽⁶⁾ Square Wave, $V_{IN, PP} = 1\text{ V}$, 1 kHz to 40 MHz		0.045		ps, RMS
t_R/t_F	Output rise/fall time	20% to 80%			200	ps
I_{EE}	Supply internal current	Outputs unterminated			110	mA
I_{CC}	Output and internal supply current	All outputs terminated, $50\ \Omega$ to $V_{CC} - 2$			618	mA

(1) Figure 10 and Figure 11 show dc and ac test setup.

(2) Parameter is specified by characterization. Not tested in production.

(3) Input source: 122.88 MHz Rohde & Schwarz SMA100A Signal Generator.

(4) Input source RMS Jitter (t_{RJIT_IN}) and Total RMS Jitter (t_{RJIT_OUT}) measured using Agilent E5052 Phase Noise Analyzer. Buffer device random additive jitter computed as: $t_{RJIT} = \text{SQRT}[(t_{RJIT_OUT})^2 - (t_{RJIT_IN})^2]$.

(5) Input source: 156.25 MHz Rohde & Schwarz SMA100A Signal Generator.

(6) Input source: 312.5 MHz Rohde & Schwarz SMA100A Signal Generator.

8.10 Timing Requirements

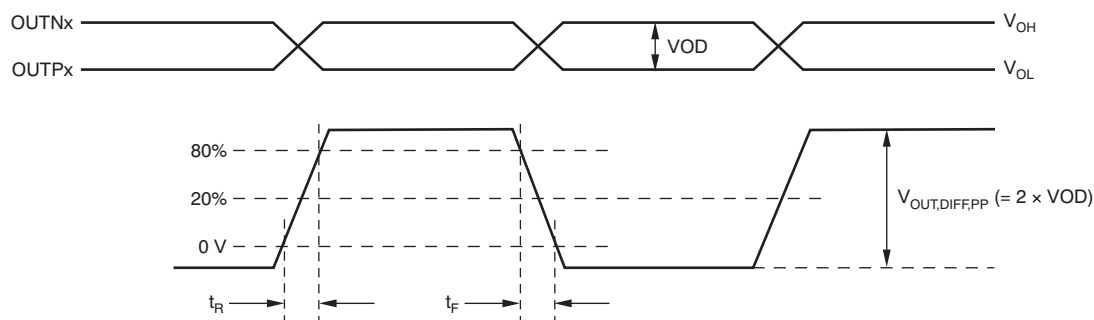
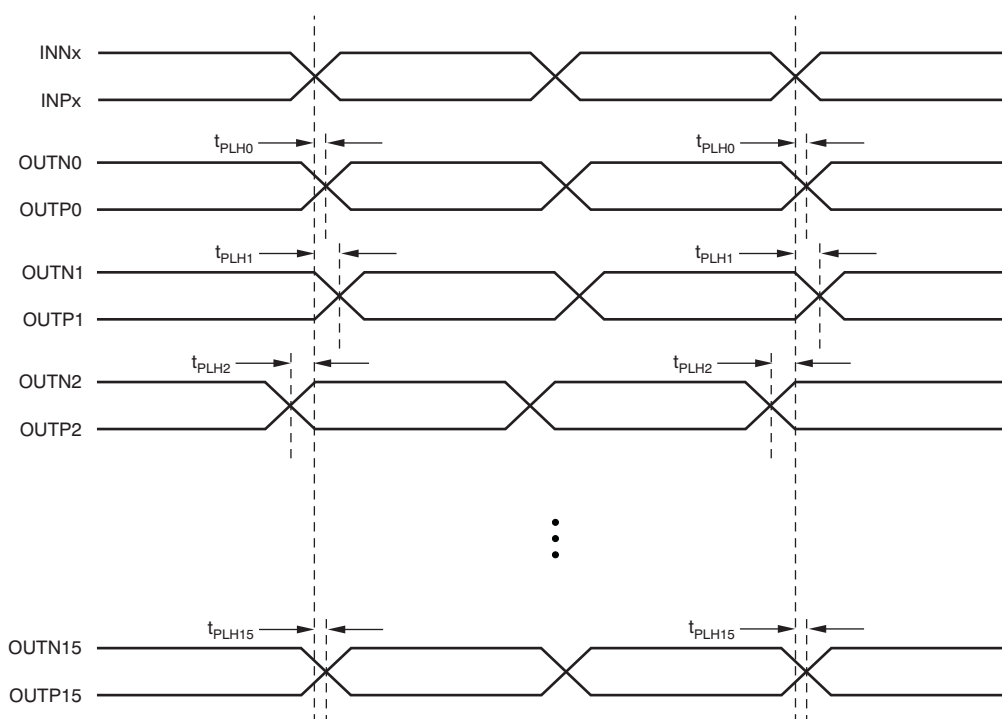


Figure 1. Output Voltage and Rise/Fall Time



- (1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest t_{PLHn} ($n = 0, 1, 2, \dots, 15$), or as the difference between the fastest and the slowest t_{PHLn} ($n = 0, 1, 2, \dots, 15$).
- (2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest t_{PLHn} ($n = 0, 1, 2, \dots, 15$) across multiple devices, or the difference between the fastest and the slowest t_{PHLn} ($n = 0, 1, 2, \dots, 15$) across multiple devices.

Figure 2. Output and Part-to-Part Skew

8.11 Typical Characteristics

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (unless otherwise noted).

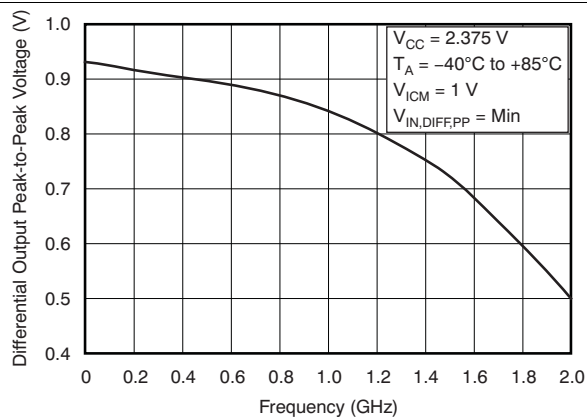


Figure 3. Differential Output Peak-to-Peak Voltage vs Frequency

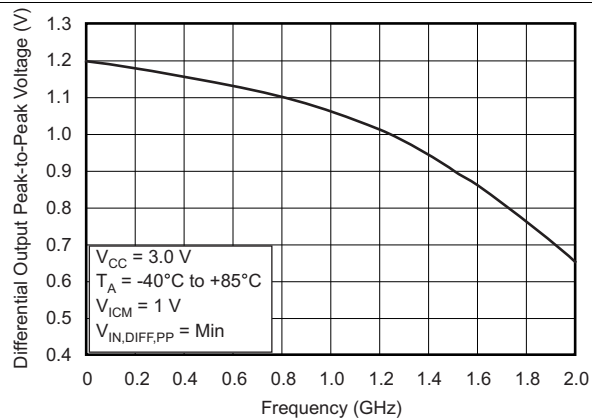


Figure 4. Differential Output Peak-to-Peak Voltage vs Frequency

9 Parameter Measurement Information

9.1 Test Configurations

This section describes the function of each block for the CDCLVP1216. Figure 5 through Figure 11 illustrate how the device should be setup for a variety of test configurations.

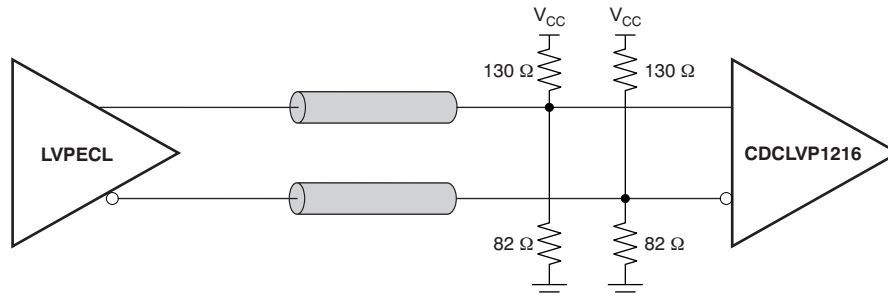


Figure 5. DC-Coupled LVPECL Input During Device Test

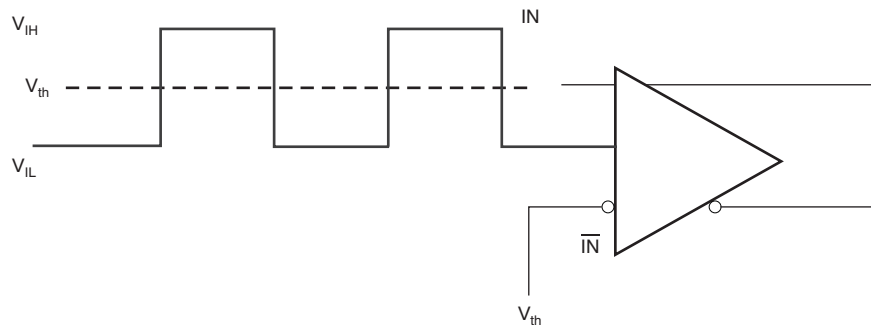


Figure 6. DC-Coupled LVCMOS Input During Device Test

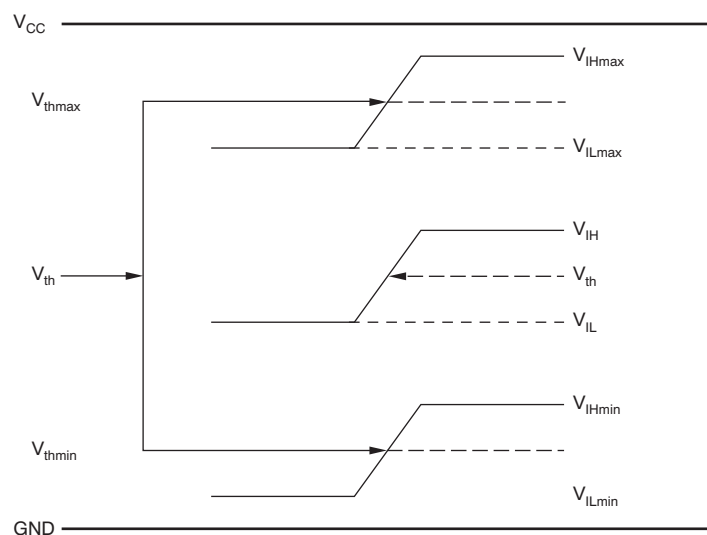


Figure 7. V_{th} Variation over LVCMOS V_{th} Levels

Test Configurations (continued)

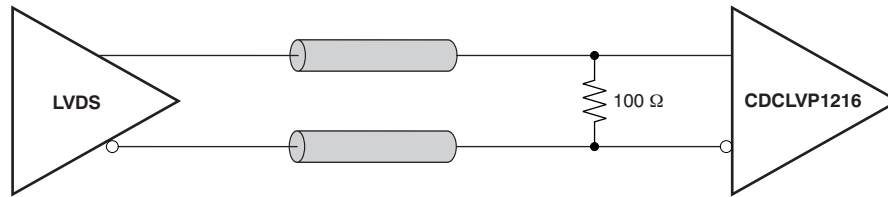


Figure 8. DC-Coupled LVDS Input During Device Test

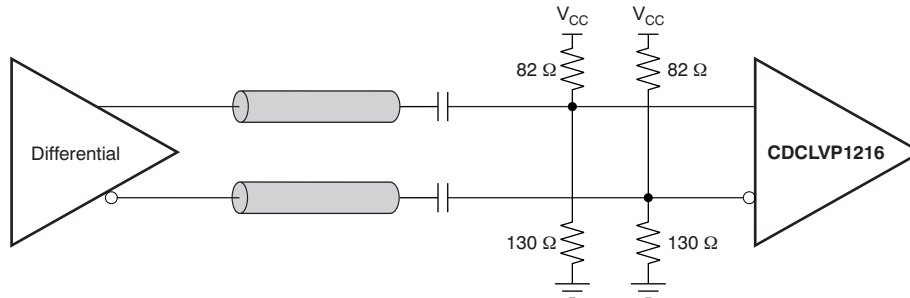


Figure 9. AC-Coupled Differential Input to Device

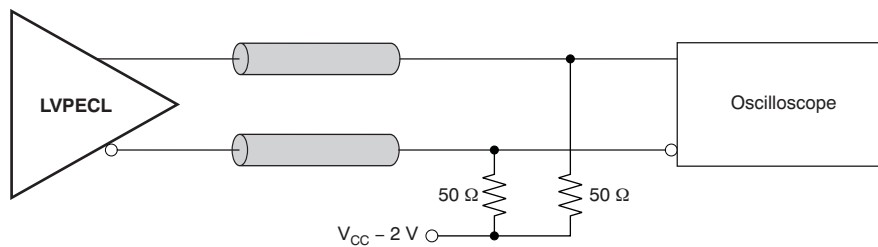


Figure 10. LVPECL Output DC Configuration During Device Test

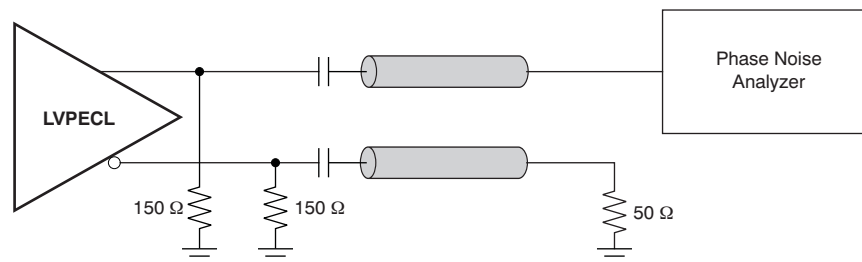


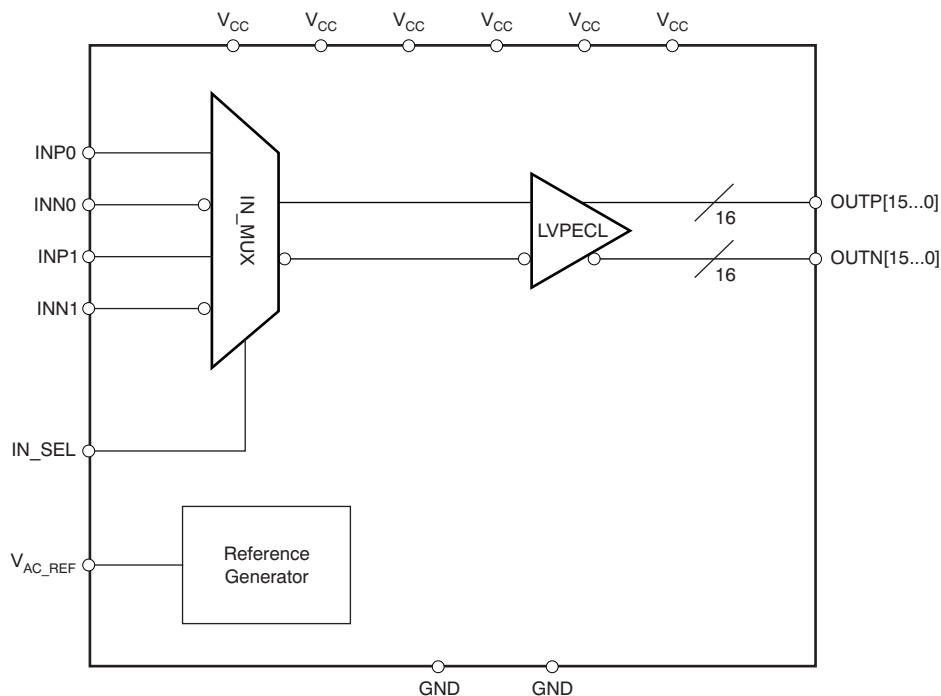
Figure 11. LVPECL Output AC Configuration During Device Test

10 Detailed Description

10.1 Overview

The CDCLVP1216 uses an open emitter follower stage for its LVPECL outputs. Therefore, proper output biasing and termination are required to ensure correct operation of the device and to maximize output signal integrity. The proper termination for LVPECL outputs is a $50\ \Omega$ to $(V_{CC} - 2)\text{ V}$, but this dc voltage is not readily available on PCB. Therefore, a Thevenin equivalent circuit is worked out for the LVPECL termination in both direct-coupled (DC) and AC-coupled configurations. These configurations are shown in [Figure 12](#) (a and b) for $V_{CC} = 2.5\text{ V}$ and [Figure 13](#) (a and b) for $V_{CC} = 3.3\text{ V}$, respectively. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltage for the driver and receiver is different, AC coupling is required.

10.2 Functional Block Diagram



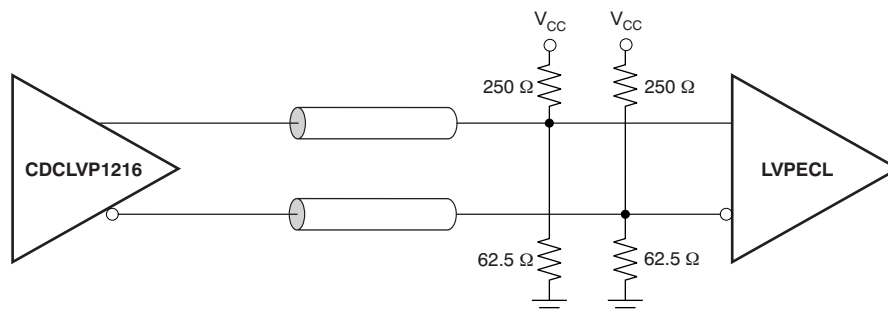
10.3 Feature Description

The CDCLVP1216 is a low additive jitter universal to LVPECL fan out buffer with 2 selectable inputs. The small package, low output skew, and low additive jitter make for a flexible device in demanding applications.

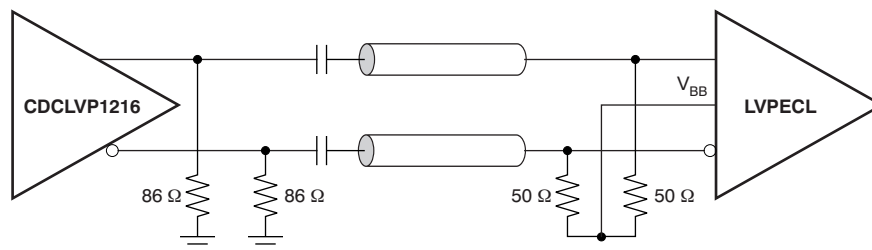
10.4 Device Functional Modes

The two inputs of the CDCLVP1216 are internally muxed together and can be selected via the control pin. Unused inputs and outputs can be left floating to reduce overall component cost. Both AC and DC coupling schemes can be used with the CDCLVP1216 to provide greater system flexibility.

10.4.1 LVPECL Output Termination



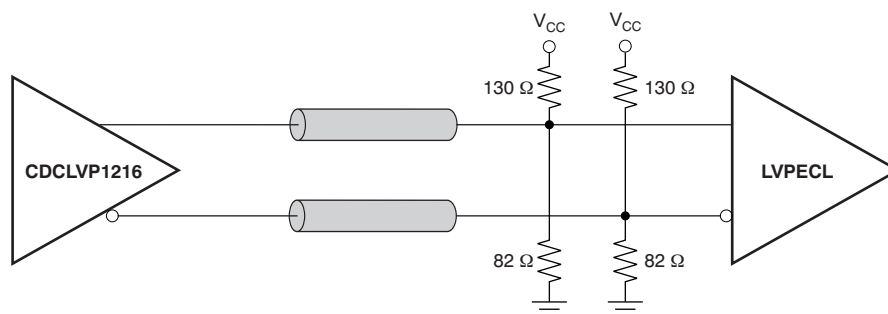
(a) Output DC Termination



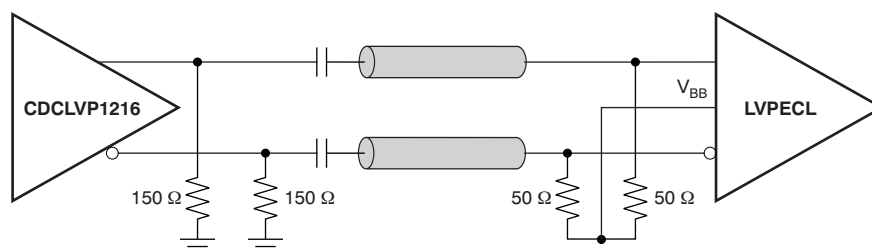
(b) Output AC Termination

Figure 12. LVPECL Output DC and AC Termination for $V_{CC} = 2.5\text{ V}$

Device Functional Modes (continued)



(a) Output DC Termination



(b) Output AC Termination

Figure 13. LVPECL Output DC and AC Termination for $V_{CC} = 3.3\text{ V}$

10.4.2 Input Termination

The CDCLVP1216 inputs can be interfaced with LVPECL, LVDS, or LVCMOS drivers. Figure 14 illustrates how to dc couple an LVCMOS input to the CDCLVP1216. The series resistance (R_S) should be placed close to the LVCMOS driver; its value is calculated as the difference between the transmission line impedance and the driver output impedance.

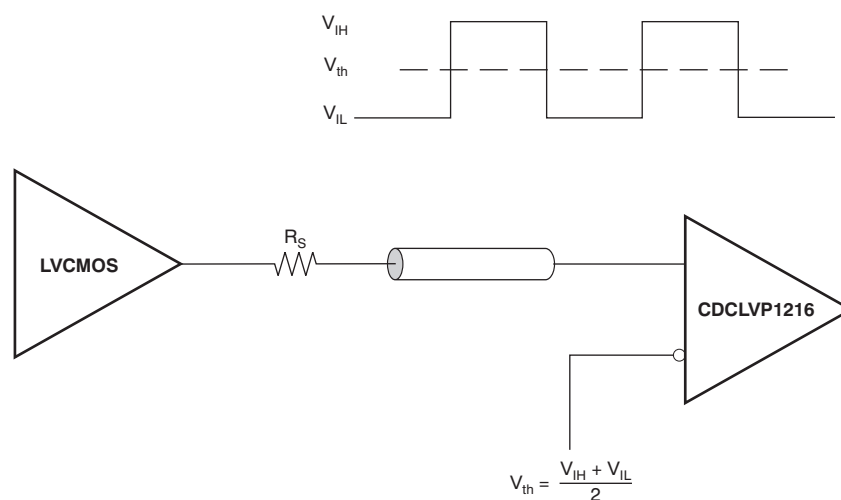


Figure 14. DC-Coupled LVCMOS Input to CDCLVP1216

Device Functional Modes (continued)

Figure 15 shows how to dc couple LVDS inputs to the CDCLVP1216. Figure 16 and Figure 17 describe the method of dc coupling LVPECL inputs to the CDCLVP1216 for $V_{CC} = 2.5\text{ V}$ and $V_{CC} = 3.3\text{ V}$, respectively.

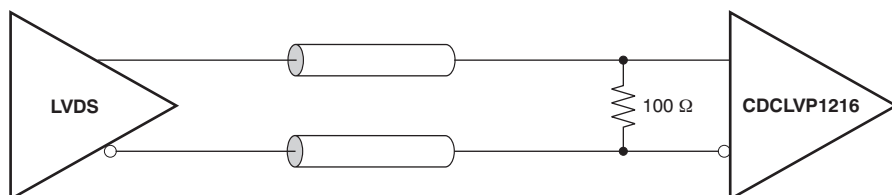


Figure 15. DC-Coupled LVDS Inputs to CDCLVP1216

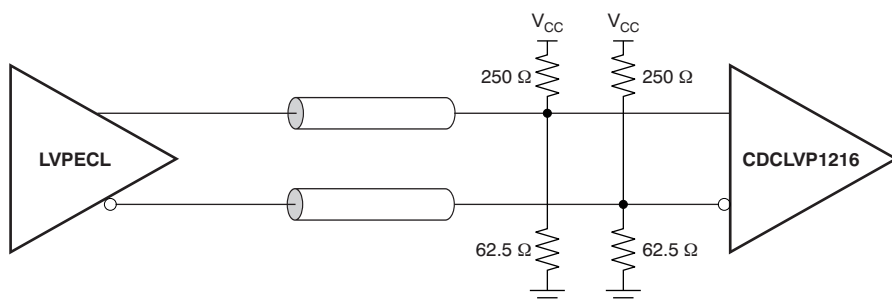


Figure 16. DC-Coupled LVPECL Inputs to CDCLVP1216 ($V_{CC} = 2.5\text{ V}$)

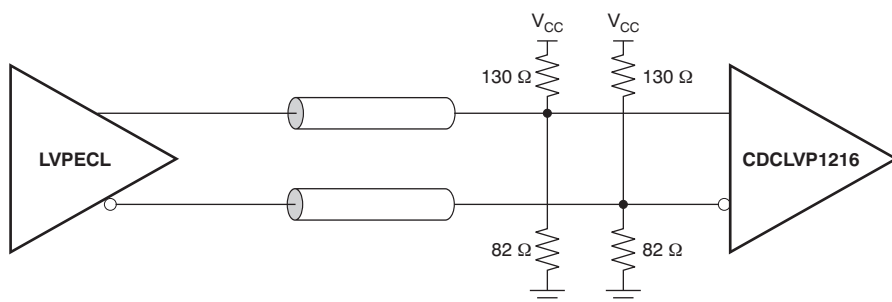


Figure 17. DC-Coupled LVPECL Inputs to CDCLVP1216 ($V_{CC} = 3.3\text{ V}$)

Device Functional Modes (continued)

Figure 18 and Figure 19 show the technique of ac coupling differential inputs to the CDCLVP1216 for $V_{CC} = 2.5$ V and $V_{CC} = 3.3$ V, respectively. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, ac coupling is required.

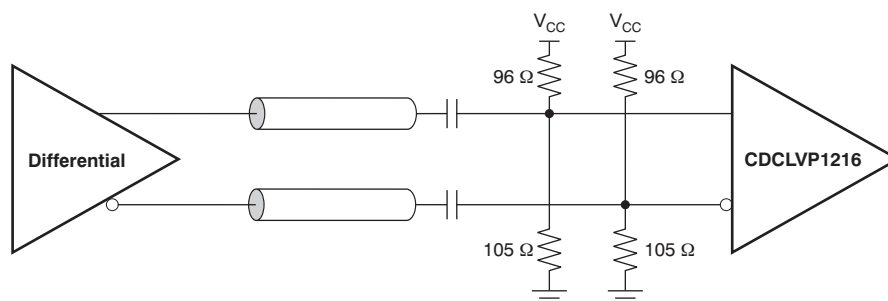


Figure 18. AC-Coupled Differential Inputs to CDCLVP1216 ($V_{CC} = 2.5$ V)

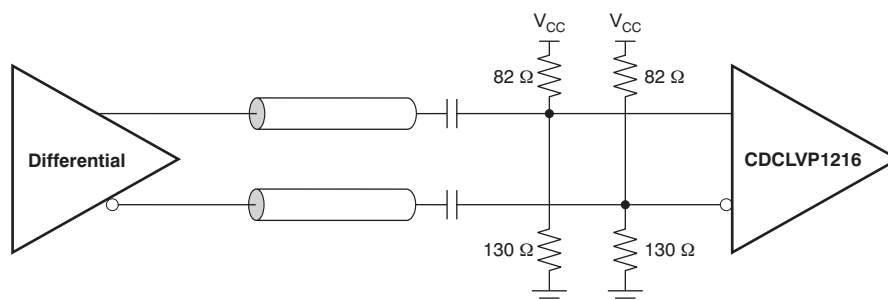


Figure 19. AC-Coupled Differential Inputs to CDCLVP1216 ($V_{CC} = 3.3$ V)

11 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The CDCLVP1216 is a low additive jitter LVPECL fanout buffer that can generate four copies of two selectable LVPECL, LVDS, or LVC MOS inputs. The CDCLVP1216 can accept reference clock frequencies up to 2 GHz while providing low output skew.

11.2 Typical Application

11.2.1 Fanout Buffer for Line Card Application

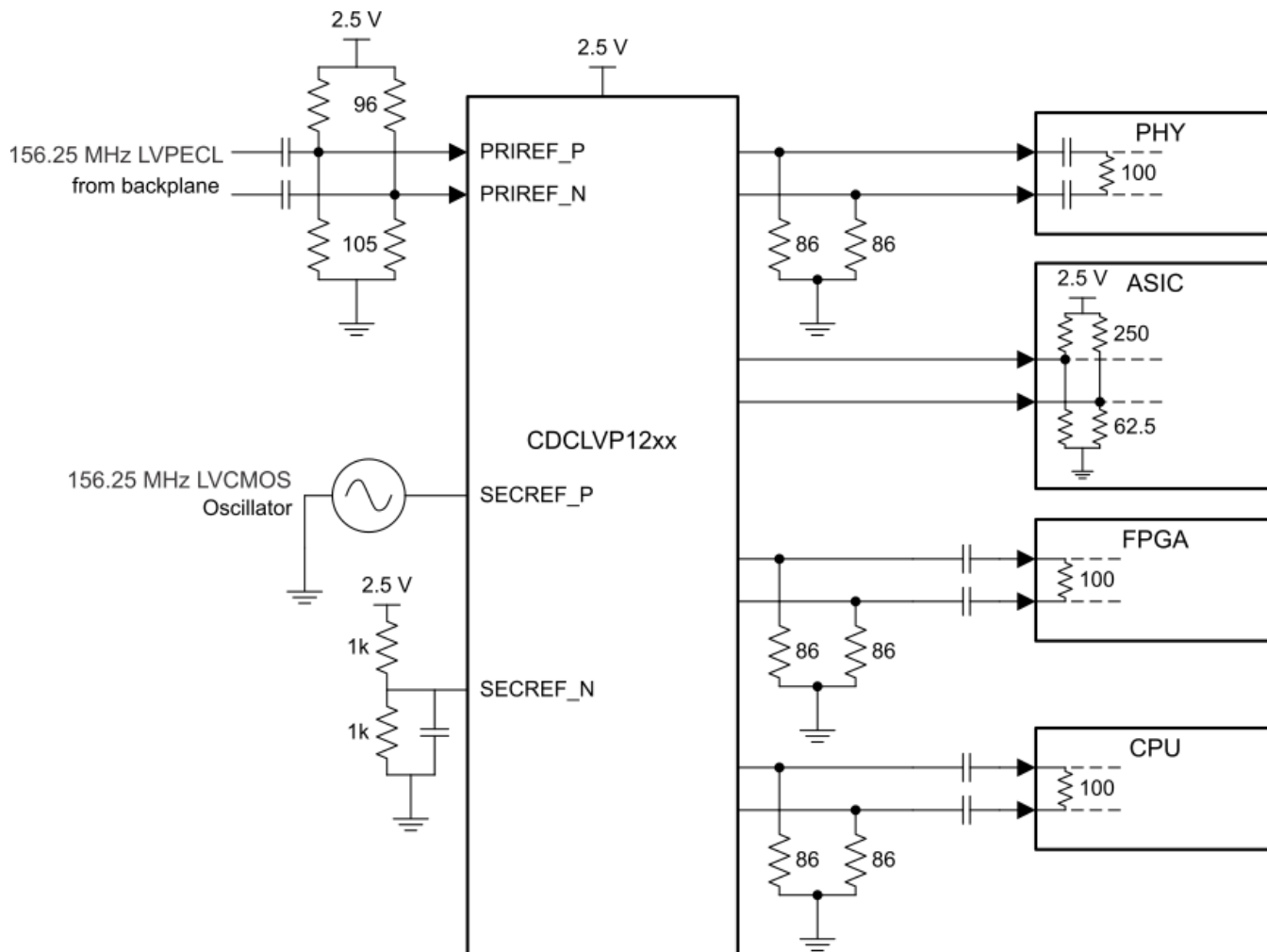


Figure 20. CDCLVP1216 Block Diagram

Typical Application (continued)

11.2.1.1 Design Requirements

The CDCLVP1216 shown in [Figure 20](#) is configured to be able to select two inputs, a 156.25 MHz LVPECL clock from the backplane, or a secondary 156.25 MHz LVCMOS 2.5V oscillator. Either signal can be then fanned out to desired devices, as shown.

The configuration example is driving 4 LVPECL receivers in a line card application with the following properties:

- The PHY device has internal AC coupling and appropriate termination and biasing. The CDCLVP1216 will need to be provided with 86 Ω emitter resistors near the driver for proper operation.
- The ASIC is capable of DC coupling with a 2.5V LVPECL driver such as the CDCLVP1216. This ASIC features internal termination so no additional components are needed.
- The FPGA requires external AC coupling but has internal termination. Again, 86 Ω emitter resistors are placed near the CDCLVP1216 and 0.1 μ F are placed to provide AC coupling. Similarly, the CPU is internally terminated and requires external AC coupling capacitors.

11.2.1.2 Detailed Design Procedure

Refer to [Input Termination](#) for proper input terminations, dependent on single ended or differential inputs.

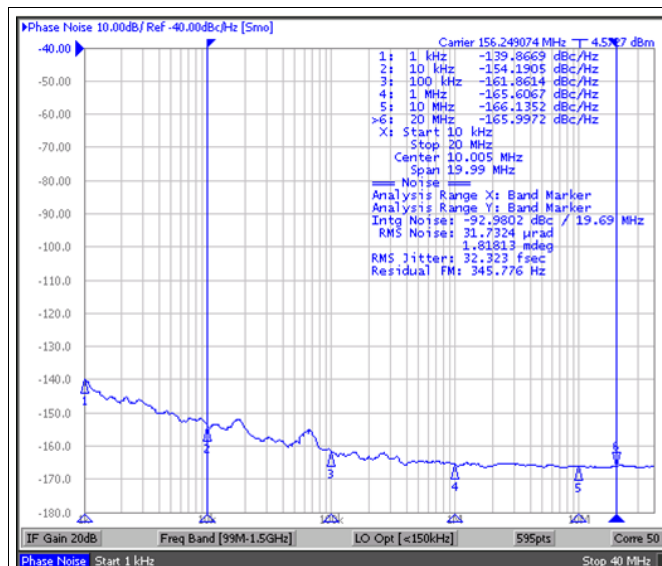
Refer to [LVPECL Output Termination](#) for output termination schemes depending on the receiver application.

Unused outputs can be left floating.

In this example, the PHY, ASIC, and FPGA/CPU require different schemes. Power supply filtering and bypassing is critical for low noise applications.

See [Power Supply Recommendations](#) for recommended filtering techniques. A reference layout is provided on the CDCLVP1216 Evaluation Module at [SCAU029](#).

11.2.2 Application Curves



Reference signal is low noise Crystek XO CPRO33.156.25

Figure 21. CDCLVP12xx Reference Phase Noise 32 fs rms (10 kHz to 20 MHz)

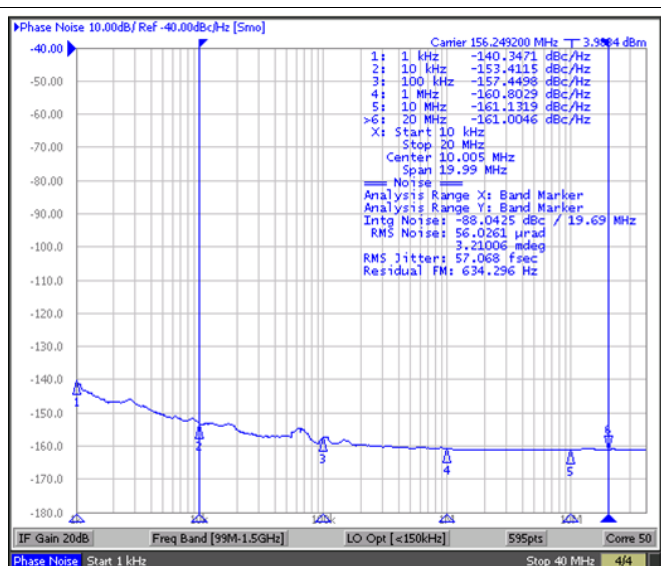


Figure 22. CDCLVP12xx Output Phase Noise 57 fs rms (10 kHz to 20 MHz)

The CDCLVP12xx's low additive noise can be shown in this line card application. The low noise 156.25 MHz XO with 32 fs RMS jitter drives the CDCLVP12xx, resulting in 57 fs RMS when integrated from 10 kHz to 20 MHz. The resultant additive jitter is a low 47 fs RMS for this configuration.

12 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply pins and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1- μF) bypass capacitors as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low dc resistance in order to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

Figure 23 illustrates this recommended power-supply decoupling method.

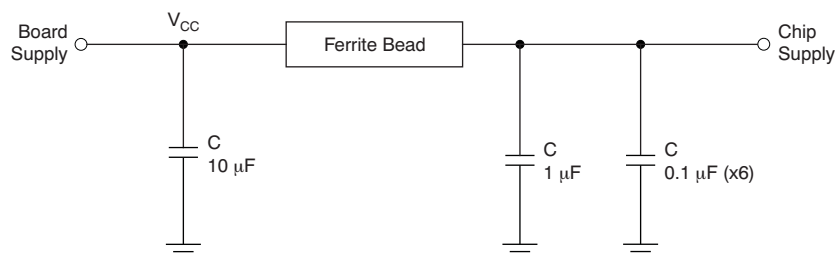


Figure 23. Power-Supply Decoupling

13 Layout

13.1 Layout Guidelines

Power consumption of the CDCLVP1216 can be high enough to require attention to thermal management. For reliability and performance reasons, the die temperature should be limited to a maximum of +125°C. That is, as an estimate, ambient temperature (T_A) plus device power consumption times $R_{\theta JA}$ should not exceed +125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. [Figure 24](#) shows a recommended land and via pattern.

13.2 Layout Example

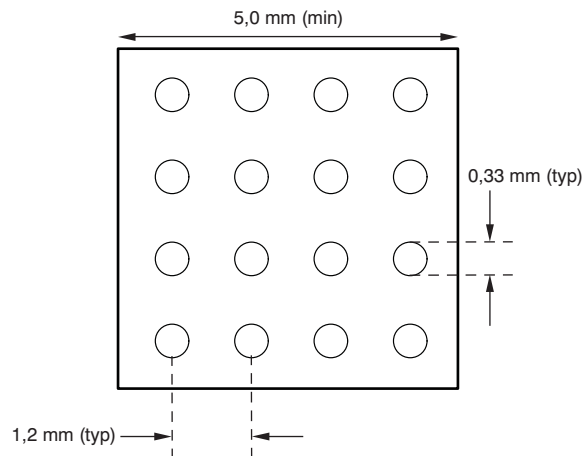


Figure 24. Recommended PCB Layout

14 Device and Documentation Support

14.1 Trademarks

All trademarks are the property of their respective owners.

14.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCLVP1216RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCLVP 1216	Samples
CDCLVP1216RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCLVP 1216	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVP1216RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CDCLVP1216RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

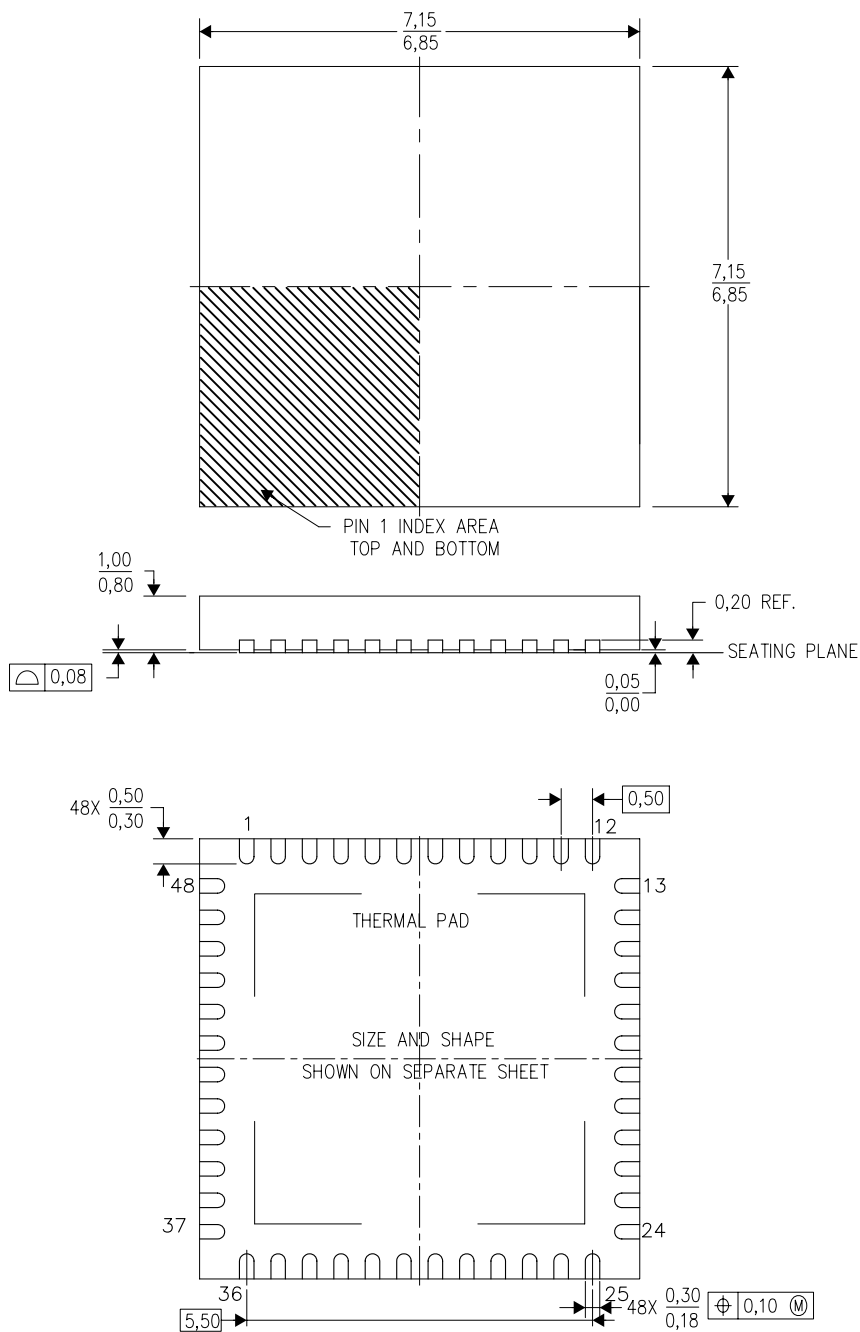


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVP1216RGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
CDCLVP1216RGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4204101/F 06/11

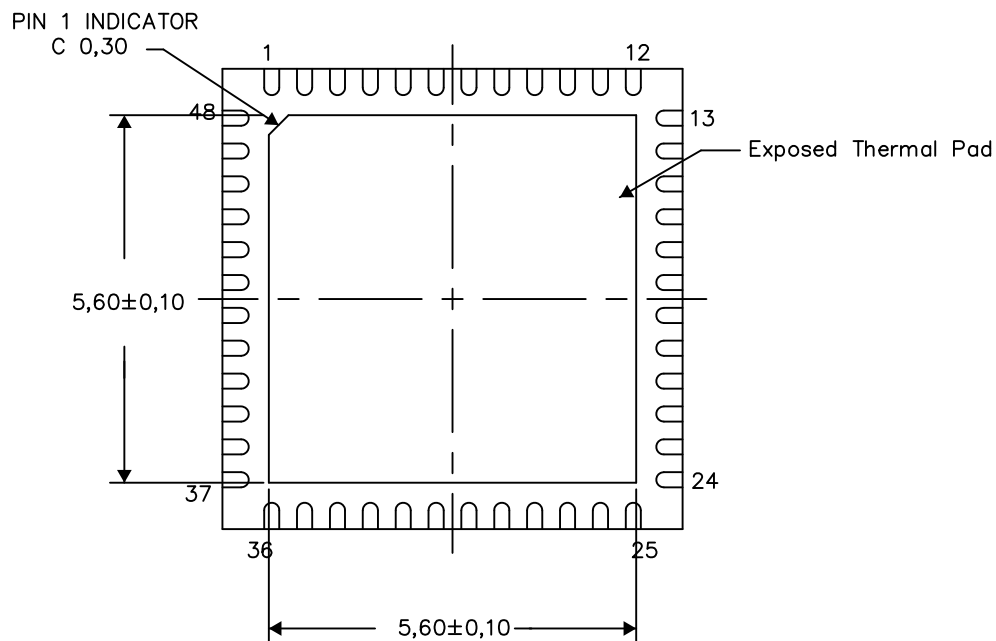
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

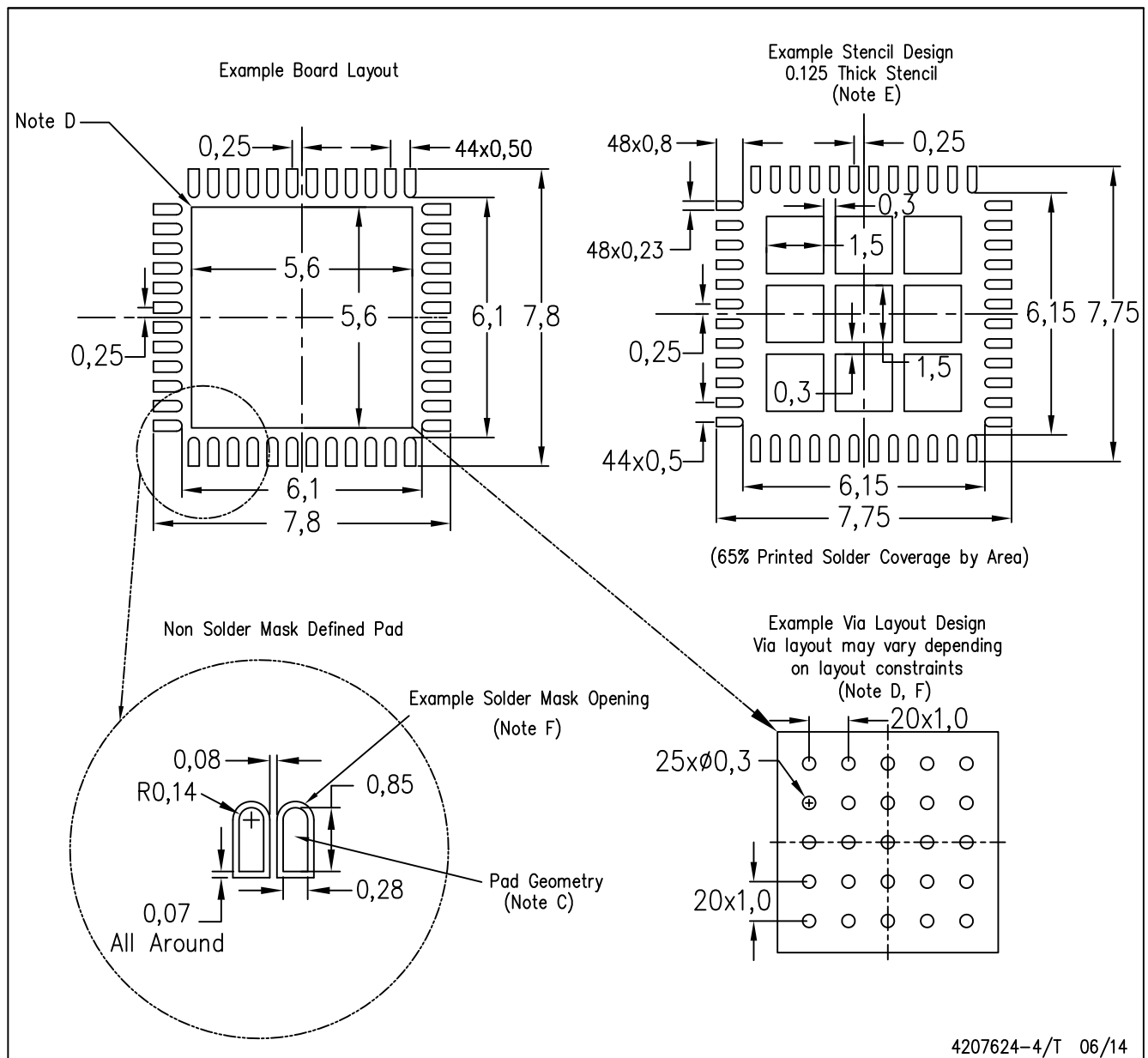


Bottom View

Exposed Thermal Pad Dimensions

4206354-5/Y 06/14

NOTE: All linear dimensions are in millimeters



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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