500 MHz to 1500 MHz Quadrature Modulator

ADL5371

FEATURES

Output frequency range: 500 MHz to 1500 MHz
Modulation bandwidth: >500 MHz (3 dB)
1 dB output compression: 14.4 dBm @ 900 MHz
Noise floor: −158.6 dBm/Hz @ 915 MHz
Sideband suppression: −55 dBc @ 900 MHz
Carrier feedthrough: −50 dBm @ 900 MHz
Single supply: 4.75 V to 5.25 V
24-lead LFCSP

APPLICATIONS

Cellular communication systems at 900 MHz
CDMA2000/GSM
WiMAX/broadband wireless access systems
Cable communication equipment
Satellite modems

FUNCTIONAL BLOCK DIAGRAM

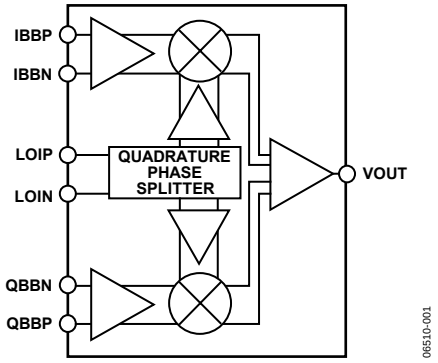

Figure 1.

GENERAL DESCRIPTION

The ADL5371 is a member of the fixed-gain quadrature modulator (F-MOD) family designed for use from 500 MHz to 1500 MHz. Its excellent phase accuracy and amplitude balance enable high performance intermediate frequency or direct radio frequency modulation for communication systems.

The ADL5371 provides a >500 MHz, 3 dB baseband bandwidth, making it ideally suited for use in broadband zero IF or low IF-to-RF applications and in broadband digital predistortion transmitters.

The ADL5371 accepts two differential baseband inputs and a single-ended local oscillator (LO) and generates a single-ended output.

The ADL5371 is fabricated using the Analog Devices, Inc. advanced silicon-germanium bipolar process. It is available in a 24-lead, exposed-paddle, Pb-free, LFCSP. Performance is specified over a −40°C to +85°C temperature range. A Pb-free evaluation board is available.

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

1/07—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V; T_A = 25°C; LO = 0 dBm[1] single-ended; baseband I/Q amplitude = 1.4 V p-p differential sine waves in quadrature with a 500 mV dc bias; baseband I/Q frequency (f_{BB}) = 1 MHz, LO frequency = 900 MHz, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
ADL5371	Low frequency		500		MHz
	High frequency		1500		MHz
Output Power, P_{OUT}			7.6		dBm
Output P1dB			14.4		dBm
Carrier Feedthrough			−50		dBm
Sideband Suppression			−55		dBc
Quadrature Error			0.1		Degrees
I/Q Amplitude Balance			−0.03		dB
Second Harmonic	$P_{OUT} - (f_{LO} + (2 \times f_{BB}))$, P_{OUT} = 6.2 dBm		−56		dBc
Third Harmonic	$P_{OUT} - (f_{LO} + (3 \times f_{BB}))$, P_{OUT} = 6.2 dBm		−50		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = 1.6 dBm per tone		57		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = 1.6 dBm per tone		27		dBm
Noise Floor	I/Q inputs = 0 V differential with a 500 mV common-mode bias, 20 MHz carrier offset		−158.6		dBm/Hz
GSM	6 MHz carrier offset, P_{OUT} = 5 dBm, P_{LO} = 6 dBm, LO = 940 MHz		−158.5		dBc/Hz
LO INPUTS					
LO Drive Level[1]	Characterization performed at typical level	−6	0	+6	dBm
Input Return Loss	See Figure 9 for the return loss vs. frequency plot		−7		dB
BASEBAND INPUTS	Pin IBBP, Pin IBBN, Pin QBBP, Pin QBBN				
I/Q Input Bias Level			500		mV
Input Bias Current	Current sourcing from each baseband input with a bias of 500 mV dc[2]		45		µA
Input Offset Current			0.1		µA
Differential Input Impedance			2900		kΩ
Bandwidth (0.1 dB)			70		MHz
Bandwidth (1 dB)			350		MHz
POWER SUPPLIES	Pin VPS1, Pin VPS2, Pin VPS3, Pin VPS4, and Pin VPS5				
Voltage		4.75		5.25	V
Supply Current			175	200	mA

[1] Higher LO drive reduces noise at a 6 MHz carrier offset in GSM applications.
[2] See the V-to-I Converter section for architecture information.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage VPOS	5.5 V
IBBP, IBBN, QBBP, QBBN	0 V to 2 V
LOIP and LOIN	13 dBm
Internal Power Dissipation	1188 mW
θ_{JA} (Exposed Paddle Soldered Down)	54°C/W
Maximum Junction Temperature	152°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

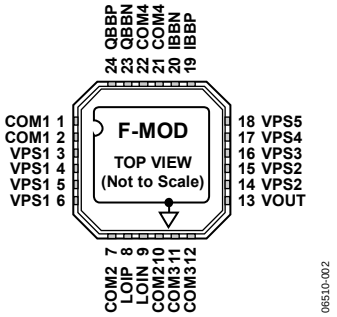


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2	COM1	Input Common Pins. Connect to ground plane via a low impedance path.
7, 10	COM2	Input Common Pins. Connect to ground plane via a low impedance path.
11, 12	COM3	Input Common Pins. Connect to ground plane via a low impedance path.
21, 22	COM4	Input Common Pins. Connect to ground plane via a low impedance path.
3 to 6	VPS1	Positive Supply Voltage Pins. All pins should be connected to the same supply (V_S). To ensure adequate external bypassing, connect 0.1 µF capacitors between each pin and ground. Adjacent power supply pins of the same name can share one capacitor (see Figure 23).
14, 15	VPS2	Positive Supply Voltage Pins. All pins should be connected to the same supply (V_S). To ensure adequate external bypassing, connect 0.1 µF capacitors between each pin and ground. Adjacent power supply pins of the same name can share one capacitor (see Figure 23).
16 to 18	VPS3 to VPS5	Positive Supply Voltage Pins. All pins should be connected to the same supply (V_S). To ensure adequate external bypassing, connect 0.1 µF capacitors between each pin and ground. Adjacent power supply pins of the same name can share one capacitor (see Figure 23).
8, 9	LOIP, LOIN	50 Ω Single-Ended Local Oscillator Input. Internally dc-biased. Pins must be ac-coupled. AC-couple LOIN to ground and drive LO through LOIP.
13	VOUT	Device Output. Single-ended RF output. Pin should be ac-coupled to the load. The output is ground referenced.
19, 20, 23, 24	IBBP, IBBN, QBBN, QBBP	Differential In-Phase and Quadrature Baseband Inputs. These high impedance inputs must be dc-biased to 500 mV dc and must be driven from a low impedance source. Nominal characterized ac signal swing is 700 mV p-p on each pin. This results in a differential drive of 1.4 V p-p with a 500 mV dc bias. These inputs are not self-biased and must be externally biased.
	Exposed Paddle	Connect to ground plane via a low impedance path.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V; T_A = 25°C; LO = 0 dBm single-ended; baseband I/Q amplitude = 1.4 V p-p differential sine waves in quadrature with a 500 mV dc bias; baseband I/Q frequency (f_{BB}) = 1 MHz, unless otherwise noted.

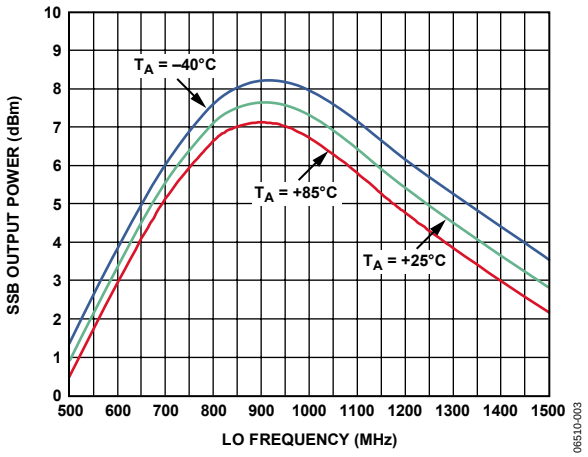


Figure 3. Single Sideband (SSB) Output Power (P_{OUT}) vs. LO Frequency (f_{LO}) and Temperature

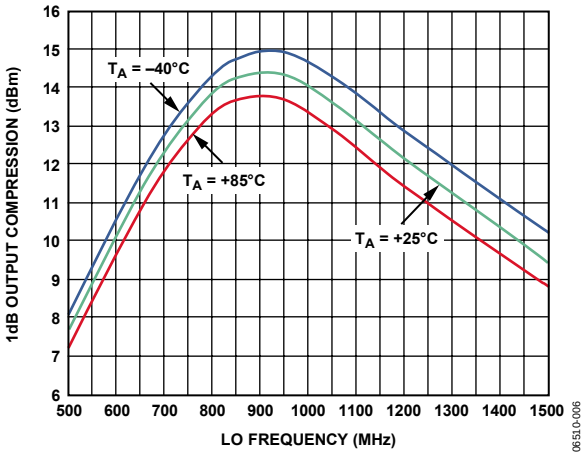


Figure 6. SSB Output 1 dB Compression Point (OP1dB) vs. f_{LO} and Temperature

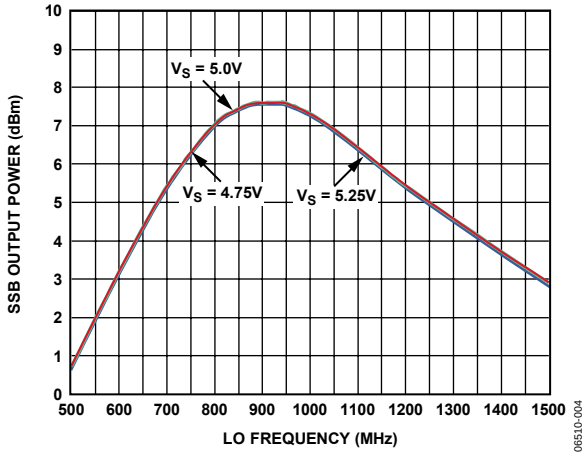


Figure 4. Single Sideband (SSB) Output Power (P_{OUT}) vs. LO Frequency (f_{LO}) and Supply

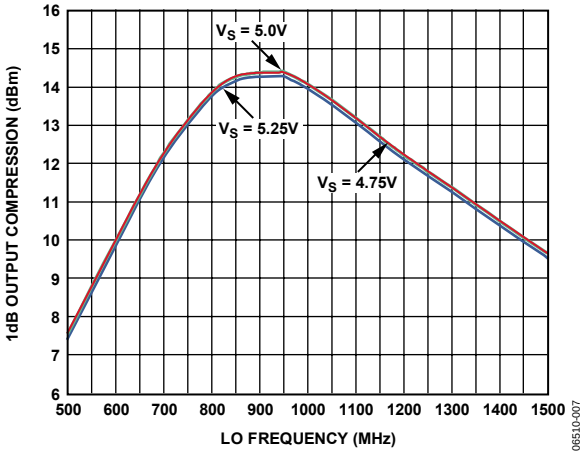


Figure 7. SSB Output 1 dB Compression Point (OP1dB) vs. f_{LO} and Supply

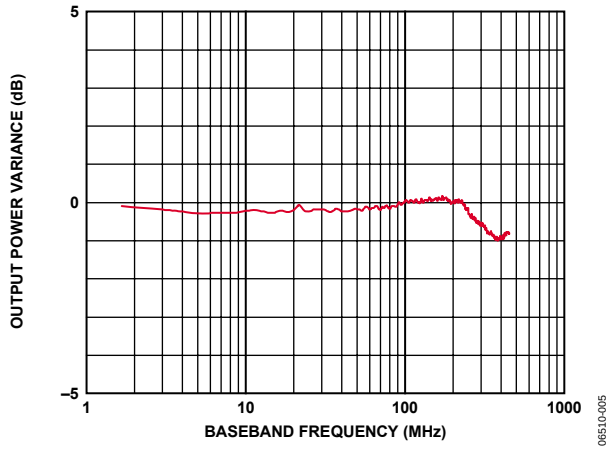


Figure 5. I/Q Input Bandwidth Normalized to Gain @ 1 MHz (f_{LO} = 900 MHz)

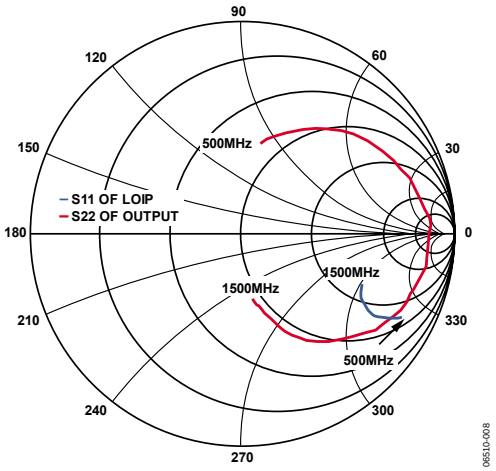


Figure 8. Smith Chart of LOIP S11 and VOUT S22 (f_{LO} from 500 MHz to 1500 MHz)

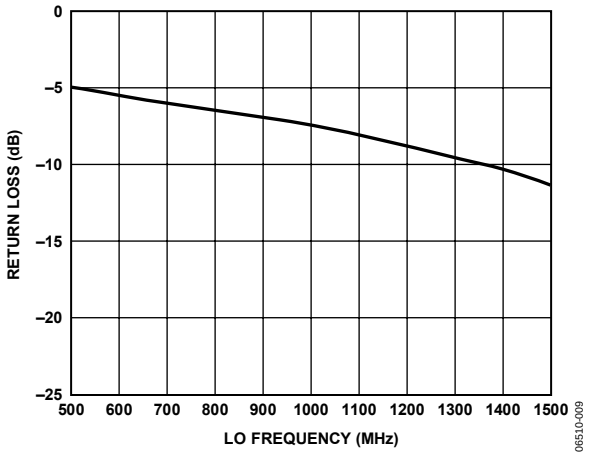


Figure 9. Return Loss (S11) of LOIP

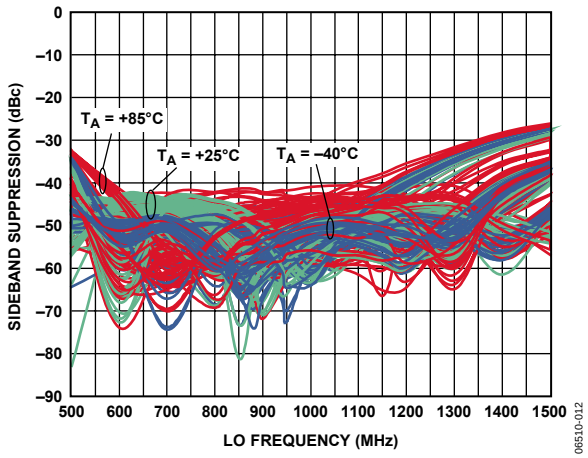


Figure 12. Sideband Suppression vs. f_{LO} and Temperature (Multiple Devices Shown)

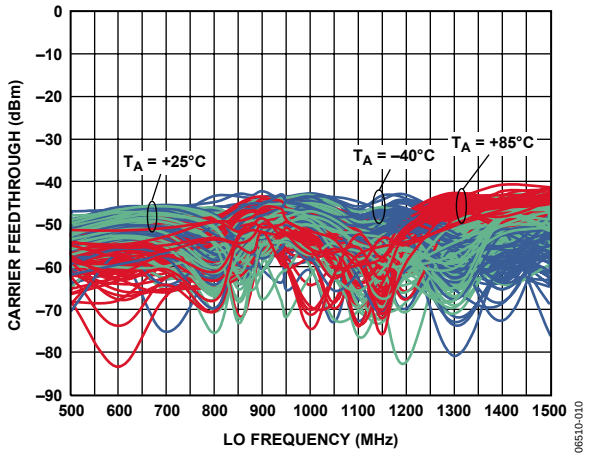


Figure 10. Carrier Feedthrough vs. f_{LO} and Temperature (Multiple Devices Shown)

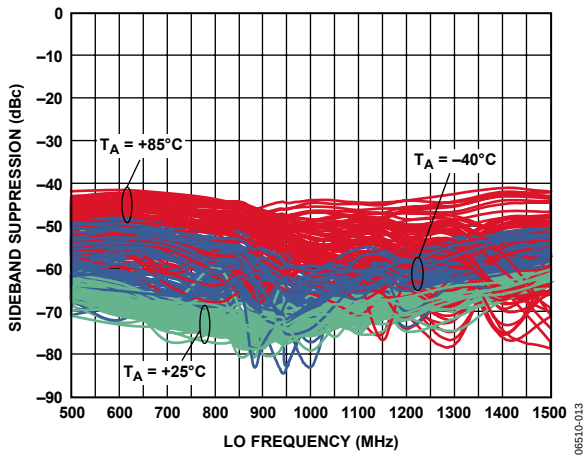


Figure 13. Sideband Suppression vs. f_{LO} and Temperature After Nulling at 25°C (Multiple Devices Shown)

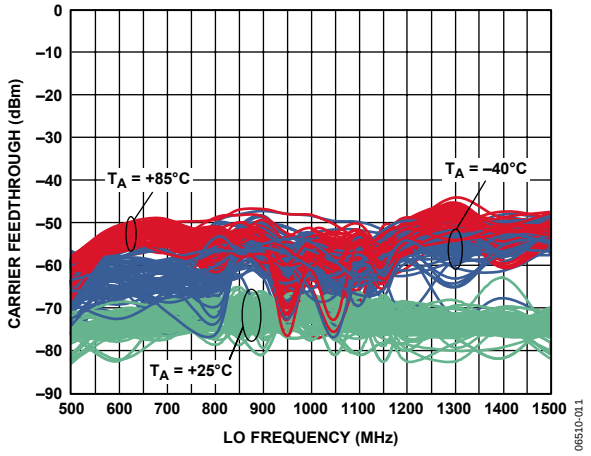


Figure 11. Carrier Feedthrough vs. f_{LO} and Temperature After Nulling at 25°C (Multiple Devices Shown)

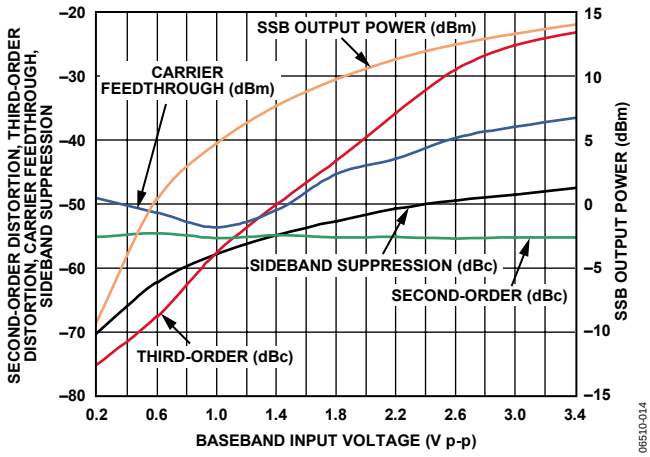


Figure 14. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. Baseband Differential Input Level (f_{LO} = 900 MHz)

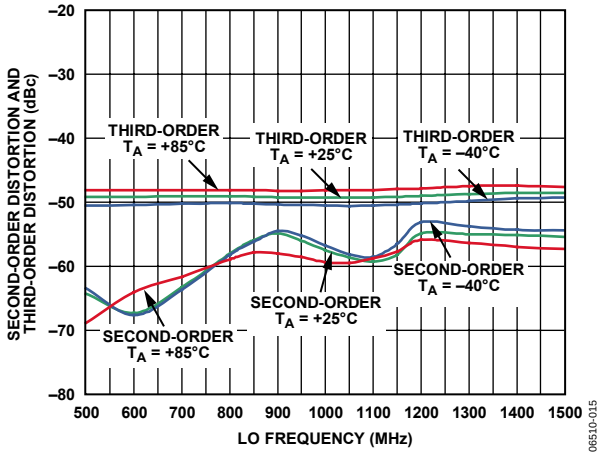


Figure 15. Second- and Third-Order Distortion vs. f_{LO} and Temperature (Baseband I/Q Amplitude = 1.4 V p-p Differential)

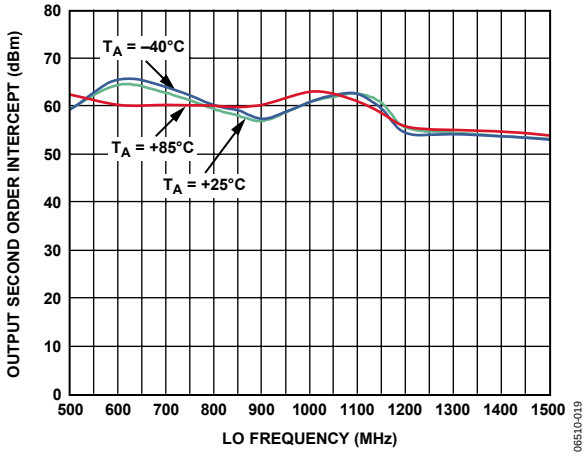


Figure 18. OIP2 vs. Frequency and Temperature

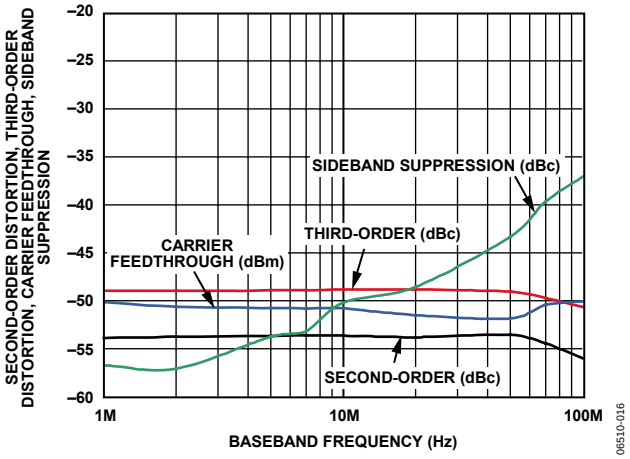


Figure 16. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. f_{BB} (f_{LO} = 900 MHz)

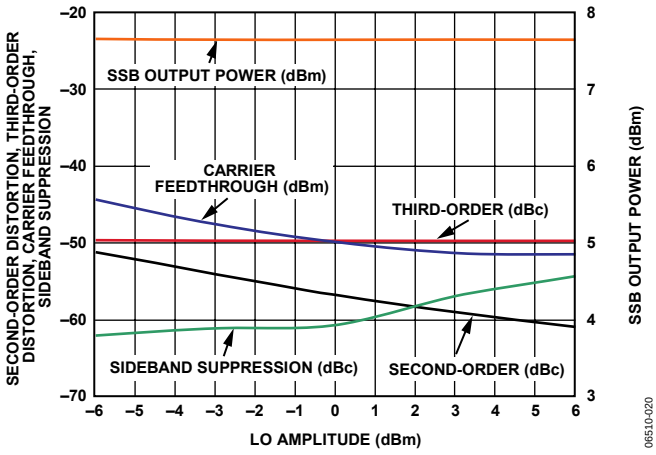


Figure 19. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. LO Amplitude (f_{LO} = 900 MHz)

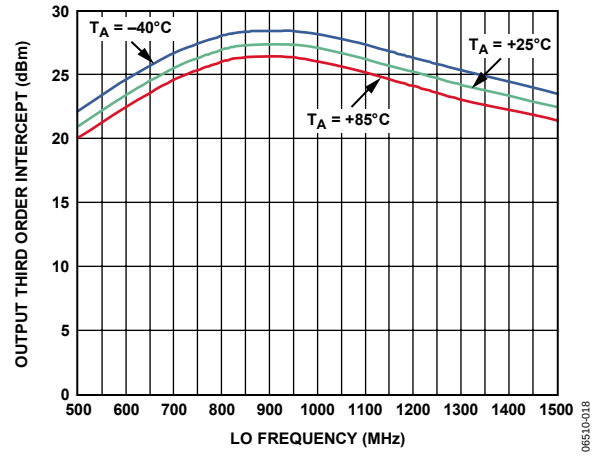


Figure 17. OIP3 vs. Frequency and Temperature

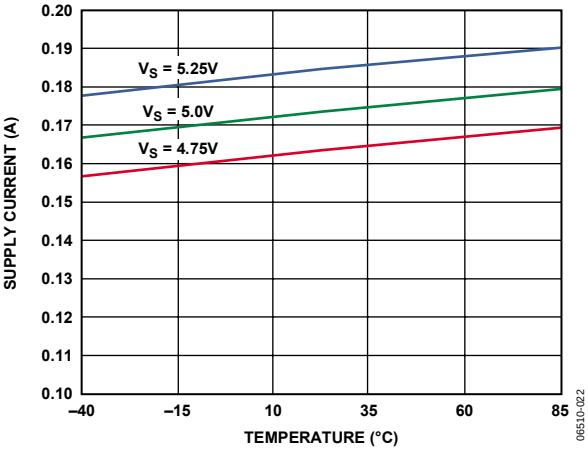


Figure 20. Power Supply Current vs. Temperature

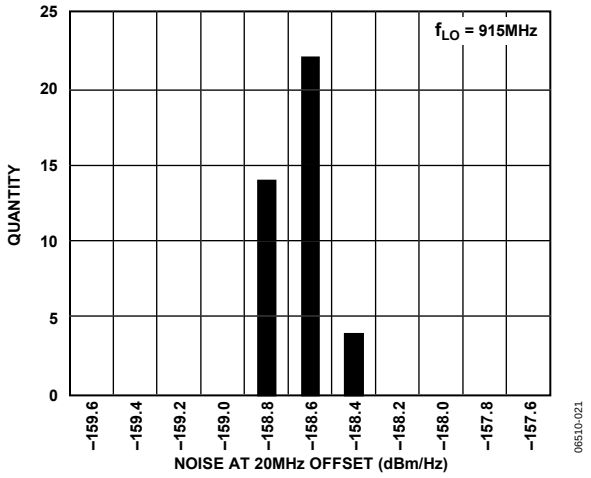


Figure 21. 20 MHz Offset Noise Floor Distribution at f_{LO} = 915 MHz (I/Q Amplitude = 0 mV p-p with 500 mV dc Bias)

THEORY OF OPERATION

CIRCUIT DESCRIPTION

Overview

The ADL5371 can be divided into five circuit blocks: the LO interface, the baseband voltage-to-current (V-to-I) converter, the mixers, the differential-to-single-ended (D-to-S) converter, and the bias circuit. A detailed block diagram of the device is shown in Figure 22.

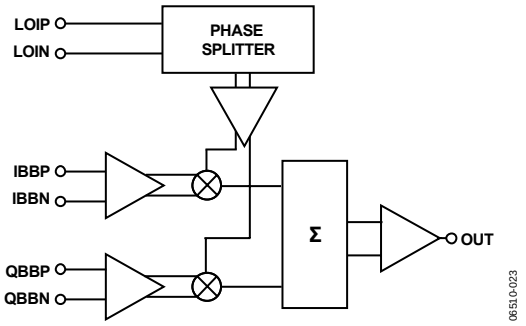


Figure 22. Block Diagram

The LO interface generates two LO signals in quadrature. These signals are used to drive the mixers. The I/Q baseband input signals are converted to currents by the V-to-I stages, which then drive the two mixers. The outputs of these mixers combine to feed the output balun, which provides a single-ended output interface. The bias cell generates a reference current for the V-to-I stage.

LO Interface

The LO interface consists of a polyphase quadrature splitter followed by a limiting amplifier. The LO input impedance is set by the polyphase. The LO can be driven either single-ended or differentially. When driven single-ended, the LOIN pin should be ac-grounded via a capacitor. Each quadrature LO signal then passes through a limiting amplifier that provides the mixer with a limited drive signal.

V-to-I Converter

The differential baseband inputs (QBBP, QBBN, IBBN, and IBBP) consist of the bases of PNP transistors, which present a high impedance. The voltages applied to these pins drive the V-to-I stage that converts baseband voltages into currents. The differential output currents of the V-to-I stages feed each of their respective Gilbert-cell mixers. The dc common-mode voltage at the baseband inputs sets the currents in the two mixer cores. Varying the baseband common-mode voltage varies the current in the mixer and affects overall modulator performance. The recommended dc voltage for the baseband common-mode voltage is 500 mV dc.

Mixers

The ADL5371 has two double-balanced mixers: one for the in-phase channel (I channel) and one for the quadrature channel (Q channel). Both mixers are based on the Gilbert-cell design of four cross-connected transistors. The output currents from the two mixers sum together into an on-chip balun, which converts the differential signal to single-ended.

D-to-S Stage

The output D-to-S stage consists of an on-chip balun that converts the differential signal to a single-ended signal. The balun presents high impedance to the output (VOUT). Therefore, a matching network may be needed at the output for optimal power transfer.

Bias Circuit

An on-chip band gap reference circuit is used to generate a proportional-to-absolute temperature (PTAT) reference current for the V-to-I stage.

BASIC CONNECTIONS

Figure 23 shows the basic connections for the ADL5371.

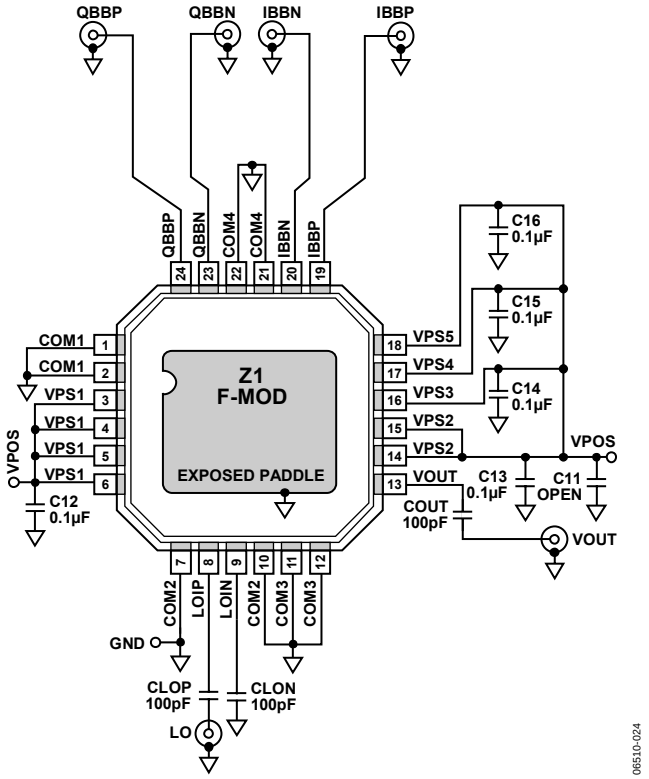


Figure 23. Basic Connections for the ADL5371

POWER SUPPLY AND GROUNDING

All the VPS pins must be connected to the same 5 V source. Adjacent pins of the same name can be tied together and decoupled with a 0.1 µF capacitor. These capacitors should be located as close as possible to the device. The power supply can range between 4.75 V and 5.25 V.

The COM1 pin, COM2 pin, COM3 pin, and COM4 pin should be tied to the same ground plane through low impedance paths. The exposed paddle on the underside of the package should also be soldered to a low thermal and electrical impedance ground plane. If the ground plane spans multiple layers on the circuit board, they should be stitched together with nine vias under the exposed paddle. The Application Note AN-772 discusses the thermal and electrical grounding of the LFCSP in detail.

BASEBAND INPUTS

The baseband inputs QBBP, QBBN, IBBP, and IBBN must be driven from a differential source. The nominal drive level of 1.4 V p-p differential (700 mV p-p on each pin) should be biased to a common-mode level of 500 mV dc.

The dc common-mode bias level for the baseband inputs range from 400 mV to 600 mV. This results in a reduction in the usable input ac swing range. The nominal dc bias of 500 mV allows for the largest ac swing, limited on the bottom end by the ADL5371 input range and on the top end by the output compliance range on most DACs from Analog Devices.

LO INPUT

A single-ended LO signal should be applied to the LOIP pin through an ac coupling capacitor. The recommended LO drive power is 0 dBm. The LO return pin, LOIN, should be ac-coupled to ground through a low impedance path.

The nominal LO drive of 0 dBm can be increased to up to 7 dBm to realize an improvement in the noise performance of the modulator (see Figure 33). This improvement is tempered by degradation in the sideband suppression performance (see Figure 19) and, therefore, should be used judiciously. If the LO source cannot provide the 0 dBm level, operation at a reduced power below 0 dBm is acceptable. Reduced LO drive results in slightly increased modulator noise. The effect of LO power on sideband suppression and carrier feedthrough is shown in Figure 19. The effect of LO power on GSM noise is shown in Figure 33.

RF OUTPUT

The RF output is available at the VOUT pin (Pin 13). The VOUT pin connects to an internal balun, which is capable of driving a 50 Ω load. For applications requiring 50 Ω output impedance, external matching is needed (see Figure 8 for S22 performance). The internal balun provides a low dc path to ground. In most situations, the VOUT pin should be ac-coupled to the load.

OPTIMIZATION

The carrier feedthrough and sideband suppression performance of the ADL5371 can be improved by using optimization techniques.

Carrier Feedthrough Nulling

Carrier feedthrough results from minute dc offsets that occur between each of the differential baseband inputs. In an ideal modulator, the quantities ($V_{IOPP} - V_{IOPN}$) and ($V_{QOPP} - V_{QOPN}$) are equal to zero, which results in no carrier feedthrough. In a real modulator, those two quantities are nonzero, and, when mixed with the LO, they result in a finite amount of carrier feedthrough. The ADL5371 is designed to provide a minimal amount of carrier feedthrough. Should even lower carrier feedthrough levels be required, minor adjustments can be made to the ($V_{IOPP} - V_{IOPN}$) and ($V_{QOPP} - V_{QOPN}$) offsets. The I-channel offset is held constant while the Q-channel offset is varied until a minimum carrier feedthrough level is obtained. The Q-channel offset required to achieve this minimum is held constant, while the offset on the I-channel is adjusted until a new minimum is reached. Through two iterations of this process, the carrier feedthrough can be reduced to as low as the output noise. The ability to null is sometimes limited by the resolution of the offset adjustment. Figure 24 shows the relationship of carrier feedthrough vs. dc offset as null.

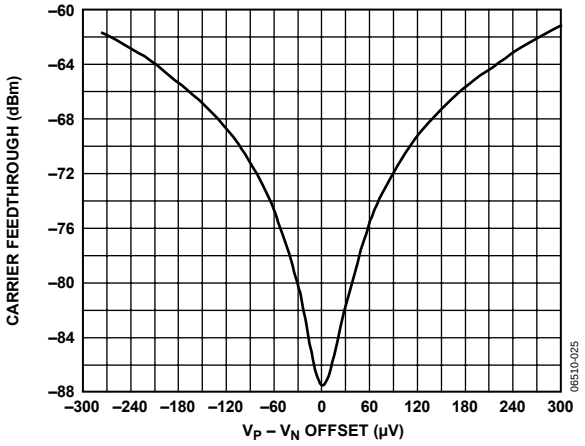


Figure 24. Typical Carrier Feedthrough vs. DC Offset Voltage

Note that throughout the nulling process, the dc bias for the baseband inputs remains at 500 mV. When no offset is applied,

$V_{IOPP} = V_{IOPN} = 500$ mV, or
$V_{IOPP} - V_{IOPN} = V_{IOS} = 0$ V

When an offset of $+V_{IOS}$ is applied to the I-channel inputs,

$V_{IOPP} = 500$ mV $+ V_{IOS}/2$, and
$V_{IOPN} = 500$ mV $- V_{IOS}/2$, such that
$V_{IOPP} - V_{IOPN} = V_{IOS}$

The same applies to the Q channel inputs.

It is often desirable to perform a one-time carrier null calibration. This is usually performed at a single frequency. Figure 25 shows how carrier feedthrough varies with LO frequency over a range of ±50 MHz on either side of a null at 940 MHz.

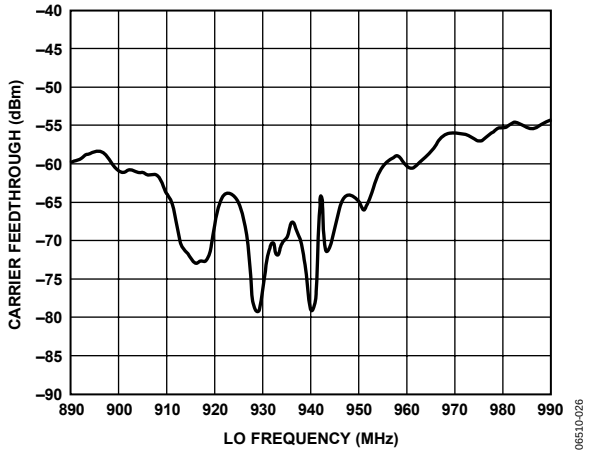


Figure 25. Carrier Feedthrough vs. Frequency After Nulling at 940 MHz

Sideband Suppression Optimization

Sideband suppression results from relative gain and relative phase offsets between the I/Q channels and can be suppressed through adjustments to those two parameters. Figure 26 illustrates how sideband suppression is affected by the gain and phase imbalances.

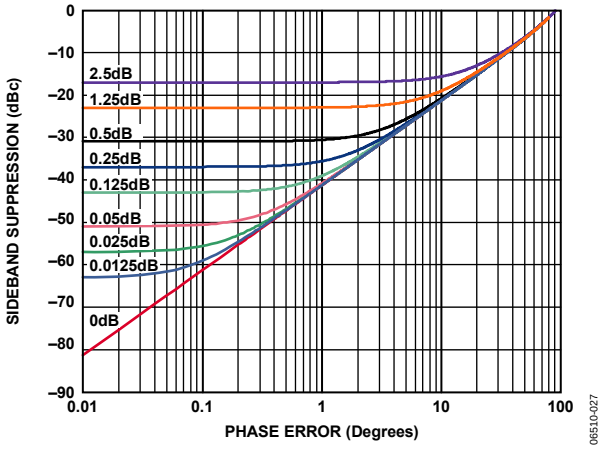


Figure 26. Sideband Suppression vs. Quadrature Phase Error for Various Quadrature Amplitude Offsets

Figure 26 underlines the fact that adjusting only one parameter improves the sideband suppression only to a point, unless the other parameter is also adjusted. For example, if the amplitude offset is 0.25 dB, improving the phase imbalance more than 1° does not yield any improvement in the sideband suppression. For optimum sideband suppression, an iterative adjustment between phase and amplitude is required.

The sideband suppression nulling can be performed either through adjusting the gain for each channel or through the modification of the phase and gain of the digital data coming from the digital signal processor.

APPLICATIONS INFORMATION

DAC MODULATOR INTERFACING

The ADL5371 is designed to interface with minimal components to members of the Analog Devices family of DACs. These DACs feature an output current swing from 0 to 20 mA, and the interface described in this section can be used with any DAC that has a similar output.

Driving the ADL5371 with a TxDAC®

An example of the interface using the AD9779 TxDAC is shown in Figure 27. The baseband inputs of the ADL5371 require a dc bias of 500 mV. The average output current on each AD9779 output is 10 mA. Therefore, a single 50 Ω resistor to ground from each DAC output results in an average current of 10 mA flowing through each resistor, thus producing the desired 500 mV dc bias for the inputs to the ADL5371.

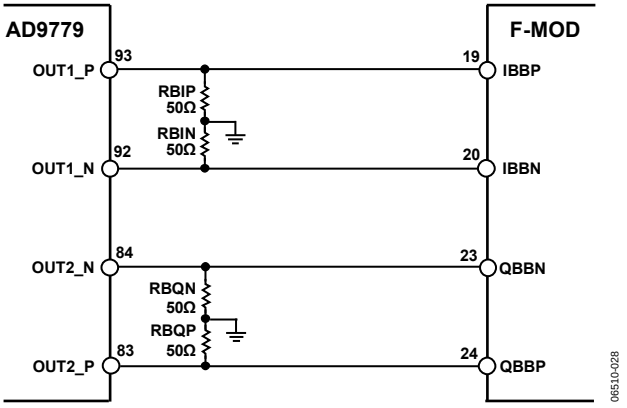


Figure 27. Interface Between the AD9779 and ADL5371 with 50 Ω Resistors to Ground to Establish the 500 mV dc Bias for the ADL5371 Baseband Inputs

The AD9779 output currents have a swing that ranges from 0 to 20 mA. With the 50 Ω resistors in place, the ac voltage swing going into the ADL5371 baseband inputs ranges from 0 V to 1 V. A full-scale sine wave out of the AD9779 can be described as a 1 V p-p single-ended (or 2 V p-p differential) sine wave with a 500 mV dc bias.

LIMITING THE AC SWING

There are situations when it is desirable to reduce the ac voltage swing for a given DAC output current. This can be achieved through the addition of another resistor to the interface. This resistor is placed in shunt between each side of the differential pair, as shown in Figure 28. It has the effect of reducing the ac swing without changing the dc bias already established by the 50 Ω resistors.

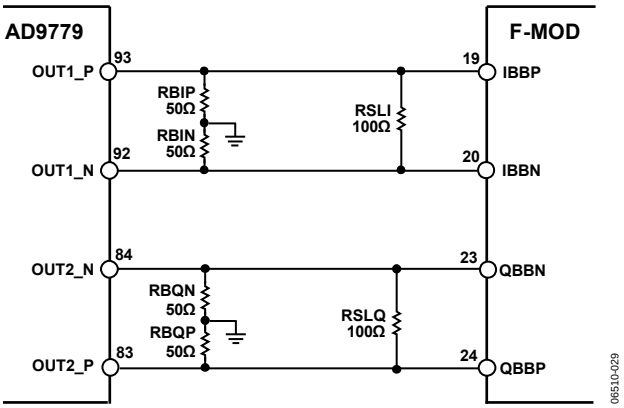


Figure 28. AC Voltage Swing Reduction Through the Introduction of a Shunt Resistor Between the Differential Pair

The value of this ac voltage swing-limiting resistor is chosen based on the desired ac voltage swing. Figure 29 shows the relationship between the swing-limiting resistor and the peak-to-peak ac swing that it produces when 50 Ω bias-setting resistors are used.

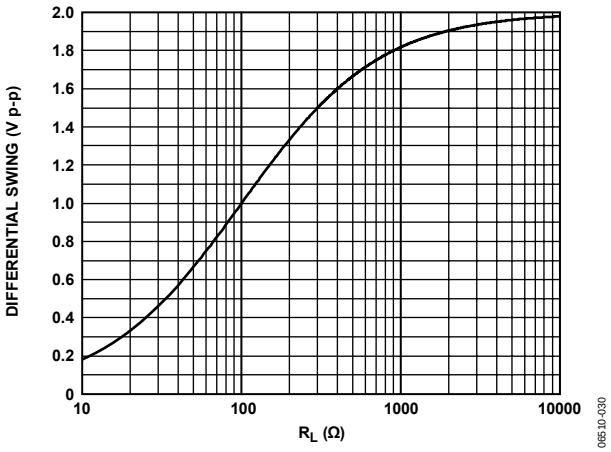


Figure 29. Relationship Between the AC Swing-Limiting Resistor and the Peak-to-Peak Voltage Swing with 50 Ω Bias-Setting Resistors

FILTERING

It is necessary to low-pass filter the DAC outputs to remove images when driving a modulator. The interface for setting up the biasing and ac swing discussed in the Limiting the AC Swing section lends itself well to the introduction of such a filter. The filter can be inserted between the dc bias-setting resistors and the ac swing-limiting resistor. Doing so establishes the input and output impedances for the filter.

Figure 30 shows an example of a third-order elliptical filter with a 3 dB frequency of 3 MHz. Matching input and output impedances makes the filter design easier, so the shunt resistor chosen is 100 Ω, producing an ac swing of 1 V p-p differential.

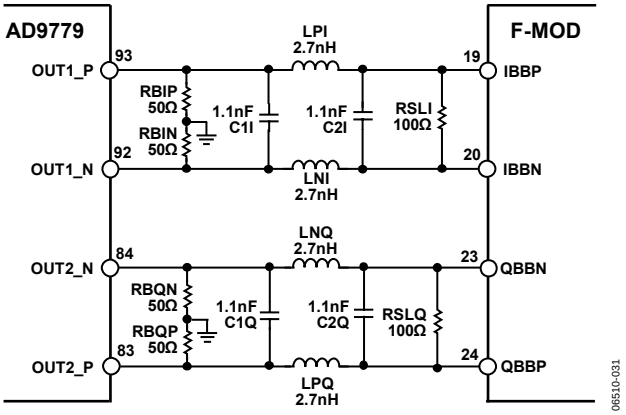


Figure 30. DAC Modulator Interface with 3 MHz Third-Order, Low-Pass Filter

USING THE AD9779 AUXILIARY DAC FOR CARRIER FEEDTHROUGH NULLING

The AD9779 features an auxiliary DAC that can be used to inject small currents into the differential outputs for each main DAC channel. This feature can be used to produce the small offset voltages necessary to null out the carrier feedthrough from the modulator. Figure 31 shows the interface required to use the auxiliary DACs. This adds four resistors to the interface.

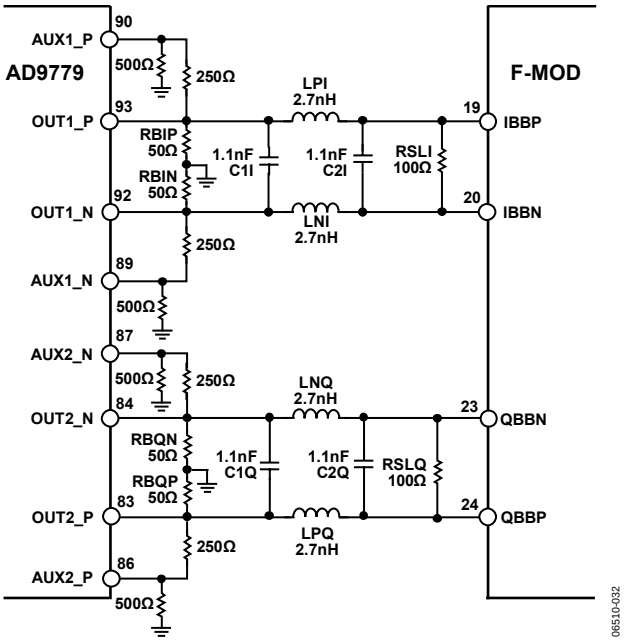


Figure 31. DAC Modulator Interface with Auxiliary DAC Resistors

GSM OPERATION

Figure 32 shows the GSM/EDGE EVM and spectral mask performance vs. output power for the ADL5371 at 940 MHz. For a given LO amplitude, the performance is independent of output power.

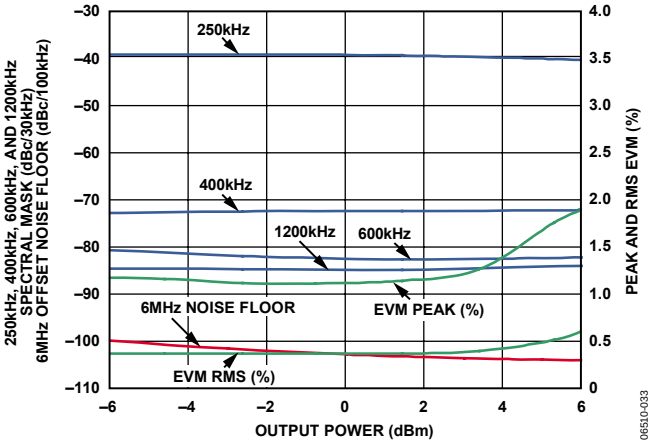


Figure 32. GSM/EDGE (8 PSK) EVM and Spectral Performance vs. Channel Power at 940 MHz vs. Output Power; LO Power = 0 dBm

Figure 33 shows the GSM/EDGE EVM and 6 MHz offset noise vs. LO amplitude at 940 MHz with an output power of 5 dBm. Increasing the LO drive level improves the noise performance with minimal degradation in EVM performance.

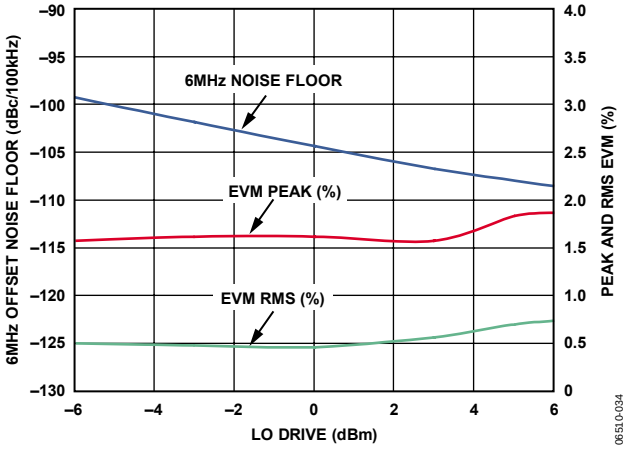


Figure 33. GSM/EDGE (8 PSK) EVM, Spectral Performance, and 6 MHz Noise Floor vs. LO Power at 940 MHz; Output Power = 5 dBm

Figure 33 illustrates that an LO amplitude of 3 dBm provides the ideal operating point for noise and EVM for a GSM/EDGE signal at 940 MHz.

LO GENERATION USING PLLS

Analog Devices has a line of PLLs that can be used for generating the LO signal. Table 4 lists the PLLs together with their maximum frequency and phase noise performance.

Table 4. ADI PLL Selection Table

Part	Frequency f_{IN} (MHz)	Phase Noise @ 1 kHz Offset and 200 kHz PFD (dBc/Hz)
ADF4110	550	–91 @ 540 MHz
ADF4111	1200	–87 @ 900 MHz
ADF4112	3000	–90 @ 900 MHz
ADF4113	4000	–91 @ 900 MHz
ADF4116	550	–89 @ 540 MHz
ADF4117	1200	–87 @ 900 MHz
ADF4118	3000	–90 @ 900 MHz

The ADF4360 comes as a family of chips, with nine operating frequency ranges. One is chosen, depending on the local oscillator frequency required. While the use of the integrated synthesizer may come at the expense of slightly degraded noise performance from the ADL5371, it can be a cheaper alternative to a separate PLL and VCO solution. Table 5 shows the options available.

Table 5. ADF4360 Family Operating Frequencies

Part	Output Frequency Range (MHz)
ADF4360-0	2400 to 2725
ADF4360-1	2050 to 2450
ADF4360-2	1850 to 2150
ADF4360-3	1600 to 1950
ADF4360-4	1450 to 1750
ADF4360-5	1200 to 1400
ADF4360-6	1050 to 1250
ADF4360-7	350 to 1800
ADF4360-8	65 to 400

TRANSMIT DAC OPTIONS

The AD9779 recommended in the previous sections of this data sheet is by no means the only DAC that can be used to drive the ADL5371. There are other appropriate DACs, depending on the level of performance required. Table 6 lists the dual TxDACs offered by Analog Devices.

Table 6. Dual TxDAC Selection Table

Part	Resolution (Bits)	Update Rate (MSPS Minimum)
AD9709	8	125
AD9761	10	40
AD9763	10	125
AD9765	12	125
AD9767	14	125
AD9773	12	160
AD9775	14	160
AD9777	16	160
AD9776	12	1000
AD9778	14	1000
AD9779	16	1000

All DACs listed have nominal bias levels of 0.5 V and use the same simple DAC-modulator interface that is shown in Figure 29.

MODULATOR/DEMODULATOR OPTIONS

Table 7 lists other Analog Devices modulators and demodulators.

Table 7. Modulator/Demodulator Options

Part	Modulator/ Demodulator	Frequency Range (MHz)	Comments
AD8345	Modulator	140 to 1000	
AD8346	Modulator	800 to 2500	
AD8349	Modulator	700 to 2700	
ADL5390	Modulator	20 to 2400	External quadrature
ADL5385	Modulator	50 to 2200	
ADL5370	Modulator	300 to 1000	
ADL5372	Modulator	1500 to 2500	
ADL5373	Modulator	2300 to 3000	
ADL5374	Modulator	3000 to 4000	
AD8347	Demodulator	800 to 2700	
AD8348	Demodulator	50 to 1000	
AD8340	Vector modulator	700 to 1000	
AD8341	Vector modulator	1500 to 2400	

EVALUATION BOARD

Populated RoHS-compliant evaluation boards are available for evaluation of the ADL5371. The ADL5371 package has an exposed paddle on the underside. This exposed paddle must be soldered to the board (see the Power Supply and Grounding section). The evaluation board is designed without any components on the underside so heat can be applied to the underside for easy removal and replacement of the ADL5371.

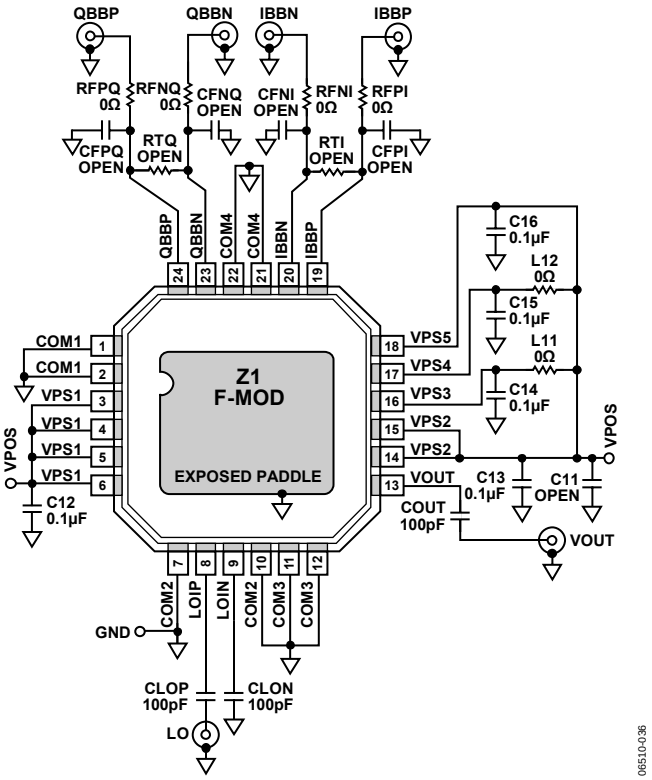


Figure 34. ADL5371 Evaluation Board Schematic

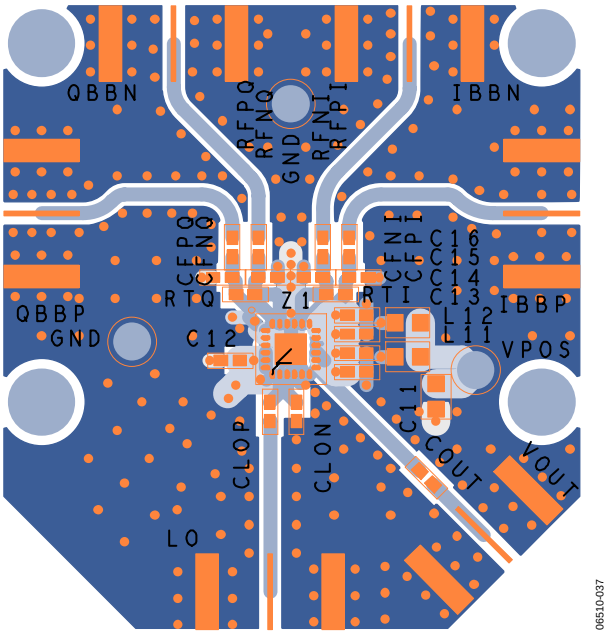


Figure 35. Evaluation Board Layout, Top Layer

Table 8. Evaluation Board Configuration Options

Component	Description	Default Condition
VPOS, GND	Power Supply and Ground Clip Leads.	Not applicable
RFPI, RFNI, RFPQ, RFNQ, CFPI, CFNI, CFPQ, CFNQ, RTQ, RTI	Baseband Input Filters. These components can be used to implement a low-pass filter for the baseband signals. See the Filtering section.	RFNQ, RFPQ, RFNI, RFPI = 0 Ω (0402) CFNQ, CFPQ, CFNI, CFPI = Open (0402) RTQ, RTI = Open (0402)

CHARACTERIZATION SETUP

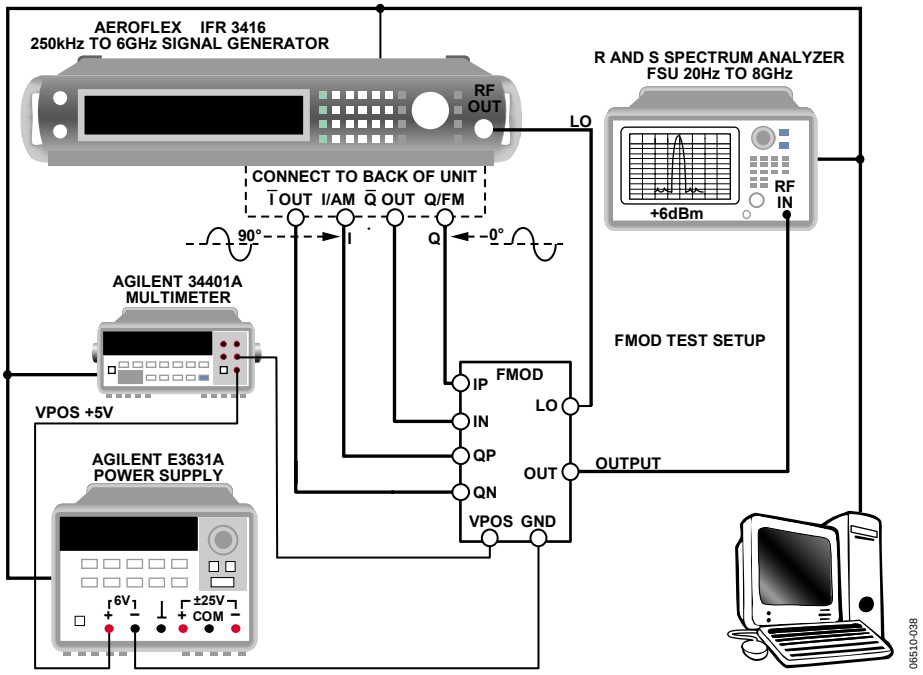


Figure 36. Characterization Bench Setup

The primary setup used to characterize the ADL5371 is shown in Figure 36. This setup was used to evaluate the product as a single-sideband modulator. The Aeroflex signal generator supplied the LO and differential I/Q baseband signals to the device under test, DUT. The typical LO drive was 0 dBm. The I channel is driven by a sine wave, and the Q channel is driven by a cosine wave. The lower sideband is the single sideband (SSB) output.

The majority of characterization for the ADL5371 was performed using a 1 MHz sine wave signal with a 500 mV common-mode voltage applied to the baseband signals of the DUT. The baseband signal path was calibrated to ensure that the V_{IOS} and V_{QOS} offsets on the baseband inputs were minimized, as close as possible, to 0 V before connecting to the DUT. See the Carrier Feedthrough Nulling section for the definitions of V_{IOS} and V_{QOS}.

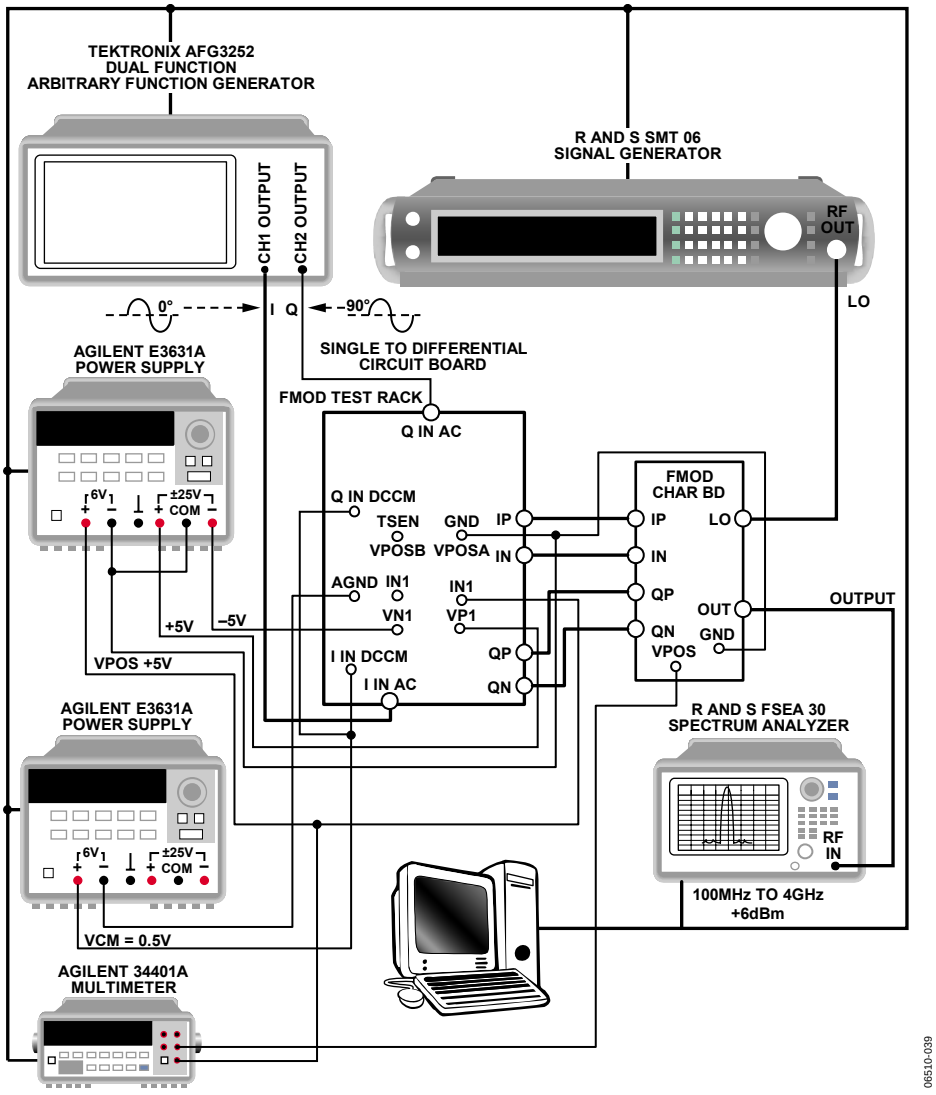
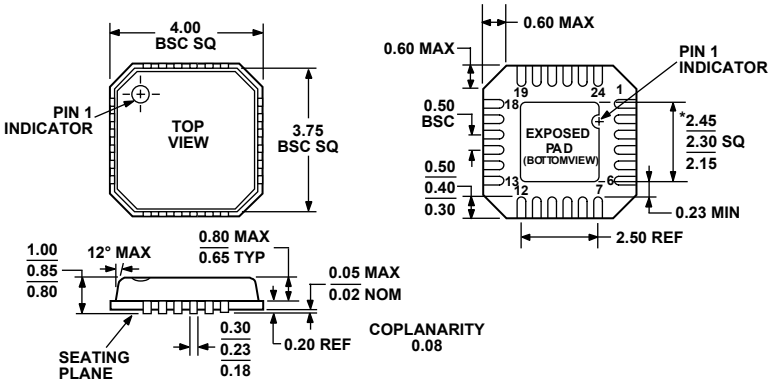


Figure 37. Setup for Baseband Frequency Sweep and Undesired Sideband Nulling

The setup used to evaluate baseband frequency sweep and undesired sideband nulling of the ADL5371 is shown in Figure 37. The interface board has circuitry that converts the single-ended I/Q inputs from the arbitrary function generator to differential I/Q baseband signals with a dc bias of 500 mV. Undesired sideband nulling was achieved through an iterative process of adjusting amplitude and phase on the Q channel. See the Sideband Suppression Optimization section for a detailed discussion on sideband nulling.

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-2
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 38. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5371ACPZ-R2[1]	–40°C to +85°C	24-Lead LFCSP_VQ, 7" Tape and Reel	CP-24-2	250
ADL5371ACPZ-R7[1]	–40°C to +85°C	24-Lead LFCSP_VQ, 7" Tape and Reel	CP-24-2	1,500
ADL5371ACPZ-WP[1]	–40°C to +85°C	24-Lead LFCSP_VQ, Waffle Pack	CP-24-2	64
ADL5371-EVALZ[1]		Evaluation Board		

[1] Z = Pb-free part.

NOTES

D06510-0-1/07(0)

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