

ESD7104

Transient Voltage Suppressors

Low Capacitance ESD Protection for High Speed Data

The ESD7104 transient voltage suppressor is designed to protect high speed data lines from ESD. Ultra-low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow-through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines such as USB 3.0 and HDMI.

Features

- Low Capacitance (0.3 pF Typical, I/O to GND)
- Low ESD Clamping Voltage
- Protection for the Following IEC Standards:
IEC 61000-4-2 (Level 4)
- UL Flammability Rating of 94 V-0
- This is a Pb-Free Device

Typical Applications

- USB 3.0
- eSATA 3.0
- Thunderbolt (Light Peak)
- HDMI 1.3/1.4
- Display Port

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T _J	-55 to +125	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T _L	260	°C
IEC 61000-4-2 Contact (ESD)	ESD	±15	kV
IEC 61000-4-2 Air (ESD)	ESD	±15	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

See Application Note AND8308/D for further description of survivability specs.



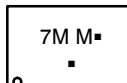
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MARKING DIAGRAM



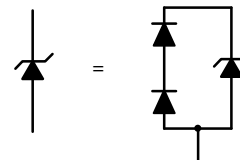
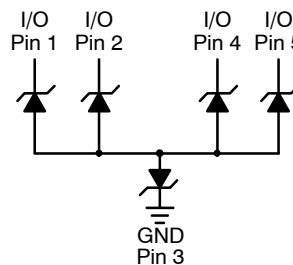
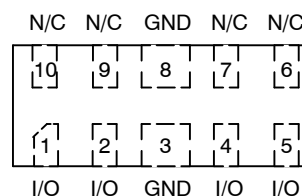
UDFN10
CASE 517BB



7M = Specific Device Code (tbd)
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONFIGURATION AND SCHEMATIC



ORDERING INFORMATION

Device	Package	Shipping
ESD7104MUTAG	UDFN10 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			5.0	V
Breakdown Voltage	V_{BR}	$I_T = 1\text{ mA}$, I/O Pin to GND	5.5			V
Reverse Leakage Current	I_R	$V_{RWM} = 5\text{ V}$, I/O Pin to GND			1.0	μA
Clamping Voltage (Note 1)	V_C	$I_{PP} = 1\text{ A}$, I/O Pin to GND (8 x 20 μs pulse)			10	V
Clamping Voltage (Note 2)	V_C	IEC61000-4-2, $\pm 8\text{ KV}$ Contact	See Figures 1 and 2			V
Clamping Voltage (Note 3)	V_C	$I_{PP} = \pm 8\text{ A}$ $I_{PP} = \pm 16\text{ A}$		14.1 19.5		V
Junction Capacitance	C_J	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$ between I/O Pins		0.2	0.3	pF
Junction Capacitance	C_J	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$ between I/O Pins and GND		0.3	0.35	pF

1. Surge current waveform per Figure 5.
2. For test procedure see Figures 3 and 4 and application note AND8307/D.
3. ANSI/ESD STM5.5.1 – 2008 Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
TLP conditions: $Z_0 = 50\ \Omega$, $t_p = 100\text{ ns}$, $t_r = 4\text{ ns}$, averaging window; $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$.

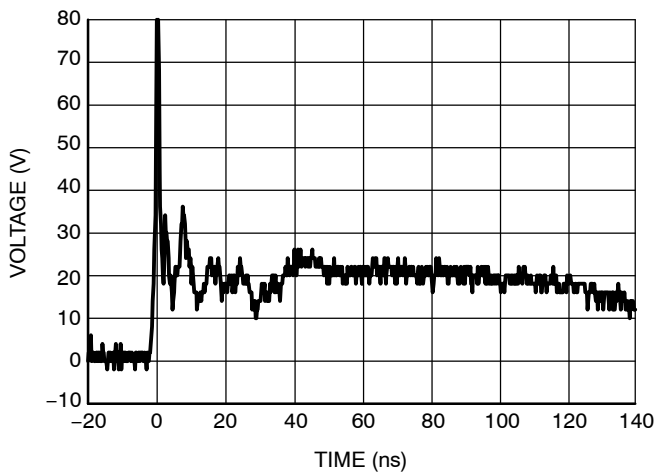


Figure 1. IEC61000-4-2 +8 KV Contact Clamping Voltage

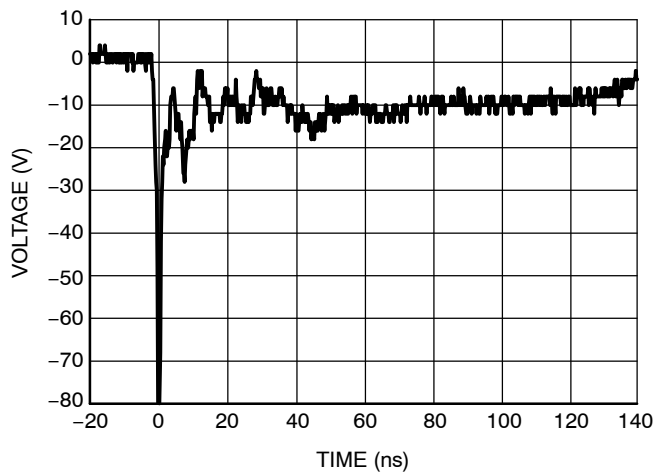


Figure 2. IEC61000-4-2 -8 KV Contact Clamping Voltage

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

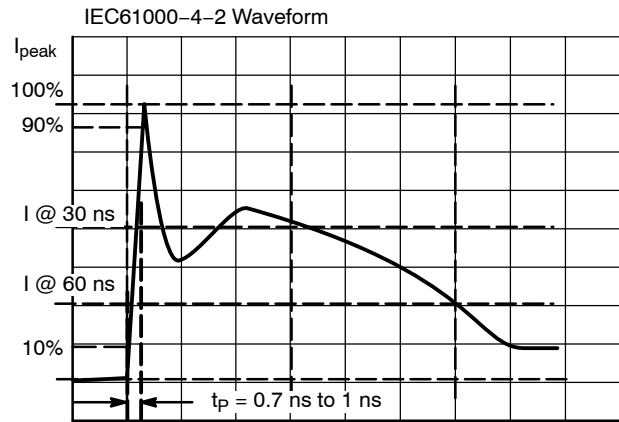


Figure 3. IEC61000-4-2 Spec

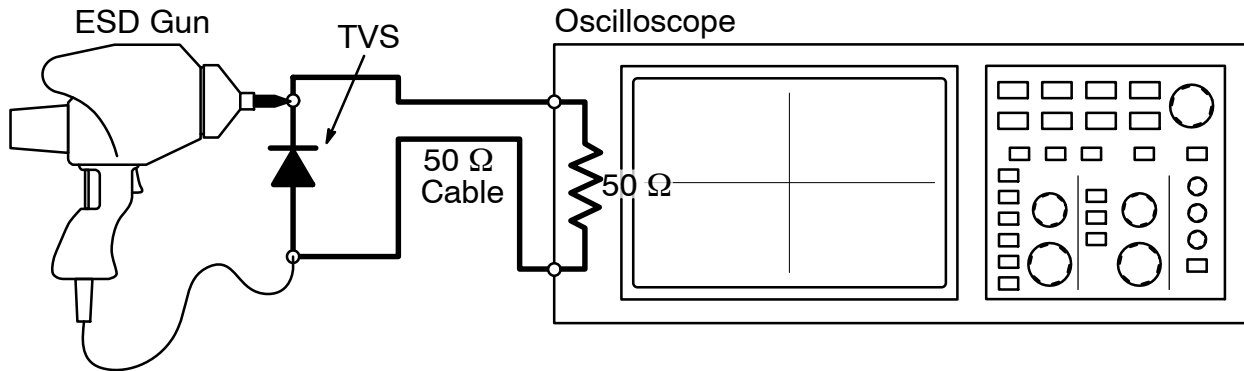


Figure 4. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

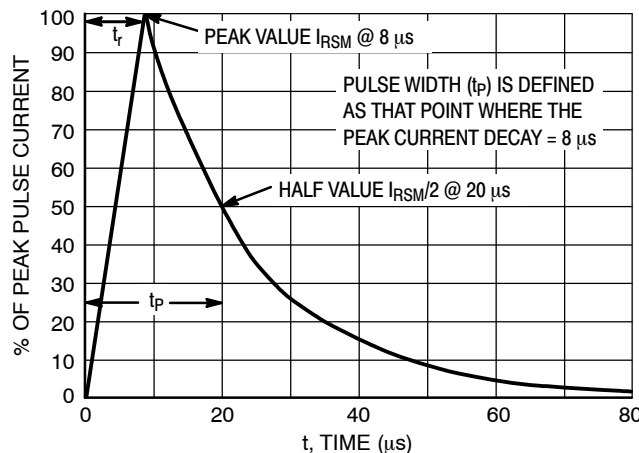


Figure 5. 8 X 20 μ s Pulse Waveform

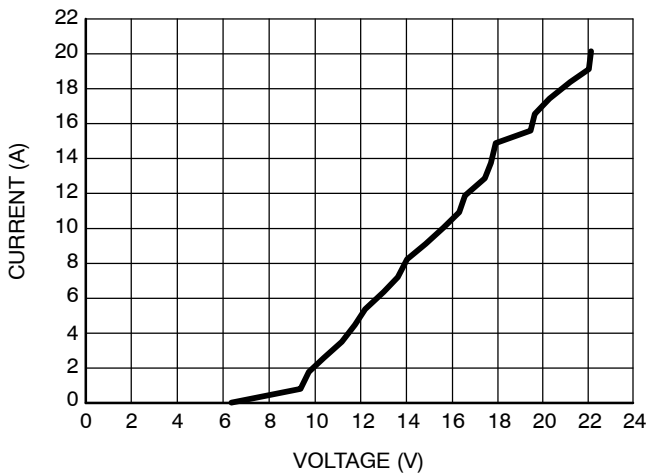


Figure 6. Positive TLP I-V Curve

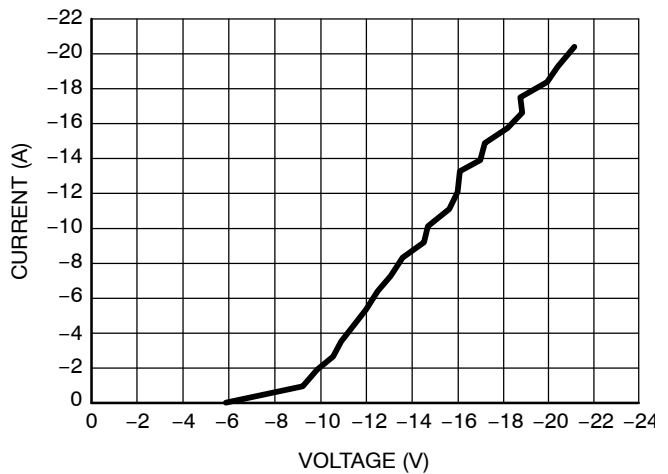


Figure 7. Negative TLP I-V Curve

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 8. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 9 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

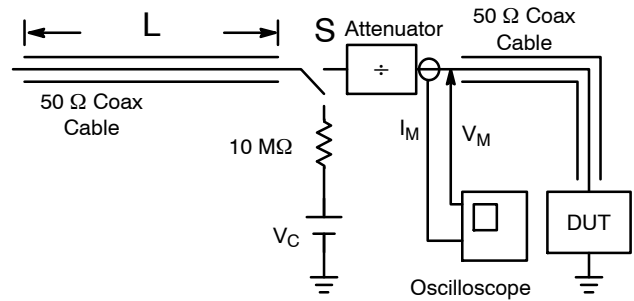


Figure 8. Simplified Schematic of a Typical TLP System

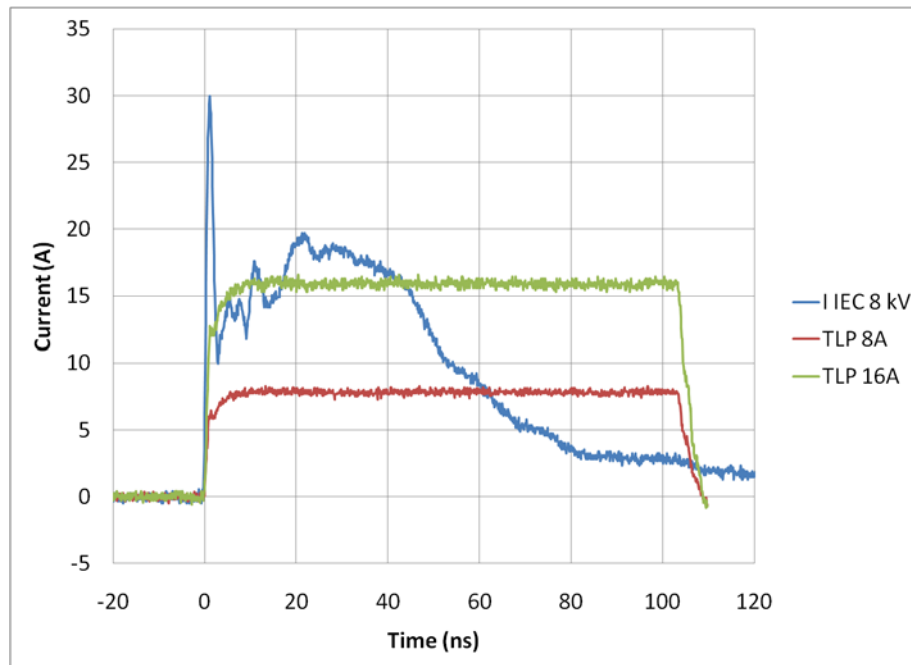


Figure 9. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

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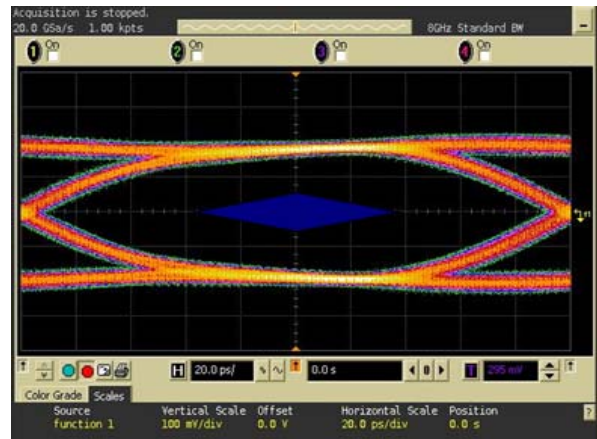
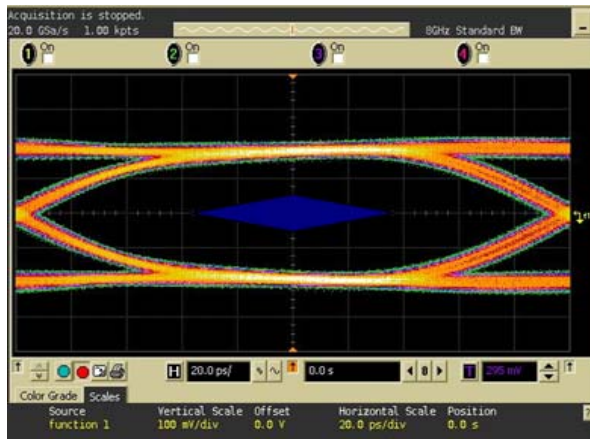


Figure 10. USB3.0 Eye Diagram with and without ESD7104. 5.0 Gb/s, 400 mV_{pp}

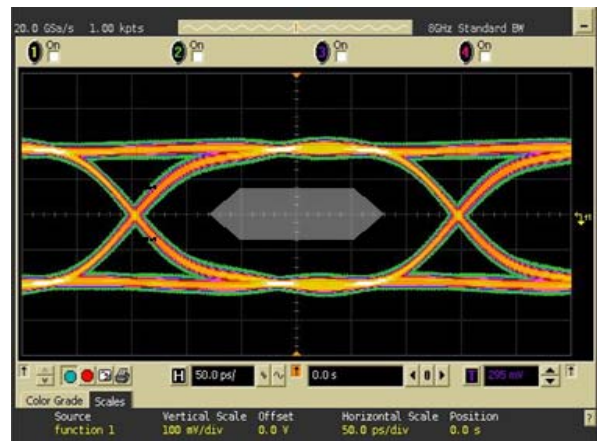
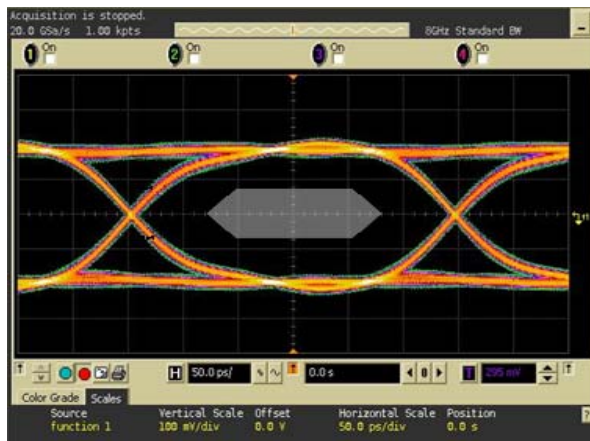


Figure 11. HDMI1.4 Eye Diagram with and without ESD7104. 3.4 Gb/s, 400 mV_{pp}

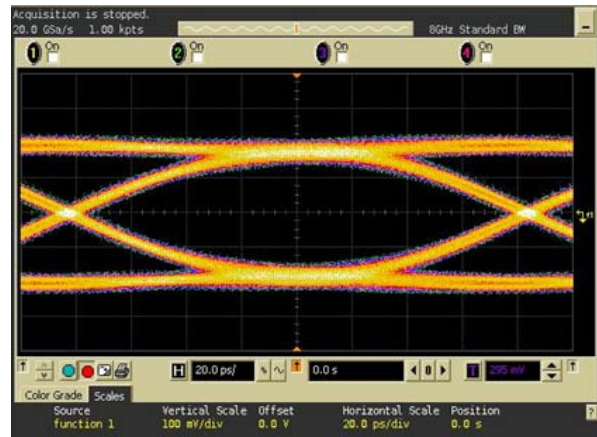
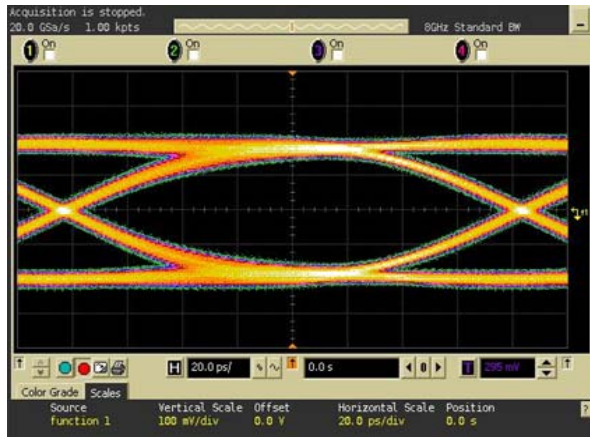


Figure 12. ESATA3.0 Eye Diagram with and without ESD7104. 6 Gb/s, 400 mV_{pp}

ESD7104

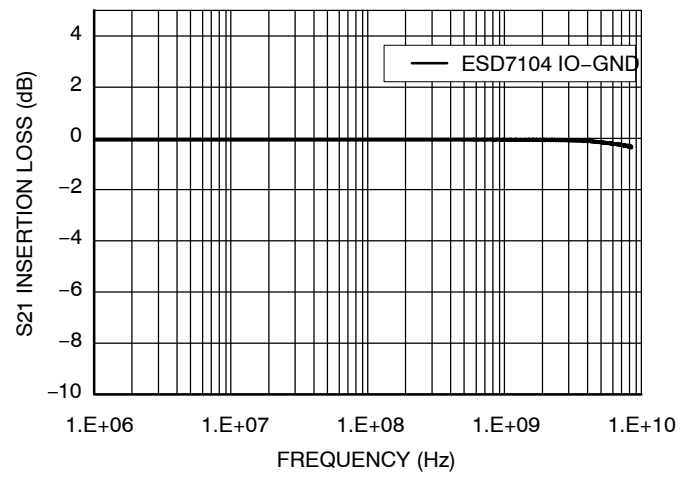


Figure 13. ESD7104 Insertion Loss

ESD7104

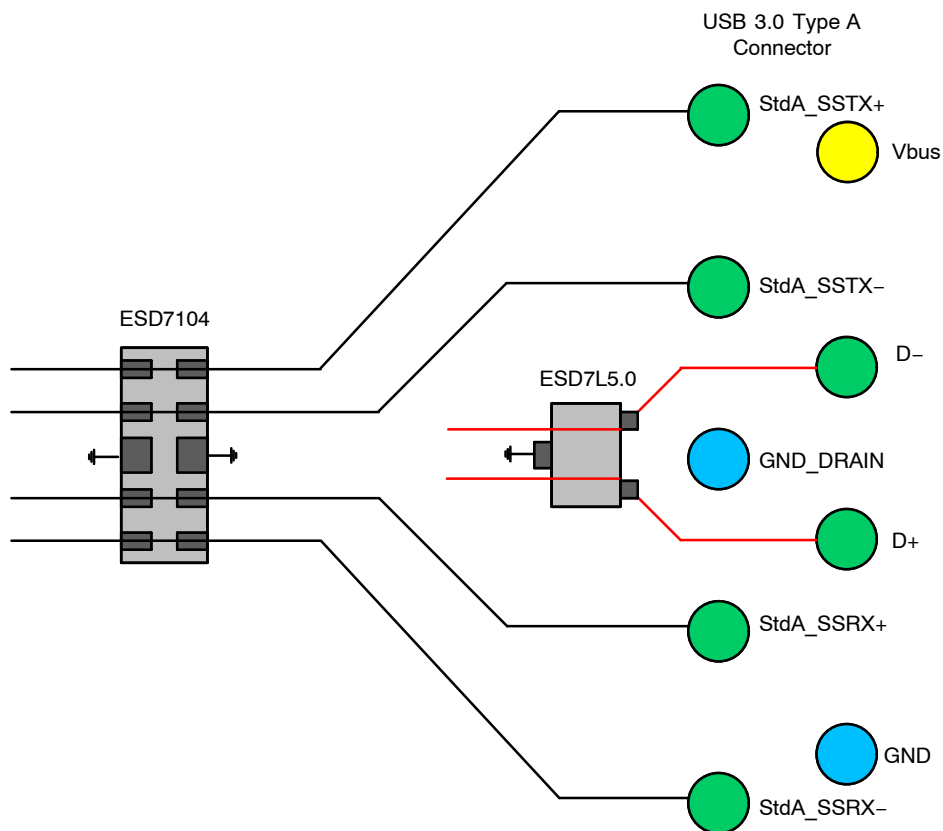


Figure 14. USB3.0 Standard A Connector Layout Diagram

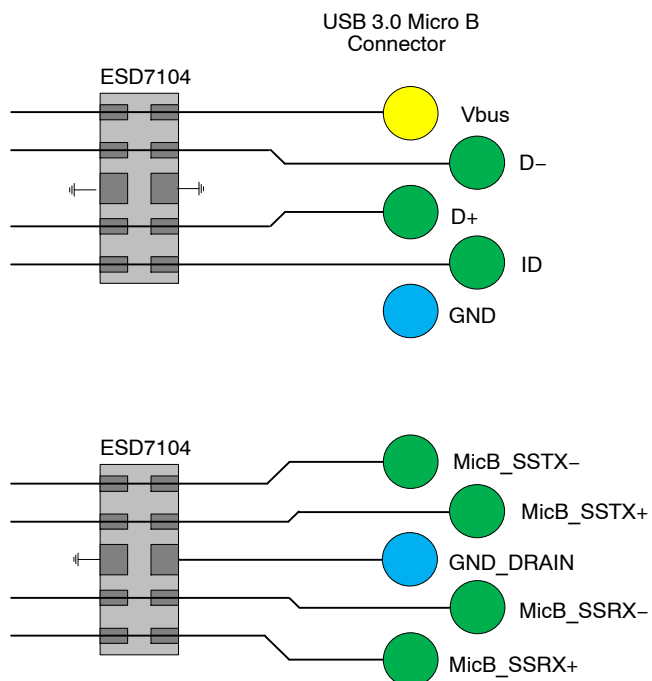


Figure 15. USB3.0 Micro B Connector Layout Diagram

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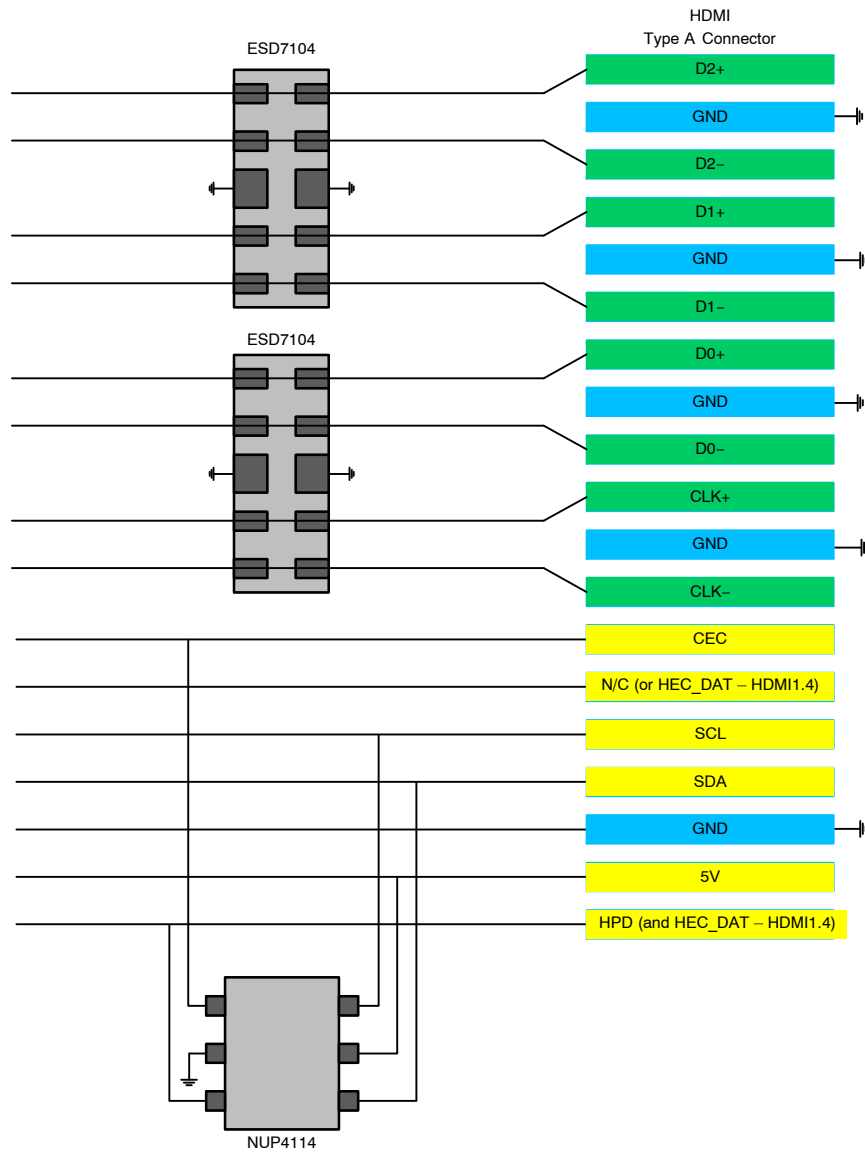


Figure 16. HDMI Layout Diagram

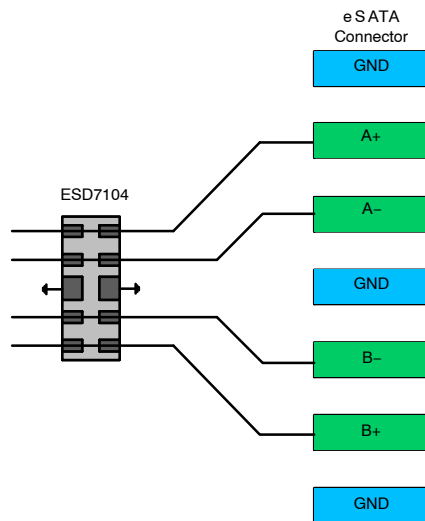
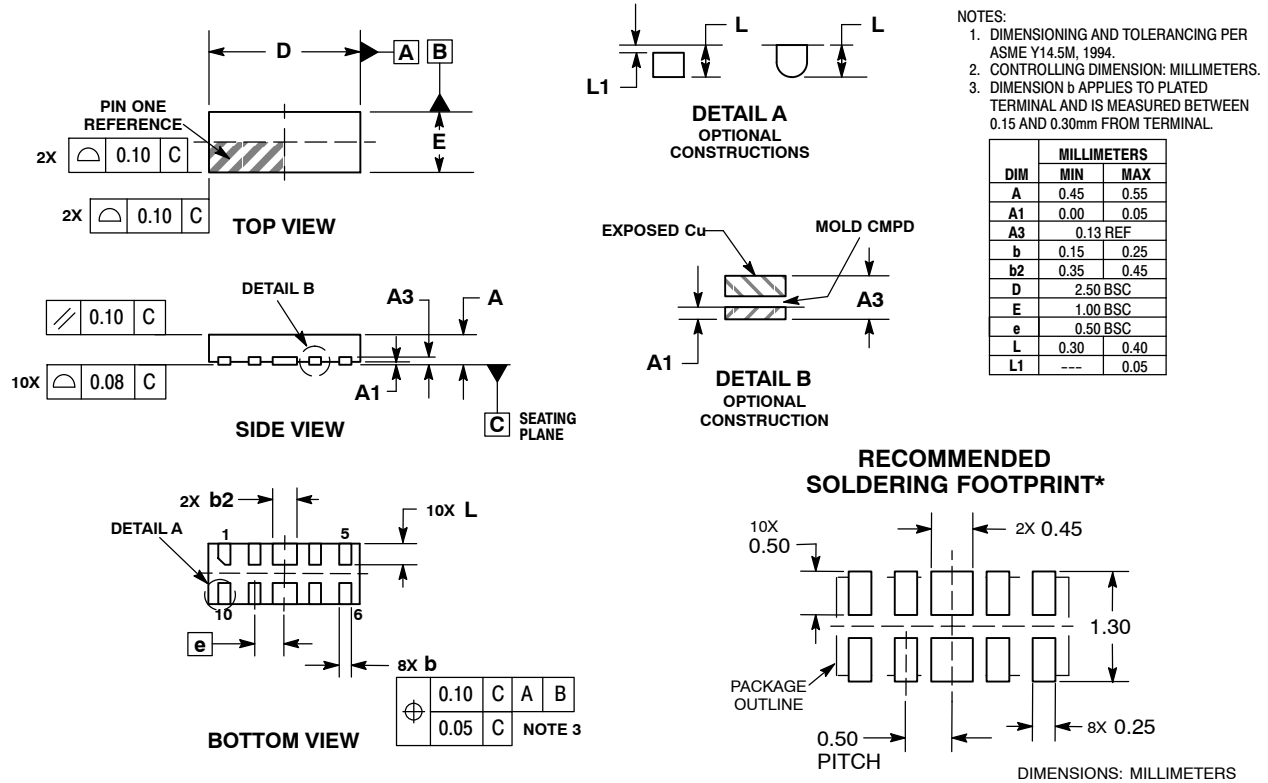


Figure 17. eSATA Layout Diagram

ESD7104

PACKAGE DIMENSIONS

UDFN10 2.5x1, 0.5P CASE 517BB ISSUE O



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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